

The HFT Detector-Elements Numbering Scheme

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The HFT consists of 3 subsystems; the PXL, the IST and the SST. This document describes a numbering scheme for each of the three subsystems.

The numbering convention in STAR is described in the controlled STAR-note **csn229B**¹. In that document the TPC is treated as a ‘two-view’ detector (East- and West-view) due to the physical separation of the East and West TPC chambers. The HFT subsystems are all constructed as a single piece, i.e. they are single-‘volume’ detectors. We have chosen the ‘convenient view’ (East or West) for each of them. The PXL detector is an East-view detector. We follow the STAR convention shown in Fig. 4 of csn229B. We keep the West-view convention for the former SSD detector. Likewise we consider the IST to be a West-view detector.

Internal software consistency requires a unique three-letter acronym for each of the subsystems. Therefore we have to select a new acronym for the former SSD, which will be SST. In terms of detector and physics description the detector continues to be named SSD.

STAR distinguishes between a ‘default view’ and a ‘detector view’. The default view is an East-view, whereas the individual detectors can follow an East- or West-view. The figures in this document adhere to the default (East) view. In the detector view, numbering of sectors or ladders is always clockwise.

An important consideration for a final phi-angle placement of the SST and IST ladders is mass distribution and ‘gap’ alignment between detectors, i.e. a tracking and physics optimization. We discuss this in more detail below.

PIXEL

Fig. 1 shows the PIXEL layout and numbering scheme. As in the TPC, the fundamental structure of the PIXEL detector is the **sector**. Each sector contains 4 **ladders** each with 10 **sensors**. The sectors are numbered clockwise from 1 through 10 when viewed from East. This numbering complies with csn229B (Fig. 4).

¹ <http://drupal.star.bnl.gov/STAR/subsys/hft>

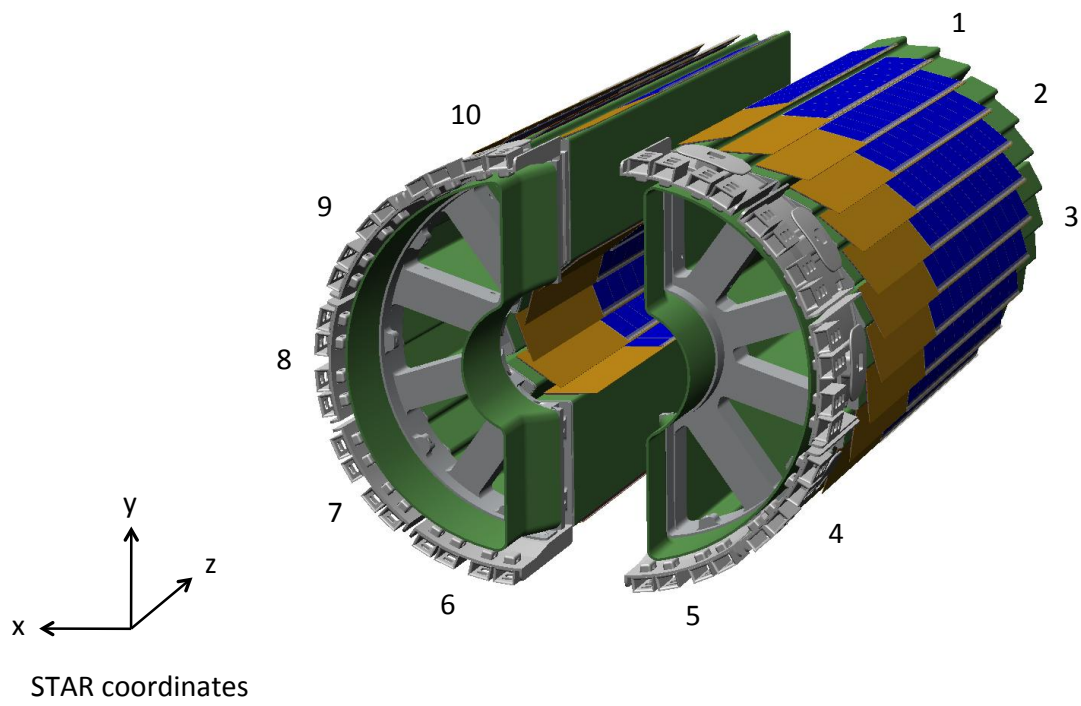
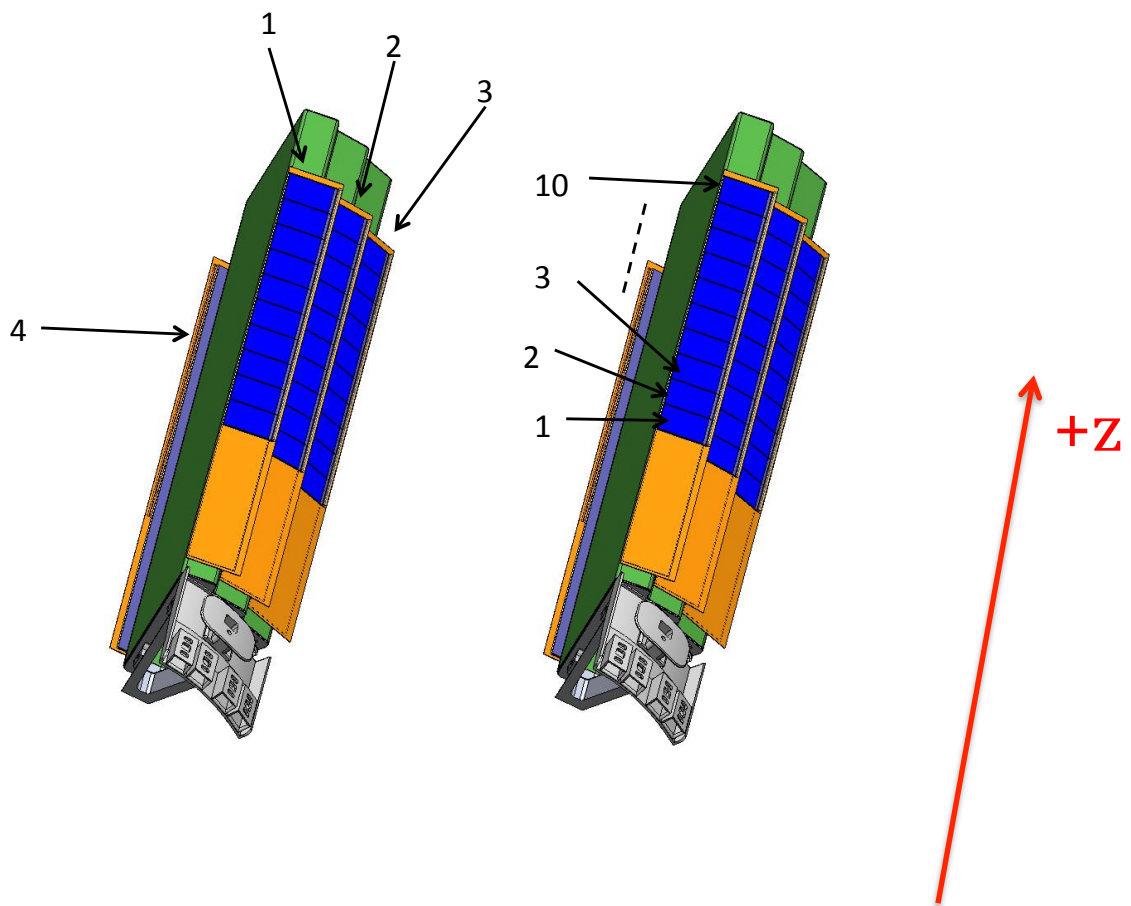


Figure 1: The PIXEL detector layout.



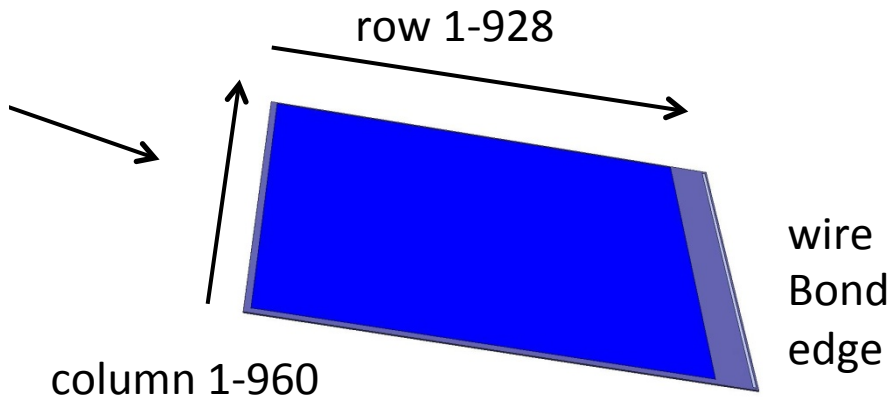


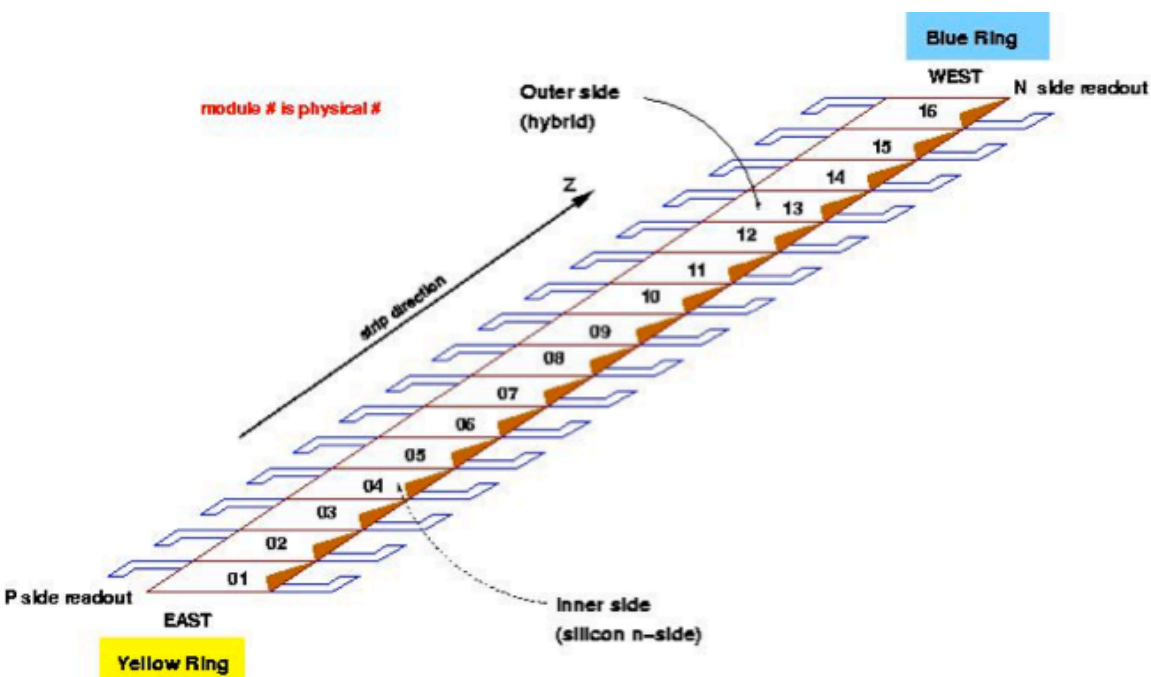
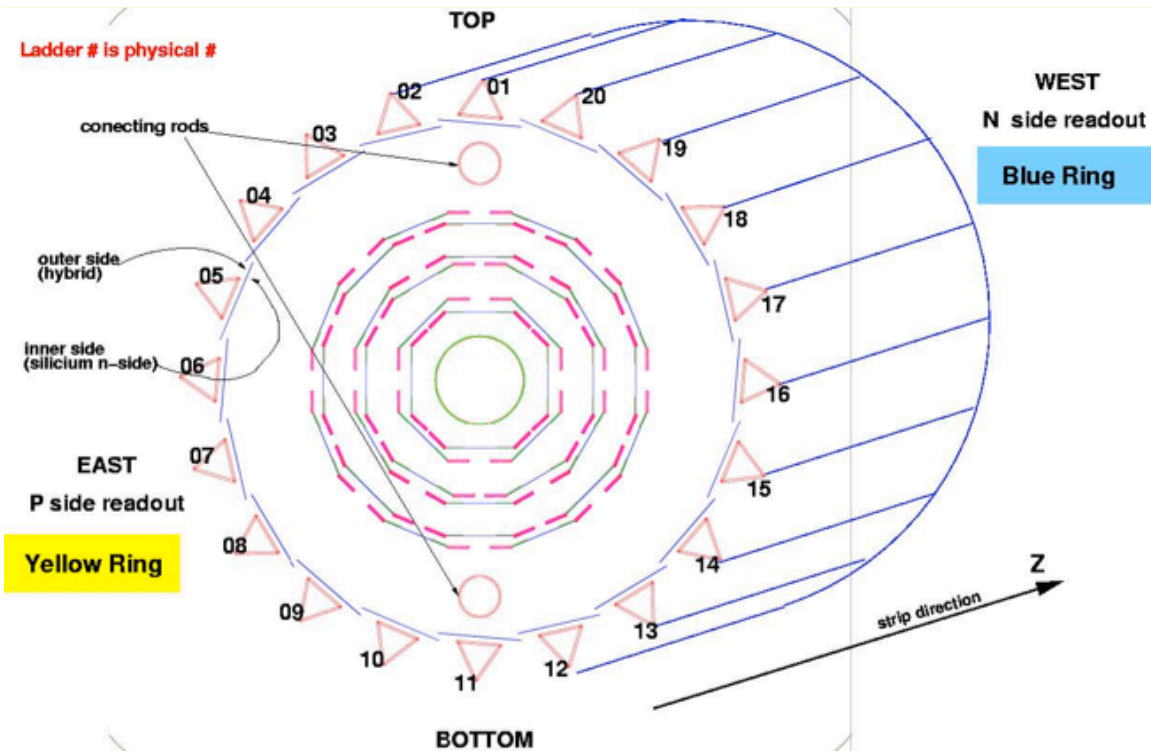
Figure 2: The numbering conventions of ladders on sectors, sensors on ladder and pixels on sensor.

The ladders on each sector are numbered clockwise from 1 to 4, with 4 being the inner ladder of each sector (Fig. 2).

The 10 sensors on a ladder are numbered from 1 through 10 counting from east (-z) to west (+z) to adhere to the STAR convention (Fig. 9 in cs229B). Figure 2 also shows the numbering convention for the individual pixels on the Ultimate sensor.

SST

The SST consists of 20 tiled ladders. The symmetry matches that of the PXL, so alignment of overlap regions has to be coordinated with the PXL rather than with TPC and IST, where this symmetry is broken.



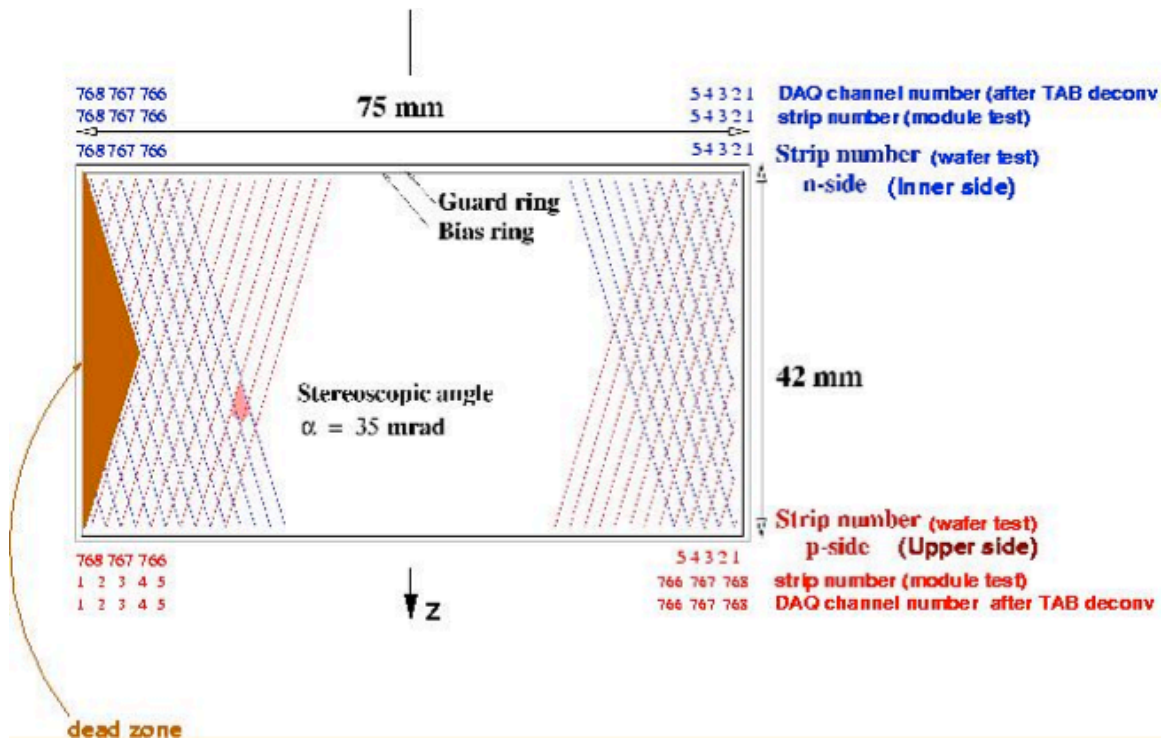


Figure 3: The naming scheme of the SST. This is an East-view of the detector.

Figure 3 shows the naming convention for the SST. The ladders are numbered clockwise from 1 to 20, starting at 12 o'clock using a West-view (default) of the detector. The only non-compliant element in this numbering is that ladder-01 straddles the y-axis.

Given the flexibility in placing the SST ladders on its support structure, one has to consider and weigh arguments based on symmetry (20 SST ladders to cover 10 PXL sectors) and physics (ϕ profile of SST radiation thickness and its alignment to TPC and/or PXL gaps based on impact on high p_T particles). Based primarily on system symmetry arguments, pending confirmation from full-scale simulations using an adequate geometry, at this time we align the SST ladders with the PXL sectors (two ladders per sector). This layout is shown in Fig. 4 that also shows the numbering of the SST ladders. This numbering fully complies with the STAR convention.

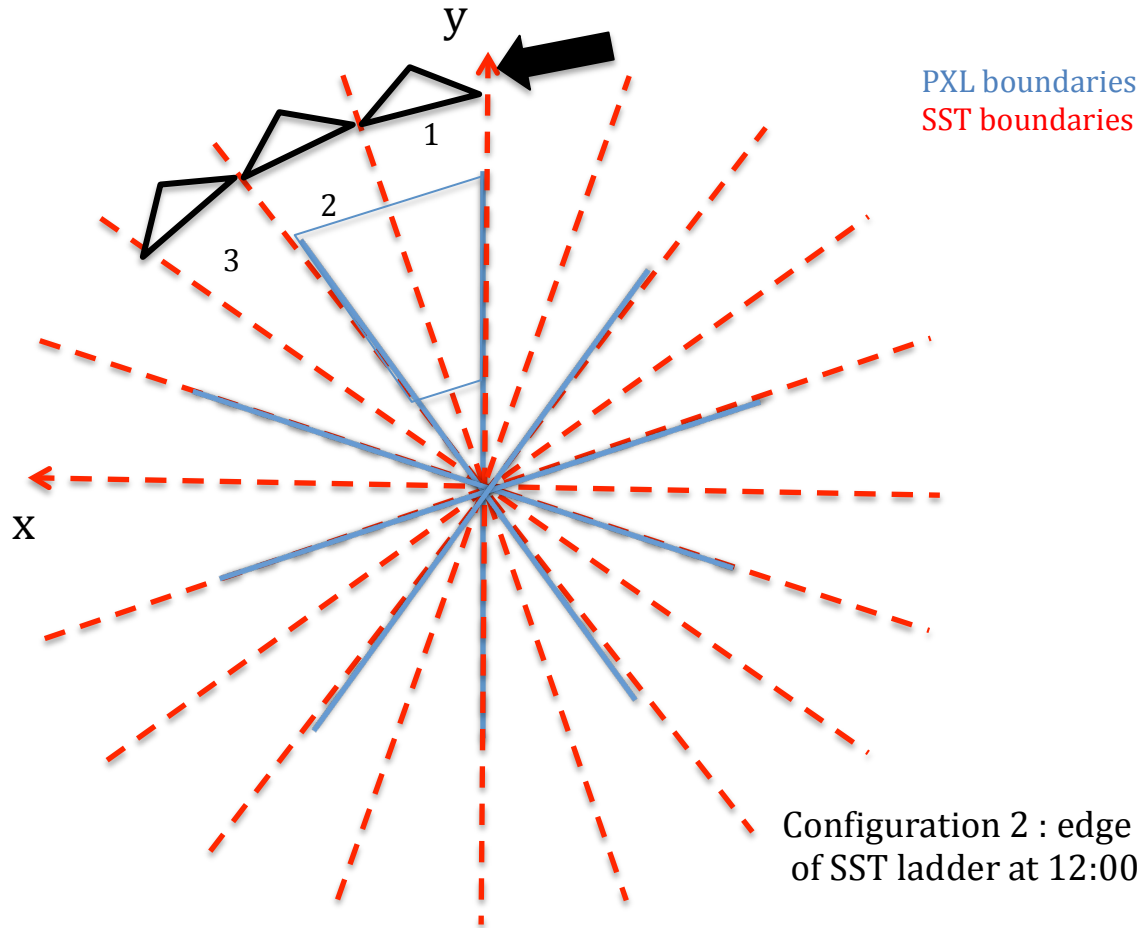


Figure 4: The numbering of the SST and its alignment with the PXL. This is an East-view of the configuration.

IST

The IST has a similar structure as the SST (a single layer, wafer/ladder based detector) and, independent of the relative fine tuning of their ladders, the overall number scheme is the same, e.g. a West-view ladder number etc. The IST consists of 24 ladders, exactly twice the number of TPC sectors (12). Each ladder will have 6 sensors, each read out by 6 APV chips. Each sensor is a pad detector with 12 columns and 64 rows with the columns along the z-direction, shown in detail in Fig. 6 and Fig. 7.

Following similar system-symmetry arguments as in the SST case, the alignment of the IST ladders with the TPC sectors is shown in Fig. 5 (see also Fig. 8). Also shown is the ladder numbering. The IST is a West-view detector. In that view the numbering of ladders is clockwise. Note that Figure 5 shows an East-view of the detector, the default view for all figures in this document. This arrangement complies with the STAR convention.

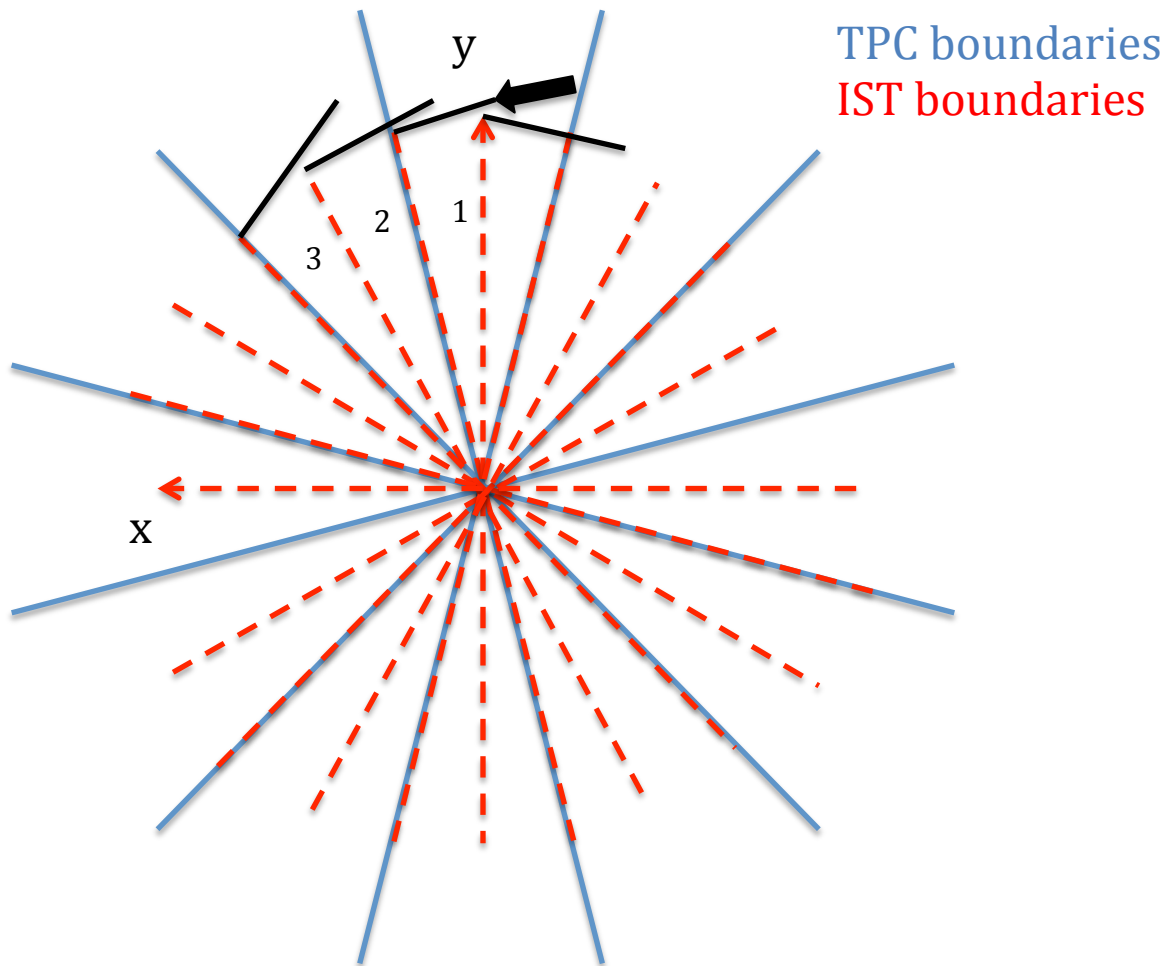


Figure 5 The numbering and alignment of IST ladders with the TPC sectors. This again is an East-view of the configuration.

The IST ladders are arranged and tiled as shown in Fig. 5 (also see the lower-left insert of Fig. 6). The silicon sensors are mounted on the bottom of the ladder, i.e. they are facing the interaction zone as shown in the Fig. 6 insert. In the same figure one sees the naming of the wafers on the ladder according to the STAR convention, starting from the East.

The main body of Fig. 6 shows a prototype IST ladder, from the side the sensors and the readout chips are mounted. In this figure there are no sensors and no chips mounted, the arrows point to the corresponding mounting positions.

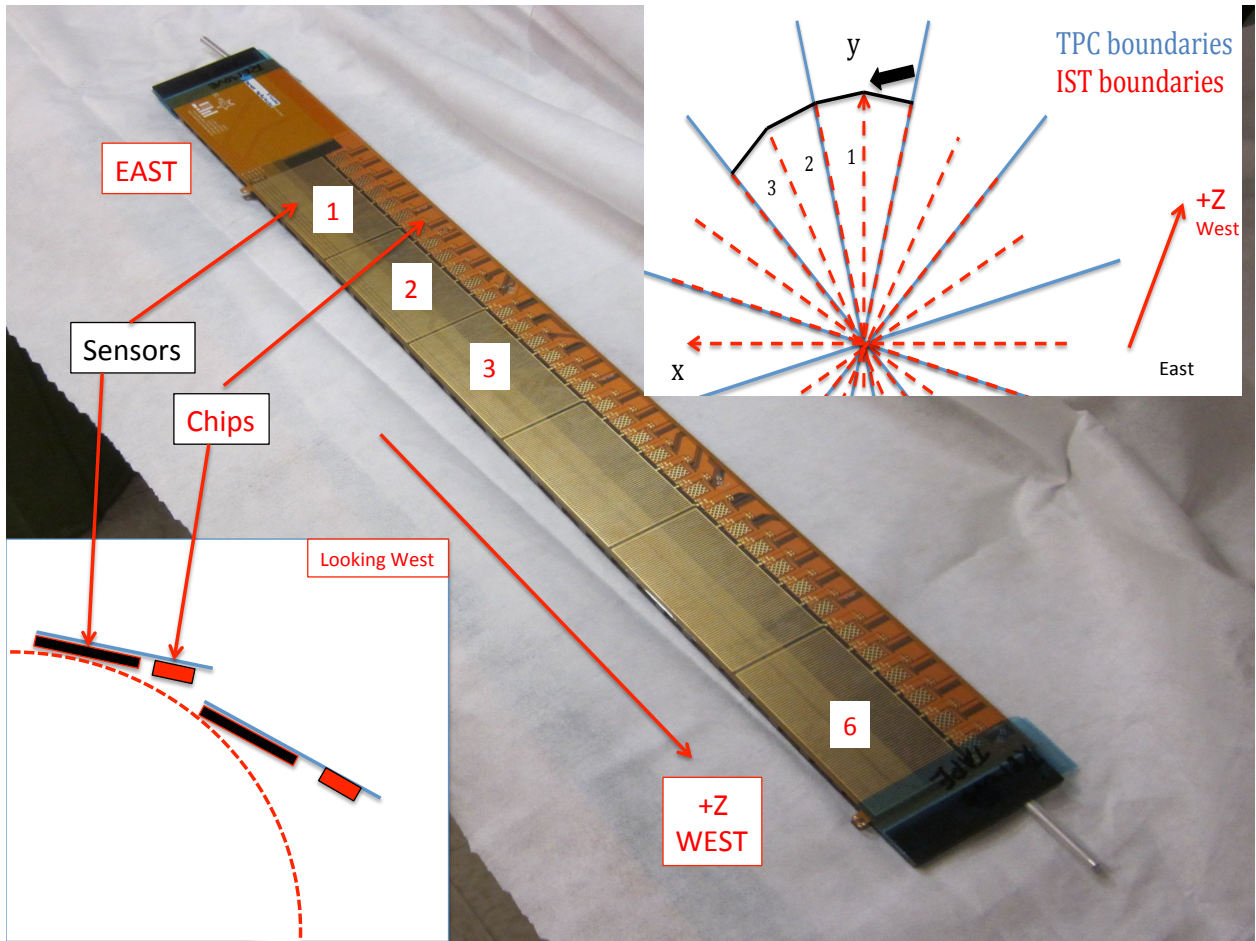


Figure 6: IST sensor numbering on a ladder. The lower-left insert schematically shows the tiling and orientation of the sensors on the ladder. In reality the sensors are tiled with a small overlap.

Figure 7 shows a top view of one wafer/sensor. The readout chips in this figure are shown as small green boxes at the bottom, where they are mounted. In the STAR convention the columns are counted from 1 to 12 from low to high z, i.e. starting from East going West, and the rows from 1 to 64, clockwise in phi if the ladder is viewed from the West. This way the row next to the readout chip is row-1 and the row farthest away is row-64. Figure 8 shows a (modified) Solid Works snapshot (with a zoom) of the phi rotated IST so that it aligns with the TPC sectors. The dotted line in the figure is the y-axis (up). One can see that the y-axis passes through the middle of the overlapping active wafer areas (deep blue in the figure) of ladder number one and twenty-four.

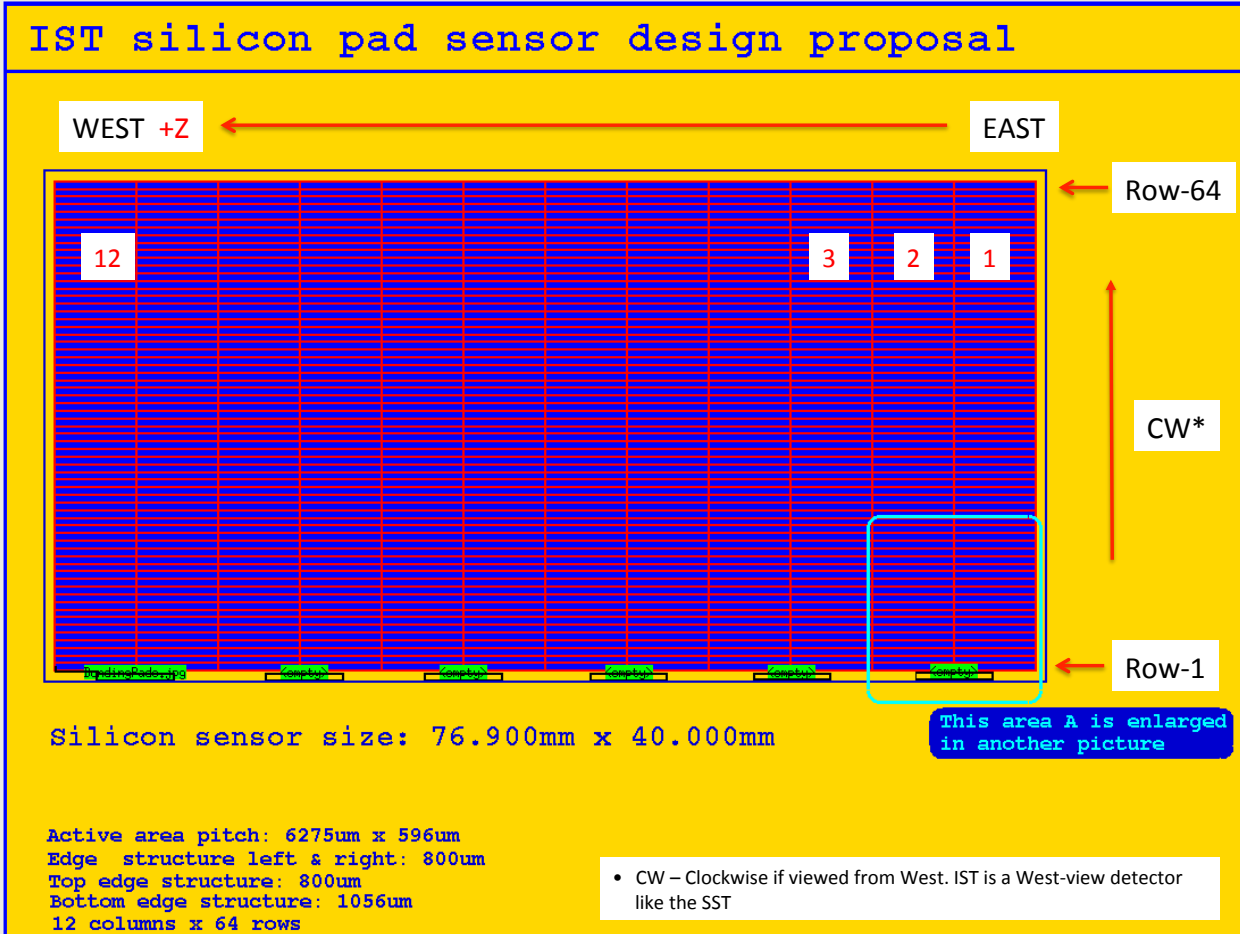


Figure 7: The numbering of pads on an IST sensor

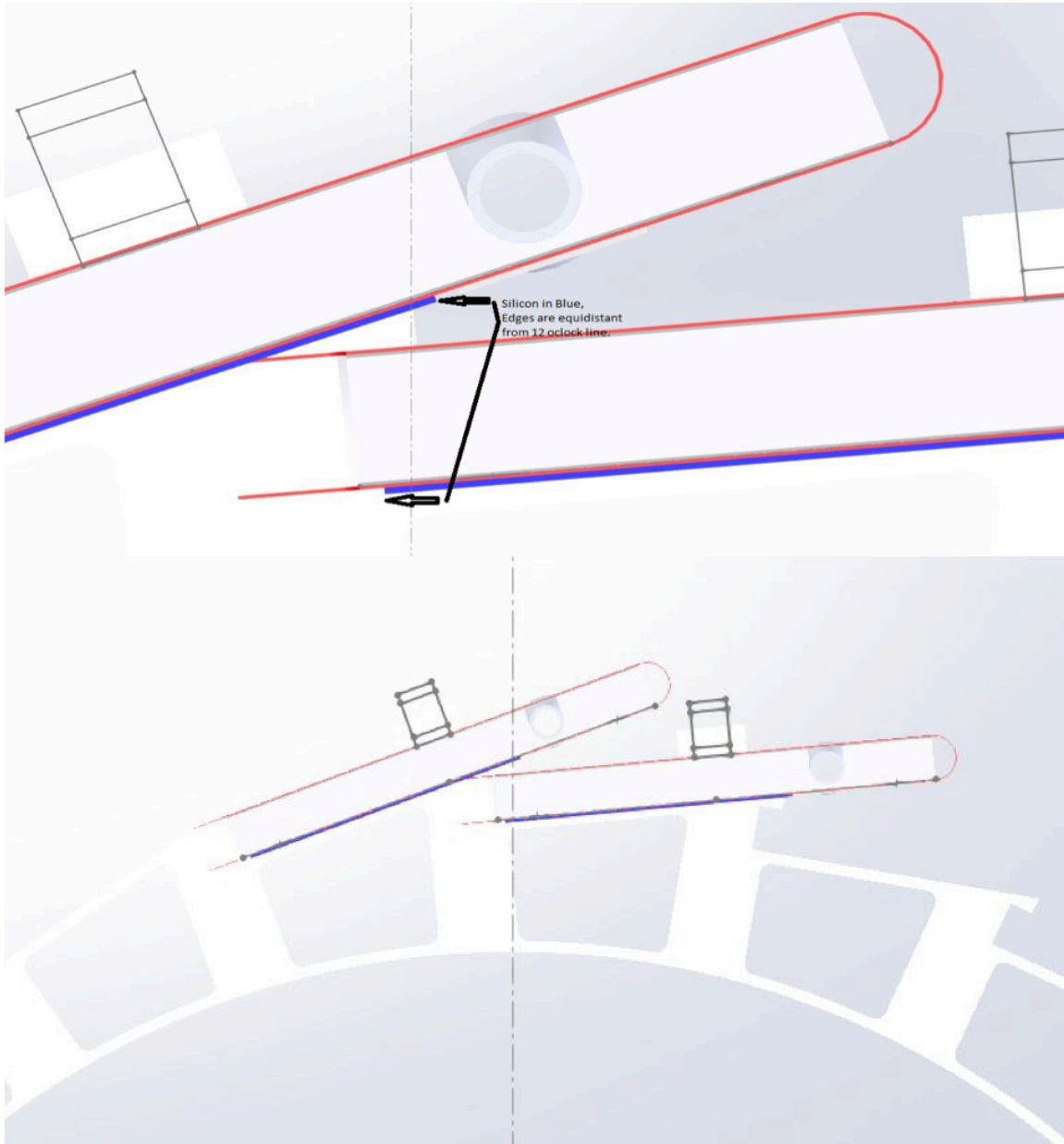


Figure 8 Solid works snapshot (and detail) of the IST tiling and phi placement relative to the y-axis (dotted line)

Supplemental HFT Conventions for Alignment

The HFT detector contains subsystems with varying minimum entities. The SSD and IST, for example, have sensors (wafers) and ladders whereas the PIXEL detector has sensors, ladders and sectors arranged in two hemispheres. For SSD and IST would make sense to use e.g. barrel-number ID, but this makes no sense for PIXELS. But, for analysis and calibration purposes, it would make sense to keep in the hit structure 'layer' information as defined by the distance from the beam-pipe center.

This information (index) can be used to sort hits etc. In figure 8 we define this 'layer' assignment starting from inside. This way the PIXEL detector can be viewed as a two layer pixel detector, one at 2.5cm and one at 8cm, the IST as layer-3 at 14cm and the SSD as layer-4 at 20cm from the beam.

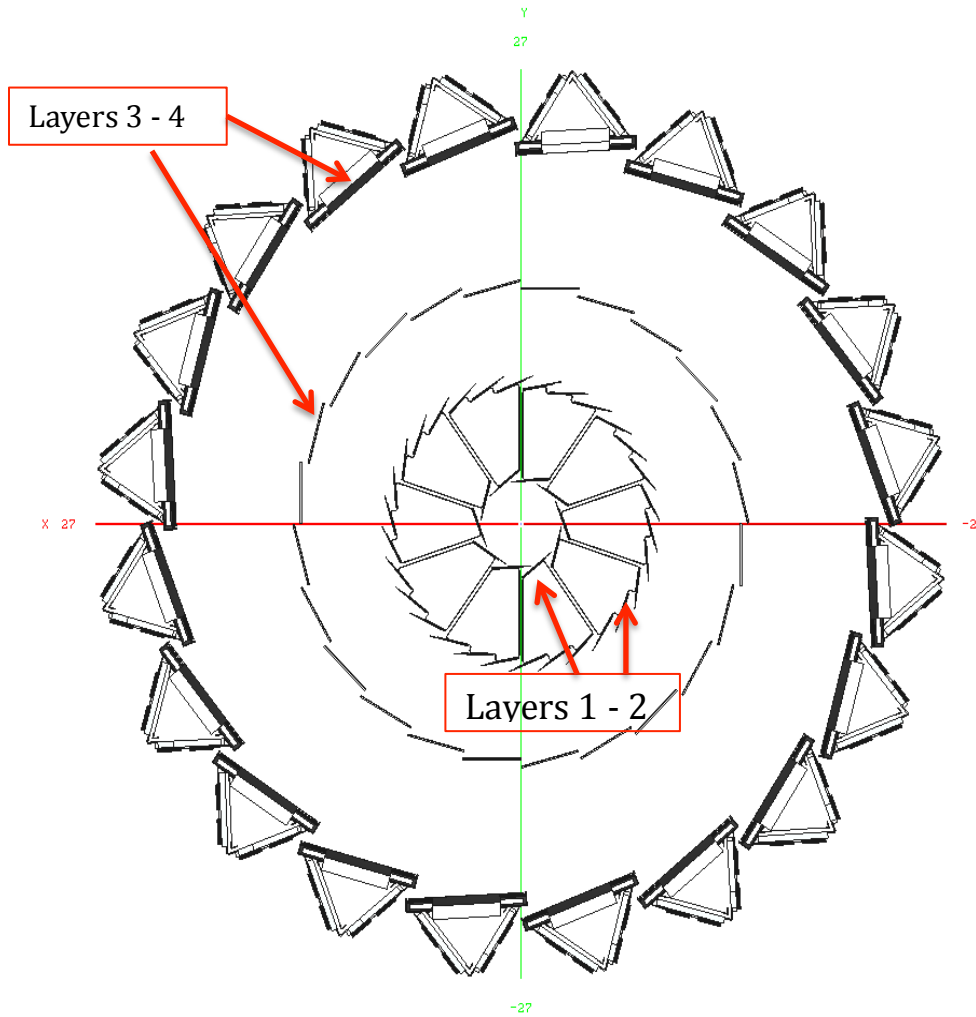


Figure 8 Layer naming convention for the HFT detector