SSD upgrade Electronics

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SSD electronics status

- Mechanical prototype of ladder board
  - Delivered
- Procurement of ladder board PCB
  - BNL will purchase board fab from Protechno (French vendor)
- Detailed study of time required to configure ladder FPGA (SEU)
  - Need to configure 40 ladders concurrently
  - Done from RAM attached to each RDO slave FPGA

SSD electronics status (2)

- Changes to ladder board
  - Switch to passive serial loading to configure ladder FPGA
    - Due to inadequate support by Altera for JTAG protocol
    - Requires re-routing 2 signals on ladder board
  - Change power connection to Nicomatic connector
    - Formerly hard-soldered pigtail

SSD electronics schedule

Item	Start date	Finish date
Final change to ladder board layout	5/10	5/10
Fabricate ladder board funct. prototype	6/10	8/10
Debug ladder board prototype	8/10	11/10
Finish RDO FPGA code	5/10	8/10
Specify RDO FPGA pinouts	7/10	7/10
RDO layout	8/10	9/10
RDO fabrication (prototype)	11/10	12/10
Debug RDO	1/11	7/11
Integrate RDO-ladder/debug	7/11	10/11
Slow controls software	6/11	6/12
DAQ software	10/11	12/11

Resources

Item	Start date	Time req'd	People involved
Final change to ladder board layout	5/10	2 wks	CR
Fabricate ladder board funct. prototype	6/10	8 wks	RAS, JH, MJL
Debug ladder board prototype	8/10	12 wks	MJL, RAS, CR
Finish RDO FPGA code	5/10	12 wks	MJL, CR
Specify RDO FPGA pinouts	7/10	3 wks	CR
RDO layout	8/10	4 wks	JH, RAS
RDO fabrication (prototype)	11/10	3 wks	JH
Debug RDO	1/11	20 wks	MJL, CR, RAS
Integrate RDO-ladder/debug	7/11	12 wks	MJL, CR
Slow controls software	6/11	30 wks	TBD
DAQ software	10/11	4 wks	MJL

CR: Christophe Renard (Subatech), RAS: Bob Scheetz (BNL), JH: John Hammond (BNL), MJL: M. LeVine (BNL), TBD: to be determined
Underlined: principal effort

Summary

- Progress is slower than hoped
- No major problems
- No major changes to estimated cost