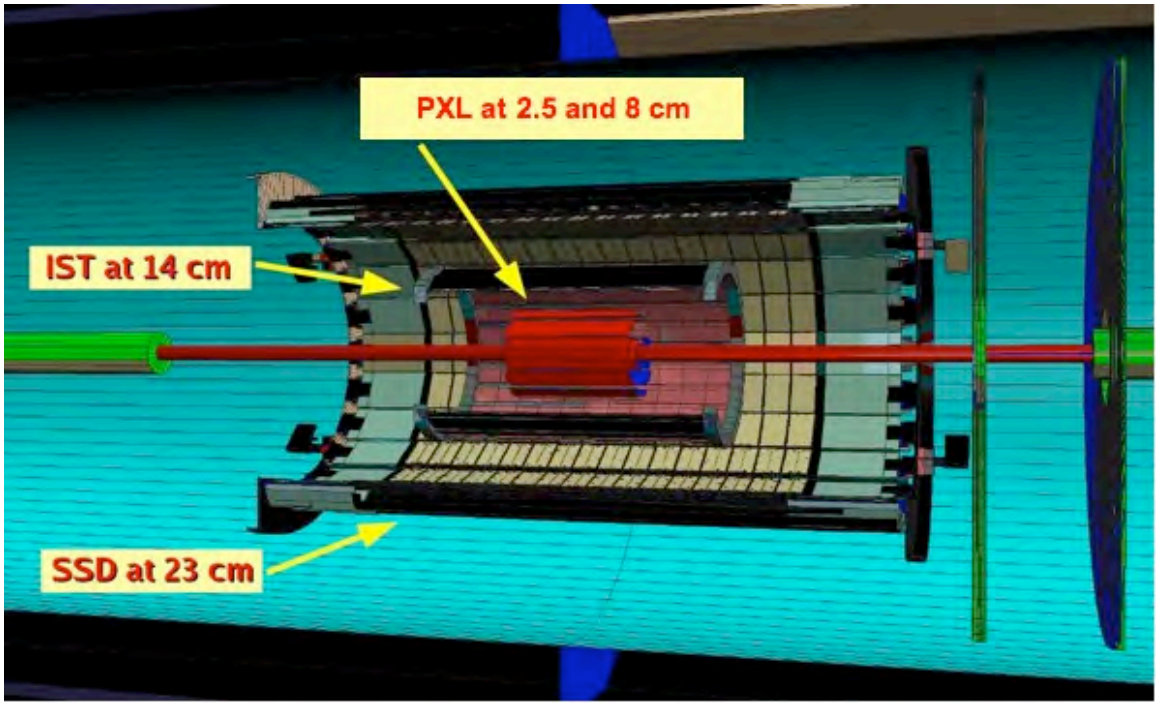
A Heavy Flavor Tracker for STAR



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List Bullet: for bullet lists

A more detailed manual is the write-up by Jim: "WordFormatingNotes"

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1. Introduction

The STAR Collaboration proposes to construct a state-of-the-art microvertex detector, the Heavy Flavor Tracker (HFT), utilizing active pixel sensors and silicon strip technology. The HFT will significantly extend the physics reach of the STAR experiment for precision measurement of the yields and spectra of particles containing heavy quarks. This will be accomplished through topological identification of D mesons by reconstruction of their displaced decay vertices with a precision of approximately 50 μm in p+p, d+A, and A+A collisions.

The HFT consists of 4 layers of silicon detectors grouped into three sub-systems with different technologies, guaranteeing increasing resolution when tracking from the TPC towards the vertex of the collision. The Silicon Strip Detector (SSD) is an existing detector in double-sided strip technology. It forms the outermost layer of the HFT. The Intermediate Silicon Tracker (IST), consisting of a layer of single-sided strip-pixel detectorss, is located inside the SSD. Two layers of Silicon Pixel Detector (PIXEL) are inside the IST. The PIXEL detectors have the resolution necessary for a precision measurement of the displaced vertex.

The PIXEL detector will use CMOS Active Pixel Sensors (APS), an innovative technology never used before in a collider experiment. The APS sensors are only 50 μm thick with the first layer at a distance of only 2.5 cm from the interaction point. This opens up a new realm of possibilities for physics measurements. In particular, a thin detector (0.28% radiation length per layer) in STAR makes it possible to do the direct topological reconstruction of open charm hadrons down to very low p_T by the identification of the charged daughters of the hadronic decay.

2. Physics Motivation

The primary motivation for the HFT is to extend STAR's capability to measure heavy flavor production by the measurement of displaced vertices and to do the direct topological identification of open charm hadrons. These are key measurements for the heavy-ion and spin physics programs at RHIC. Heavy quark measurements will facilitate the heavy-ion program as it moves from the discovery phase to the systematic characterization of the dense medium created in heavy-ion collisions as well as obtain a detailed measurement of the nucleon spin structure in polarized p+p collisions. The primary physics topics to be addressed by the HFT include heavy flavor energy loss, flow, and a test of partonic thermalization at RHIC. This program has been identified as key goals for the RHIC program in the Long Range Plan RHIC-II science program and in the RHIC mid-term scientific plan.

From a precise measurement of the spectra and the production ratios of D-meson states, we will be able to extrapolate to the total yield for charm quark production. Furthermore, the open charm production rate is high enough at RHIC that the coalescence process becomes relevant for Charmonium production. Knowledge of the total production cross section for charm quarks is essential as a baseline for J/ψ measurements. A meaningful answer to the question of whether the J/ψ mesons are suppressed or enhanced at RHIC requires knowledge of the charm production in heavy-ion reactions.

A heavy quark can be used to probe the properties of the medium created in heavy-ion collisions. The radiation of gluons is kinematically suppressed for heavy flavored quarks passing through the medium: thus they should lose less energy in the dense medium. An important measurement to be made with the HFT is $R_{CP}R_{AA}$, the ratio of charmed meson production in central Au+Au collisions to the binary-scaled production rate in peripheral Auor +Au collisions. Current measurements using non-photonic electrons as a measure of the abundance of charm and bottom hadrons indicate that the rate of energy loss for heavy quarks is unexpectedly high and inconsistent with our current understanding in pQCD models. Based on the non-photonic electron data the theory of heavy quark energy loss is uncertain and may be completely wrong, especially with regards to bottom.

Another important measurement to be made with the HFT is a measurement of the elliptic flow of D-mesons down to very low p_T values. It is generally accepted that elliptic flow is established in the partonic phase. If charm quarks, with a mass much larger than the temperature of the system, undergo elliptic flow then it has to arise from many collisions with the abundant light quarks. Thus, flow of charm quarks can be taken as a probe for frequent re-scatterings of light quarks and is an indication of thermalization that may be reached in the early stages of heavy-ion collisions at RHIC. We believe that proof of thermalization constitutes the last step in the characterization of the strongly interacting matter created at RHIC. These important measurements require a very thin detector to push the measurement down to the lowest momenta where transverse elliptic flow is manifest.

Without the HFT upgrade the STAR experiment will not be able to execute the comprehensive heavy flavor program proposed here. However, STAR has been able to

complete some initial charm measurements with the TPC alone, and with the data from the recent Run 7 STAR might be able to make limited progress towards an initial estimate for the B-meson contribution to the spectrum of the non-photonic electrons in Au+Au collisions.

The complete physics case for the HFT has been presented in the HFT proposal[5] and has been presented in the HFT Science Review. In this Conceptual Design Report we will present the physics capabilities of the HFT in terms of charm flow, charm suppression, LC measurements, and the capability to distinguish between charm and bottom production. The first two points have been presented in detail already in the original proposal and we will present a brief summary while concentrating on the latter two points.

2.1. Charm Flow

Charm quarks are abundantly produced at RHIC energies. Due to their high mass and small interaction cross section, the strength of elliptic flow of heavy flavor hadrons may be a good indicator of thermalization occurring at the partonic level. If all quarks in heavy flavor hadrons flow with the same pattern as the quarks in the light flavor hadrons, this indicates frequent interactions between all quarks. Hence, thermalization of light quarks is likely to have been reached through partonic re-scattering.

Figure 1 shows what precision in flow measurement can be reached with 500 M minimum bias events taken in STAR with the HFT. The red points show expectations from a cascade model[1] for the case that the charm quark has the same size partonic flow as measured for the light quarks. The green points show the limiting case where the charm quark has zero partonic v2. Our measurement is expected to fall between those limits. It is obvious that the HFT will allow for a precision measurement that will shed light on the question of thermalization.

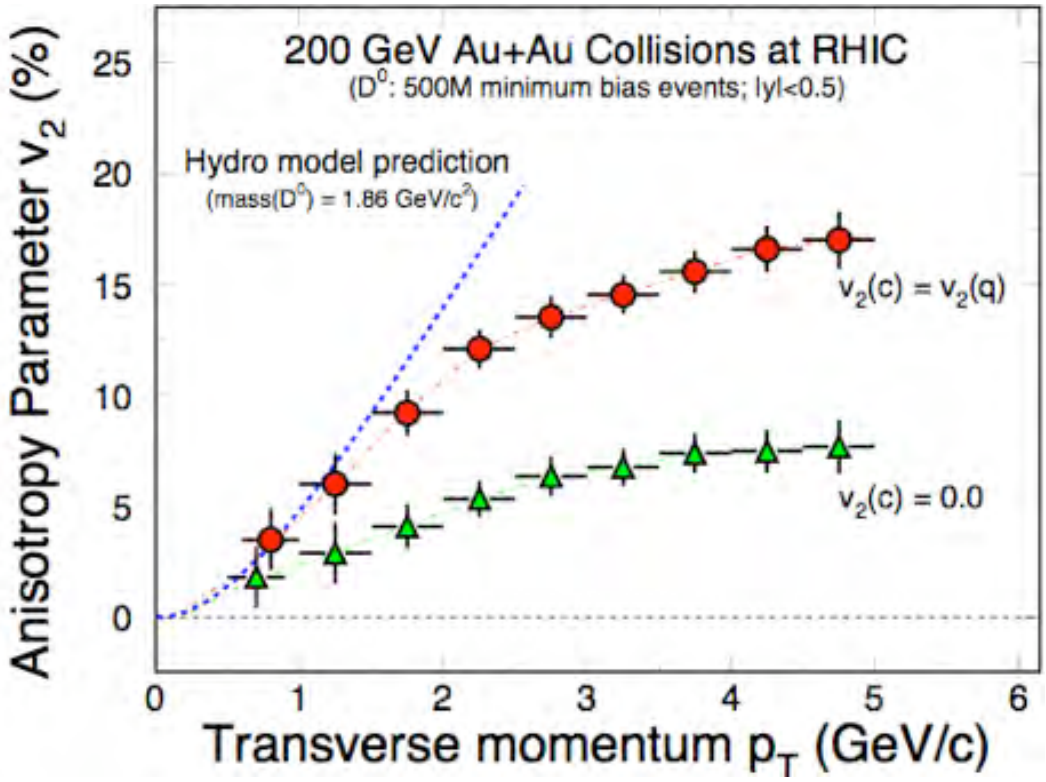


Figure 1: v2 as a function of pT for the case of charm flow the same as light quark flow (red) and for the case where charm does not flow (green).

2.2. Heavy Quark Energy Loss

The discovery of a factor of 5 suppression of high p_T hadrons ($5 < p_T < 10$ GeV/c) produced in Au+Au collisions at RHIC and the disappearance of the away-side jet has been interpreted as evidence for jet quenching.[2,3] This effect was predicted to occur due to radiative energy loss of high energy partons that propagate through a dense and strongly interacting medium.[4] The energy loss of heavy quarksFigure 2 is predicted to be significantly less compared to light quarks because of a suppression of gluon radiation at angles $\Theta < M_Q/E$, where M_Q is the heavy quark mass and E is the heavy quark energy. This kinematic effect is known as the "dead cone" effect. The suppression of small angle radiation has the advantage that the heavy quark fragmentation function and the spectrum of light particles produced in association with the heavy quarks can be calculated perturbatively.

Figure 2 shows the precision for RCP that can be achieved with 500 M minimum bias events in STAR with the HFT under the assumption that the suppression for heavy quarks is of the same size as the suppression for the light quarks.

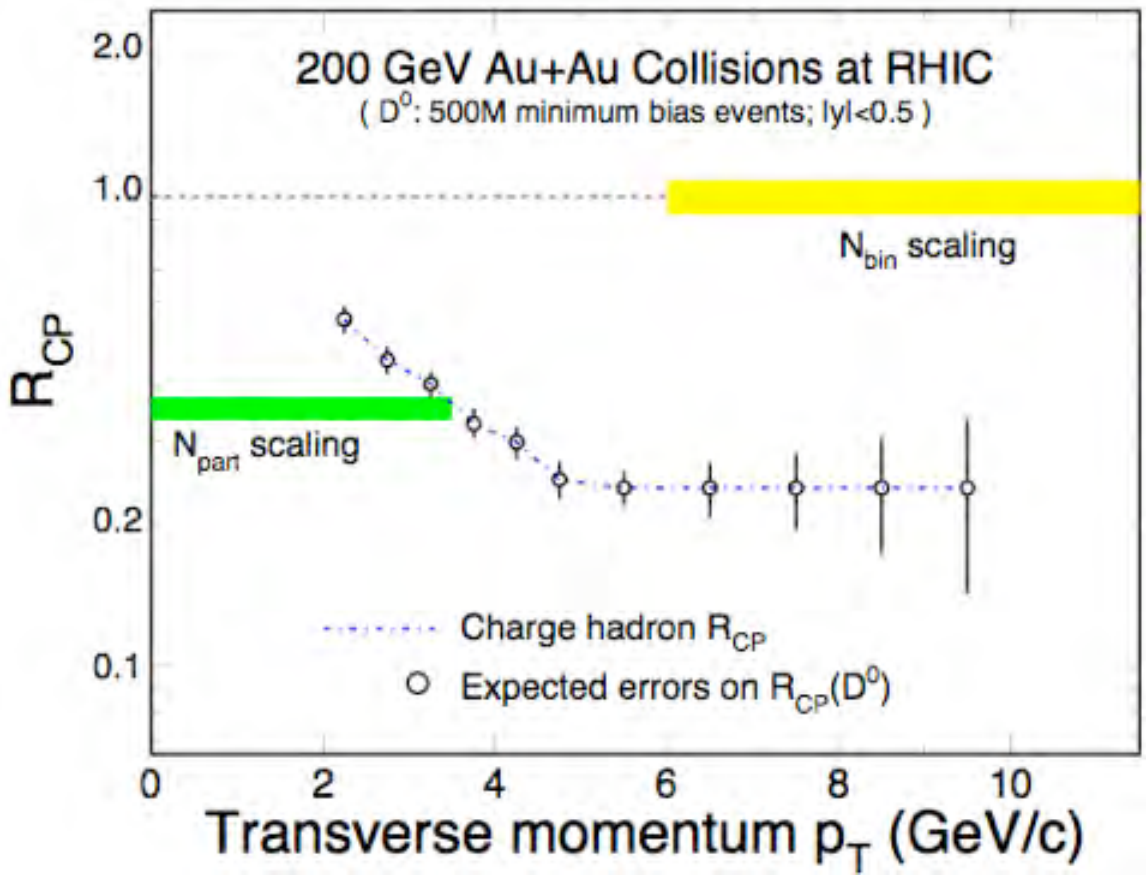


Figure 2: R_{AA} as a function of p_T.

2.3. A Baryon with a Charm Quark

In central Au+Au collisions at RHIC, a baryon to meson enhancement has been observed in the intermediate p_T region ($2 < p_T < 6$ GeV/c).[5,6] These results are usually explained by a hadronization mechanism involving collective multi-parton coalescence rather than independent vacuum fragmentation. The success of the coalescence approach implies deconfinement and possibly thermalization of the light quarks prior to hadronization.

Since Λ_c is the lightest charmed baryon, and its mass is not far from that of D^0 meson, a similar pattern of baryon/meson enhancement is expected in the charm sector[7] Therefore it would be very interesting to measure R_{CP} of Λ_c baryon and compare it to R_{CP} of D^0 meson. In addition, Λ_c/D^0 enhancement would be a possible explanation[8] of the large suppression of high- p_T electrons from charm and beauty decays.[9]

The feasibility of a Λ_c measurement with the Heavy Flavor Tracker will be discussed.

2.3.1. Measurement Method

Λ_c baryons can be reconstructed through their hadronic p-K^--π^+ decay channel (B.R. 5.0 %), despite its very short decay length $c\tau$ = 59.9 μm, by using topological cuts: primary track rejection based on Distance of Closest Approach to event Primary Vertex (DCA_PV), well reconstructed Λ_C decay vertex (daughter tracks intersect within ~2 sigma cut), Λ_C momentum pointing back to the primary vertex.

A possibility of using a resonant intermediate Λ(1520) state has been investigated, and an improvement of S/B ratio by factor ~10 could be expected. However, a full simulation hasn't been performed, and results shown hereafter are for non-resonant decay.

2.3.2. Simulation procedure

Central (b = 0-3 fm) Au+Au HIJING events ($\sqrt{s_{NN}}$ = 200 GeV) have been used to estimate combinatorial background, 18000 events total have been simulated. Into each event, 10 Λ_C have been inserted with a flat p_T spectrum shape to enhance statistics at high p_T, requiring them to decay through p-K^--π^+ decay channel. To facilitate the acceptance of HFT detector, events were simulated with vertex Z position in +- 5cm from detector center. Detector geometry used for these simulations is described in detail in.[10]

Rescaling to the physics case assumed power-law shape of Λ_C p_T spectrum, with $\langle p_T \rangle$ = 1.0 GeV/c, and n = 11. The yield estimate (for no Λ_C/D^0 enhancement) assumed Λ_C/D^0 ratio 0.2.[7] Given the overall uncertainty of c-cbar cross-section at RHIC, D^0 dN/dy = 0.002 per binary collision has been used, which is half of the value measured by the STAR Collaboration.[11]

At RHIC-II luminosity, PIXEL detector will integrate over ~12 minimum bias collisions. For realistic estimate of this pile-up effect, pseudo-random hits were added to PIXEL detector layers, corresponding to minimum bias interaction rate 80 kHz and Gaussian primary vertex z-distribution with σ_z = 15 cm. This is the upper estimate of pile-up hit densities when running at RHIC-II luminosity - very likely, interaction rate will be smaller and primary vertex σ_z bigger.

To estimate Λ_C signal and background in peripheral collisions, N_{bin} scaling with R_{CP} similar to that of charged hadrons[12] was assumed for Λ_C signal and $(N_{part})^3$ scaling assumed for background (3-particle combinations). For particle identification (PID) of Λ_C daughter tracks, the new STAR Time of Flight (TOF)[13] performance was estimated to separate pion – kaon for p_T < 1.6 GeV/c and proton – (pion+kaon) for p_T < 3.0 GeV/c with 90% efficiency.

Λ_C analysis relies on untriggered data set, as there are no obvious signs one could trigger on (i.e., photons or leptons). Therefore, large datasets of minimum bias and/or central events are needed. With DAQ1000 upgrade, STAR data acquisition will be able to reach over 500 events/s sustained DAQ rate. Given this rate and estimated 40% accelerator+detector duty factor, the number of events recorded per month running is ~ 500M. The results in the next section are for statistics of 500M central and 500M

peripheral events. This makes this measurement a goal for the 3rd year of HFT detector operation.

2.3.3. Results

In order to obtain a signal with high significance, very good pointing resolution is needed, and Λ_C decay daughter tracks have to be reconstructed with high efficiency. The combined acceptance + tracking efficiency is shown in Figure 1, for D^0 (red) and Λ_C (blue) in pseudorapidity $|\eta|<1$, requiring daughter tracks to be reconstructed and have good hits (i.e., not pile-up hits) in the PIXEL detector. Obviously, efficiency to reconstruct Λ_C is lower due to its three-body decay (i.e., three instead of two tracks, with lower p_T). Because of large combinatorial background, PID information was required for Λ_C decay daughter tracks, limiting the detector acceptance (magenta points in Figure 3).

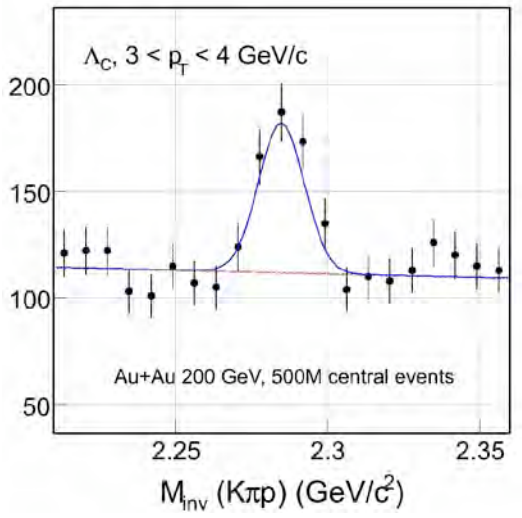


Figure 3: Acceptance+efficiency of ΛC and D0 reconstruction.

Topological cut optimization procedure was performed for both central (0-10%) and peripheral (60-80%) collisions, to maximize signal significance ($S/\sqrt{(S+B)}$). The results are shown in Table 1 and Table 2, estimated invariant mass peak for 3-4 GeV/c p_T bin is shown in Figure 4. A 3-sigma signal hasn't been achieved for $p_T < 2$ GeV/c. For $p_T > 5$ GeV/c, a good significance could be achieved without requiring daughter track PID information, however this hasn't been studied in detail.

p_T [GeV/c]	S/ð(S+B)	S/(S+B)	Λ_C produced	Λ_C reconstructed
2-3	4	0.03	23M	507
3-4	8	0.3	7.3M	184
4-5	14	0.9	2.4M	203

Table 1: Signal significance, purity and number of produced and reconstructed Λ_C in 500M central Au+Au collisions (for no Λ_C/D^0 enhancement). Decay branching ratio, acceptance, efficiency and topological cuts are taken into account.

p_T [GeV/c]	S/ð(S+B)	S/(S+B)	Λ_C produced	Λ_C reconstructed
2-3	5	0.9	940k	26
3-4	6	0.9	410k	40
4-5	6	0.9	180k	35

Table 2: Same as table 1, for 500M peripheral Au+Au collisions

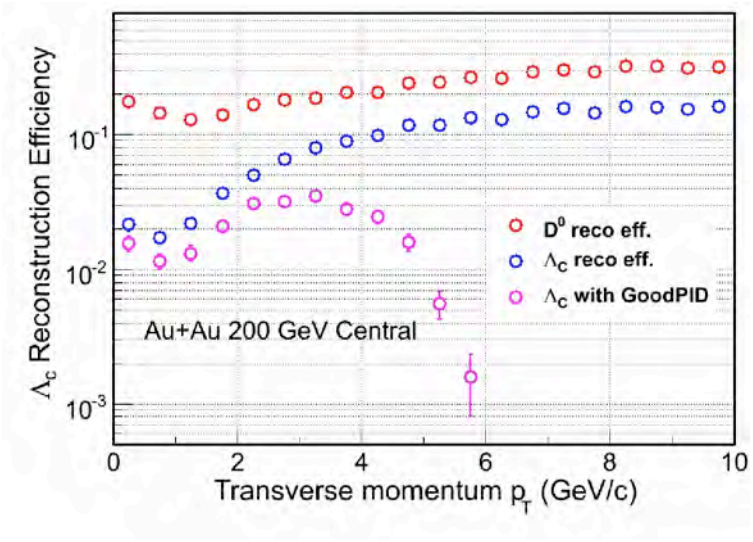


Figure 4: Estimated invariant mass peak for in p_T 3-4 GeV/c, in 500M central Au+Au collisions.

To estimate errors of Λ_C/D^0 measurement, two scenarios have been used: 1. no enhancement, ratio equal to 0.2 and flat in p_T, 2. The same enhancement as Λ/K^0_S [2]. Given D^0 much larger yield and cτ, errors coming from its measurement are negligible. Statistical errors on $R_{CP}(\Lambda_C)/R_{CP}(D^0)$ are shown in Figure 5. Note, that for the case of enhanced Λ_C yield, these errors are dominated by measurement in peripheral collisions.

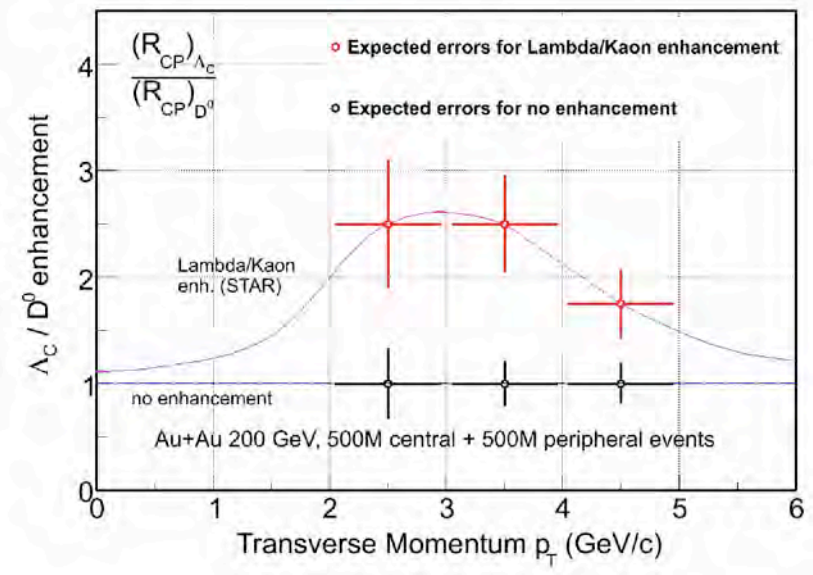


Figure 5: Statistical errors of Λ_C/D^0 ratio measurement for the case of no enhancement, and Λ/K^0_S-like enhancement.

2.3.4. Summary

Feasibility of Λ_C reconstruction with HFT has been shown using a full simulation of detector, with STAR reconstruction/tracking software. Measurement of Λ_C/D^0 ratio will allow us to distinguish between extreme enhancement scenarios, although this measurement is limited by statistics in peripheral collisions. Increased efficiency is expected, due to improved detector design [13] and due to possibly lower pile-up hit densities in RHIC-II luminosity, to be fully simulated in the future. Using resonant decay modes could also lead to better signal significance. These improvements will result in smaller errors on Λ_C/D^0 ratio measurement.

2.4. Mesons with a Bottom Quark

The bottom and charm quark are expected to behavior very differently in the QGP due to their large difference in mass[14]. The surprising observation of large suppression of high p_T non-photonic electron production has triggered a lot of developments on models involving dramatically different bottom charm meson production mechanism.[15,16,] Similarly, large non-photonic electron elliptic flow is observed in the low p_T region but there is the tendency of flow reduction at higher p_T possibly due to bottom quark contribution. Independent measurements on bottom quark production would be critical to disentangling different heavy meson production mechanisms and provide crucial information on the medium properties. On the other hand, measurement of bottom meson is important to clarifying the J/ψ production mechanism in the medium. Apart from the primordial production, a significant fraction of J/ψ comes from the B meson decay. Measurements on B meson production would allow us to subtract the contamination from the B-decay component.

With the current detector configuration, the B contribution to the non-photonic electron spectrum was estimated to be about 50% at pT > 5 GeV/c[17] with large uncertainties. With the HFT, the measurements will dramatically improve. Besides exclusive measurements with large luminosity, B mesons are usually measured using leptons and J/ψ particles through their semi-leptonic decay and J/ψ decay channels, respectively.

2.4.1. Measurement Methods

When measuring B mesons using leptons from their semi-leptonic decay, we utilize the impact parameter (d_0) method used by the ALICE collaboration[18] to separate electrons of B decays from those of D decays. Since B mesons have mean proper decay lengths of about 500 μm, their decay electrons are characterized by large impact parameters with respect to the interaction vertex. With the two pixel layers which instrument the innermost part of the HFT, the tracks' d_0 will be measured in STAR with a resolution σ_{d0} ~ 20 μm for $p_T \geq 2$ GeV/c. A cut imposing a minimum value of d_0 rejects a large fraction of the electrons from light meson decays and photon conversions, as well as primary pions misidentified as electrons. The charm contamination will be reduced with a p_T cut, as electrons of B decays have a harder p_T distribution than those of D decays due to the larger mass of the b quark. The UA1 Collaboration[19] has developed a Monte-Carlo method to extract the minimum- p_T -differential cross section at the B-meson level from the decay-electron p_T differential cross section, assuming the B-meson decay kinematics is well understood.

When measuring B meson through their decay J/ψ, we utilized the method developed by CDF[20] to calculate the pseudo-cτ of J/ψ and apply a certain cut on it to distinguish direct and B-decay J/ψ. Figure 1 illustrates how different variables are defined. The pseudo-cτ is defined as $c\tau' = \vec{L} \cdot \frac{p_T^{\psi}}{|p_T^{\psi}|} \cdot \frac{M_{\psi}}{|p_T^{\psi}|}$, where $\vec{L}$ is the path length between the J/ψ production point and collision vertex, M_{ψ} is the J/ψ mass and p_T^{ψ} is the J/ψ p_T which is required to be larger than 1.25GeV/c. Additionally, we define DCA as the distance of closest approach between paired electrons. A DCA cut of 50 μm is applied since the simulation shows the DCA for electron pairs from J/ψ are mostly within this range. The pseudo-cτ is less than 15% smaller[21] than the actual B meson cτ. In this analysis, the only physical background considered is direct J/ψ including feed-down contribution from higher mass charmonium states. Charm continuum and Drell/Yan might have similar level of contribution (see later discussions). The background due to the random combination of electron pairs during the mass reconstruction is removed via subtracting the same sign electron pair when analyzing mass and pseudo-cτ distribution. The signals are $B^{\pm}/B^0$ mixture with a 1.094% branching ratio to decay to J/ψ.[22]

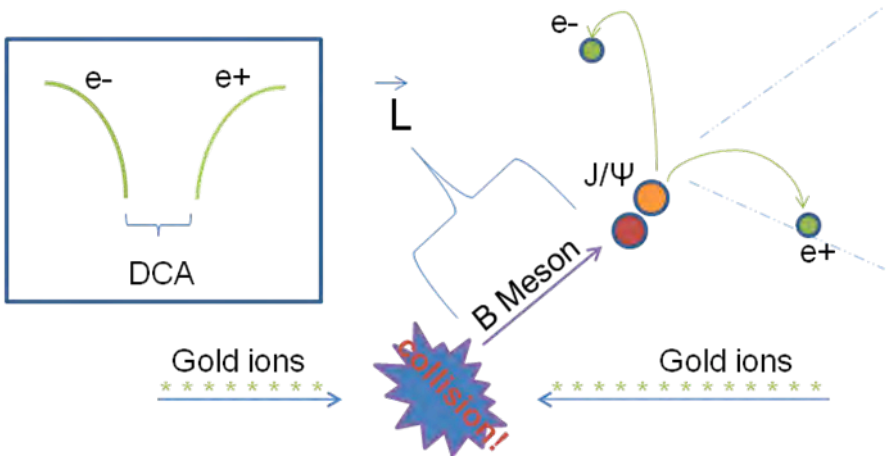


Figure 6: definition of variables used in the analysis. See text for details.

2.4.2. Simulation procedure

In the simulation of B meson semi-leptonic decays, we used the geometry described in the HFT CD0 proposal.[23] We first generated 3600 HIJING background events for central (b < 3 fm) Au+Au collisions at 200 GeV, with vertex Z between -5 and 5 cm for the best utilization of the pixel layers. Then for each event, we embedded 10 B^+ mesons which were forced to decay only into neutrino, positron and $\overline{D^0}$, and 10 D^+ mesons which were forced to decay only into neutrino, positron and $\overline{K^0}$. The B and D mesons were required to have a flat p_T distribution to enhance the statistics at high p_T , and p_T weights were applied later in the analysis to mimic the spectra in reality. The embedded events then went through the STAR data reconstruction chain to simulate the particle tracking by STAR detectors, and were stored into the standard data files for analysis.

In the simulation for B → J/ψ decay, we use the same geometry. PYTHIA is used to generate 353.5k direct J/ψ→ e^+e^- and 162.1k B → J/ψ→ e^+e^- decay in full phase space. Comparison of the acceptance of J/ψ with collision Z_{vertex} at the center of STAR and within ±5 cm shows little difference, we therefore fixed the collision vertex at the STAR center in most of the simulation for simplicity. These J/ψ are then embedded into most central Au+Au collisions generated from HIJING. 20 J/ψ are embedded into one single HIJING event to save computing time. Finally all the events are pushed through the STAR reconstruction chain to simulate realistic detector response. We also reconstructed a similar amount of direct and B-decay J/ψ in most central Au+Au collisions including PIXEL detector pile-up effects from expected RHIC-II luminosity.

2.4.3. Measurements through B semi-leptonic decay

We applied the p_T weights so that B/D spectrum and their relative contributions to non-photonic electrons follow the FONLL calculations[24], and the combined electron sample from B^+ and D^+ decays obeys the measured non-photonic electron spectrum for central

(0-5%) Au+Au collisions at 200 GeV.[25] The simulation input of the non-photonic electron p_T yields is shown in the left panel of Figure 7, normalized by the number of minimum bias events with vertex Z between -5 and 5 cm. The total tracking efficiency is about 55%, including both the TPC and the HFT pixel layers. Figure 8 presents the simulation results of the impact parameter distributions of electrons from B and D decays, for four p_T bins. Similar with the estimations in Ref. [17], the non-photonic electron sample is dominated by the D contribution for $2 < p_T < 3$ GeV/c, and the B contribution increases with p_T.

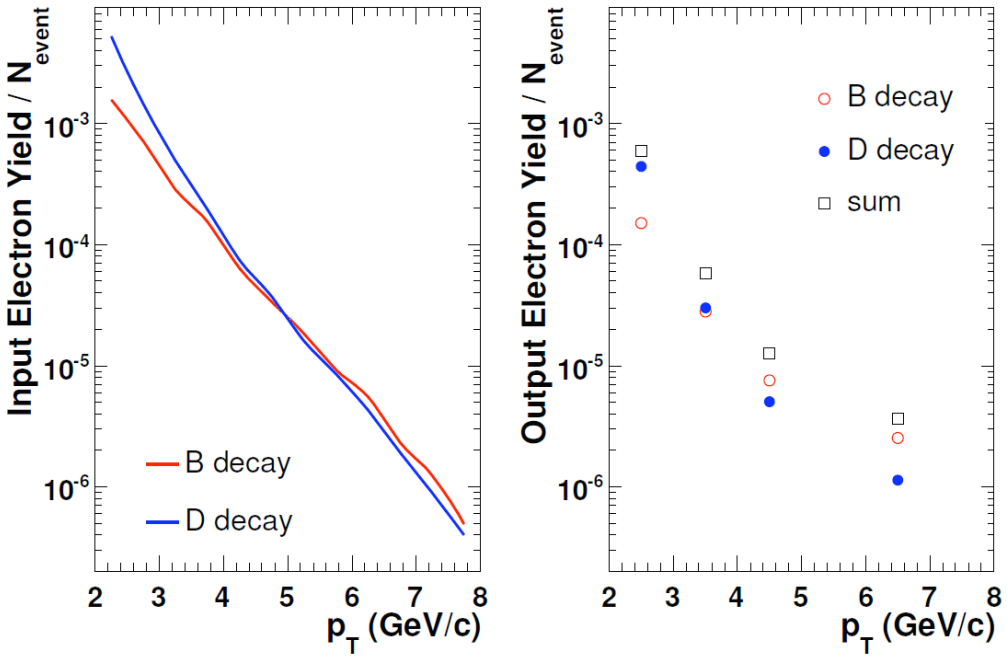


Figure 7: The simulation input (left panel) and output (right panel) of the non-photonic electron yields as a function of pT , normalized by the number of minimum bias events with vertex Z between -5 and 5 cm.

Above 4 GeV/c, there is a d_0 region (200−600 μm) where the B contribution is dominant. We selected electrons within this d_0 region to enhance the B contribution, and the electrons satisfying this condition were counted for each p_T bin, and the output is plotted in the right panel of Figure 7. The purities of the B-tagged electrons are 25%, 48%, 60% and 69% respectively, from low to high p_T bins, and the yields are 150, 28, 7.5 and 2.5 per million minimum bias central Au+Au events with vertex Z between -5 and 5 cm. The ALICE Coll. reported the purity of B-tagged electrons to be 80% for the collisions at LHC with the same method[26]. When we tried our approach with the FONLL B contribution [24] for LHC, we did see a purity of ~80% for $p_T > 4$ GeV/c. The purity obtained in this approach depends on the relative B/D contribution, which is an input yet to be measured. In the analysis of the real data, we first go through the above simulation procedures without applying the weight for the relative B/D contribution, and leave the simulated d_0 distributions un-normalized for electrons from B and D separately for each p_T bin. The measured d_0 distribution will then be fit with a parameterized combination of

the simulated d_0 distributions for electrons from B and D, and the relative B/D contribution will be retrieved as fitting parameters. With the relative B/D contribution measured, we can estimate the purity of B-tagged electrons for different DCA regions, and determine the optimal cuts for B reconstruction.

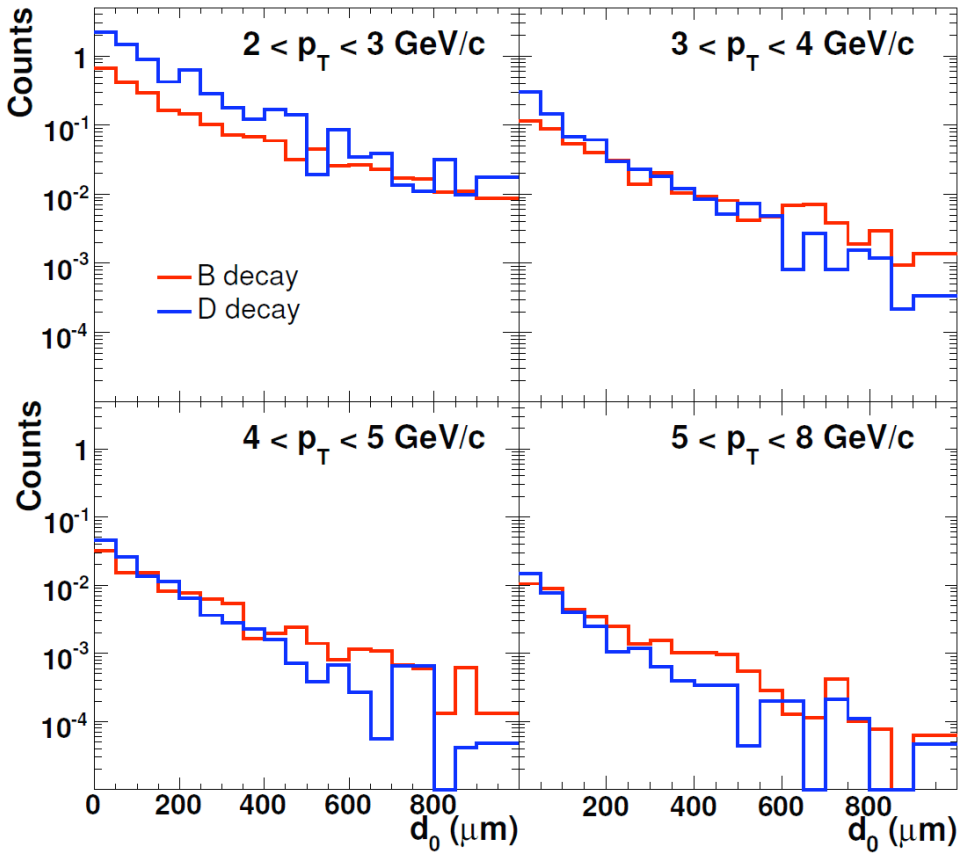


Figure 8: The simulation results of the impact parameter distributions of electrons from B and D decays.

We have estimated the feasibility of the impact parameter method for the proposed STAR HFT detector with the worst case: all the D-decay electrons come from D^+ mesons, whose decay length is ~300 μm. In reality, D^0 and D_s^0 mesons also decay into a substantial portion of D-decay electrons, and the corresponding decay length is only about 100 μm. In the future, we will consider the more realistic case, where the D-decay electrons in the d_0 region (200–600 μm) should be significantly suppressed, and hence, the purity of B-tagged electrons should increase. The yield of B-tagged electrons above 4 GeV/c is 10 per million minimum bias central Au+Au events with vertex Z between -5 and 5 cm. This number was obtained with the assumption of a 100% efficiency of the electron identification, which could be only 10% in reality, depending on the detectors involved and the identification approach. However, we can enhance the statistics of high-p_T electrons by applying high-tower triggers using STAR BEMC. When triggering on the track's minimum energy deposition in the BEMC tower, we can almost guarantee one

high-p_T electron per event. The electron yield above 4 GeV/c could be enhanced by a factor of 5000. All the discussions above are focusing on Au+Au collisions.

2.4.4. Measurements through B→J/psi+X decay

The goal of this analysis is to obtain the S/B ratio and efficiency as a function of pseudo-$c\tau$ cut in most central Au+Au collisions with and without the addition of PIXEL detector pile-up effect in RHIC-II luminosity.

In the analysis, the J/ψ signal is obtained by subtracting like-sign electron pairs mass spectrum from the unlike-sign electron pair spectrum within a mass window between 2.8GeV/c^2 and 3.2GeV/c^2. Figure 9 shows the mass distribution for unlike-sign and like-sign pairs in a single p+p and Au+Au collision where perfect electron identification is assumed. One can see the like-sign mass spectrum represents the combinatory background very well. The track quality cuts requires N_{fit}>20 and N_{fit}/N_{max}> 0.5, where N_{fit} and N_{max} are the number of fit points and maximum number of possible registered points for the reconstructed track.

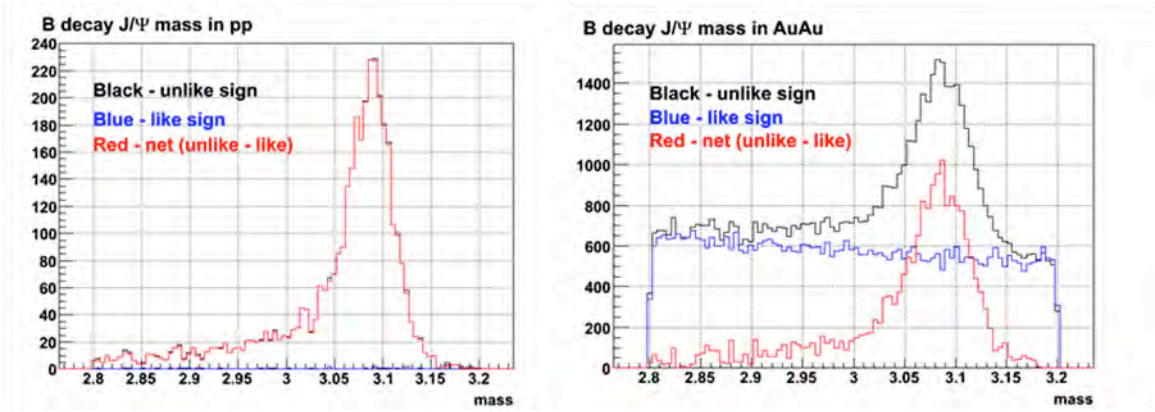


Figure 9: J/ψ mass distribution in single p+p collision and central Au+Au collisions. Black and blue histograms represent unlike, like-sign electron pairs, respectively; Red histogram is obtained after subtracting like-sign spectrum from unlike-sign spectrum. Note that 20 J/ψ–>ee are embedded into one Au+Au collision, therefore the S/B in the mass distribution does not reflect the actual value in real data.

Figure 10 shows the J/ψ pseudo-$c\tau$ distribution in most central Au+Au collisions where the left panel is for B → J/ψ and the right panel is for direct J/ψ. The black and red histograms are the results from unlike-sign and like-sign pairs, respectively. The red histogram is obtained after subtracting the like-sign pairs from the unlike-sign pair distribution. If the technique works well, the like-sign pairs should represent the combinatory background and the red histogram should be the pseudo-$c\tau$ distribution for B-decay J/ψ. We confirmed this by comparing the result with the one from tagged B-decay J/ψ which showed consistent results. Since direct J/ψ originates from the collision vertex, its pseudo-$c\tau$ distribution is expected to be a narrow Gaussian peak centering at zero with the width determined by the tracking resolution. In Figure 10 one can see that beside the expected Gaussian peaks, there are additional tails on both positive and

negative sides that are most likely coming from the wrong association of reconstructed track and PIXEL hits. As we will show later, similar tails are seen in CDF measurements. The B-decay J/ψ distribution contains a long tail in the positive pseudo-cτ due to the long B meson life time, a sharp Gaussian tail on the negative region due to tracking resolution and a tail due to the wrong association of tracks and PIXEL hits as in the case of direct J/ψ.

Figure 11 shows the pseudo-cτ distribution for B-decay and direct J/ψ in most central Au+Au collisions with and without PIXEL pile-up effects. We used the normalization from p+p collisions. The FONLL calculation [24] predicts the total $b\bar{b}$ cross section in p+p collisions at RHIC is 1.87 μb which leads to 3.74 μb for B meson production. Measurements from PHENIX run2005 p+p collisions show that the total direct J/ψ → e^+e^- production is about 178 nb. Taking into account the B → J/ψ → e^+e^- branching ratio, we obtained the yield ratio of direct J/ψ over B-decay J/ψ is about 65. The results show that the tail from the track and PIXEL hits misassociation is the major background for measuring B mesons. This background becomes larger when pile-up effects are added. This is demonstrated more clearly in the change of the S/B ratio before and after adding the pile-up effects.

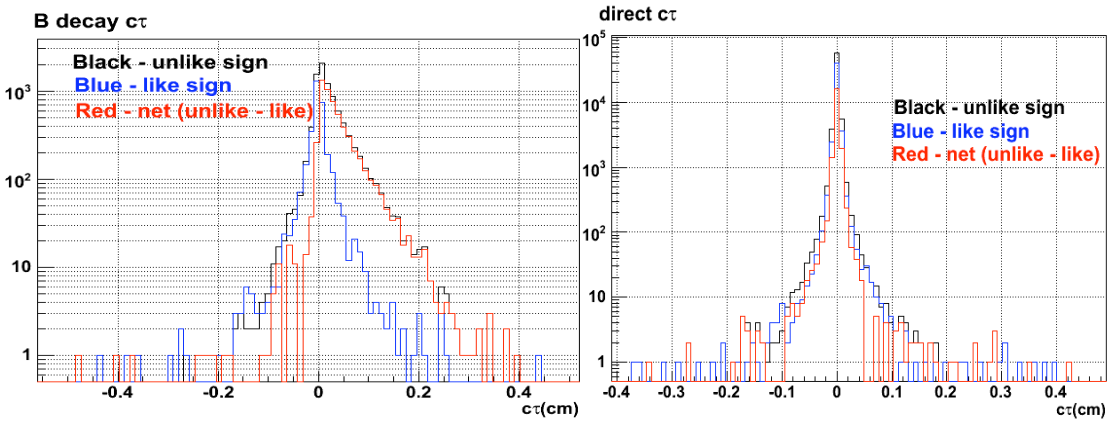


Figure 10: pseudo-ct distribution for the B-decay J/ψ (left panel) and direct J/ψ (right panel). See text for details.

Figure 12 shows the S/B ratio and efficiency in measuring B meson as a function of cut on pseudo-cτ. One can see that the pile-up effects increase when the cut increases. This is because the pileup hits on PIXEL detector enhance the probability of track and PIXEL hit misassociation which is the source for the non-Gaussian tail in the pseudo-cτ distribution. The results shows that the S/B ratio reach maximum of 1~2 at a pseudo-cτ cut at 500 μm where the efficiency for B-decay J/ψ is about 30%. Notice that these results do not include any nuclear or QGP effects for J/ψ and B meson production. As we know from the PHENIX run2004 measurement,[27] J/ψ production at mid-rapidity is suppressed by a factor of three in most central Au+Au collisions. If B meson is much less suppressed, the S/B ratio can increase significantly. In the real data analysis, one way to measure the B → J/ψ yield is to obtain, for example, the background p_T shape by

applying a very small pseudo-cτcut. After that one we apply a large cut to obtain the B-decay J/ψ p_T shape using the background shape as a reference.

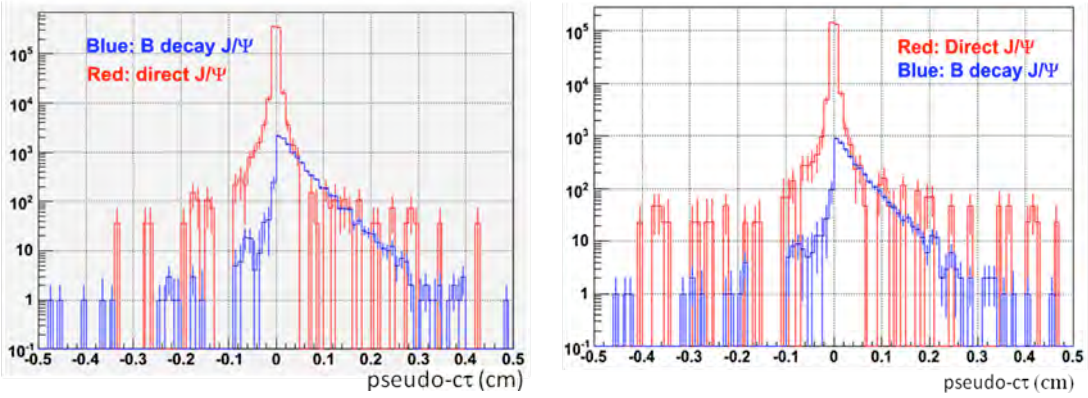


Figure 11: Pseudo-cτ distribution for direct and B-decay J/ψ in more central Au+Au collisions before (left panel) and after (right panel) including PIXEL detector pile-up effect in 1× RHIC-II luminosity. The red and blue histograms are from direct and B-decay J/ψ, respectively.

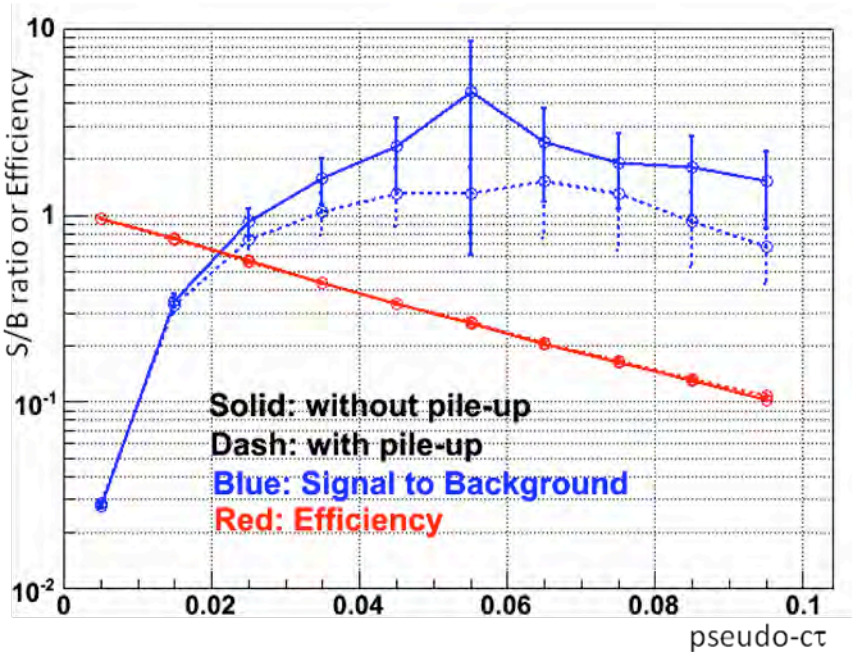


Figure 12: S/B ratio and efficiency as a function of pseudo-ct cut for B → J/ψ measurements in most central Au+Au collisions. The dashed curves represent result including PIXEL pile-up effect in 1× RHIC-II luminosity. The red curves are efficiency and blue curves are S/B ratio. The error bars are statistical errors only.

We then studied the effect of PIXEL detector position resolution on the measurements. Figure 13 presents the results when PIXEL detector resolution is changed from 8 μm to 80 μm without including the pile-up effect. We changed the electron pair DCA cut from 50 μm to 200 μm to keep the efficiency unchanged. Left panel shows pseudo-cτ distribution for direct and B-decay J/ψ. Compared to the results in the left

panel of Figure 11, one can see the distribution for direct J/ψ become much wider due to the worse resolution while the effect on B-decay J/ψ is not that obvious due to the much larger B meson cτ. The widened direct J/ψ distribution leads to five to ten times smaller S/B which is shown in the right panel of the figure. Therefore the HFT PIXEL detector is unique in this measurement.

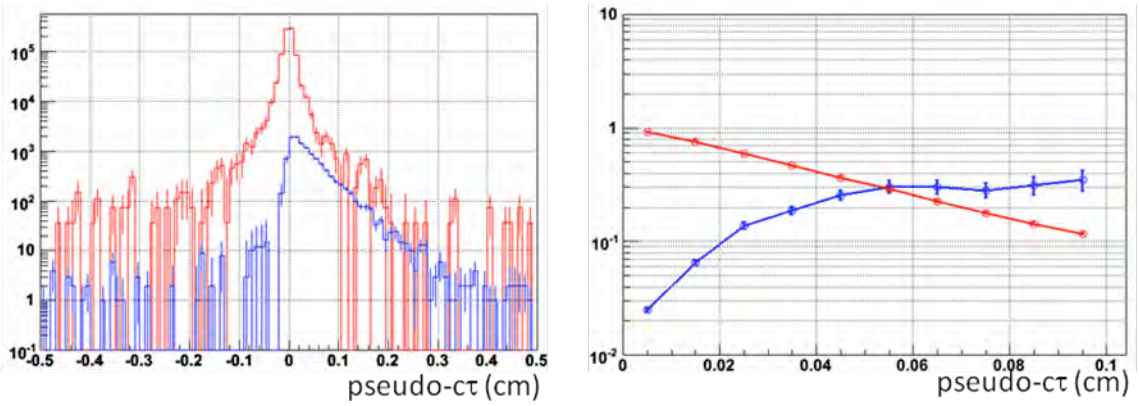


Figure 13: Results after changing the PIXEL detector position resolution from 8μm to 80μm; Left panel is pseudo-cτ distribution for direct J/ψ (red) and B-decay J/ψ (blue); right panel is the S/B (blue) and efficiency (red) as a function of pseudo-cτ cut.

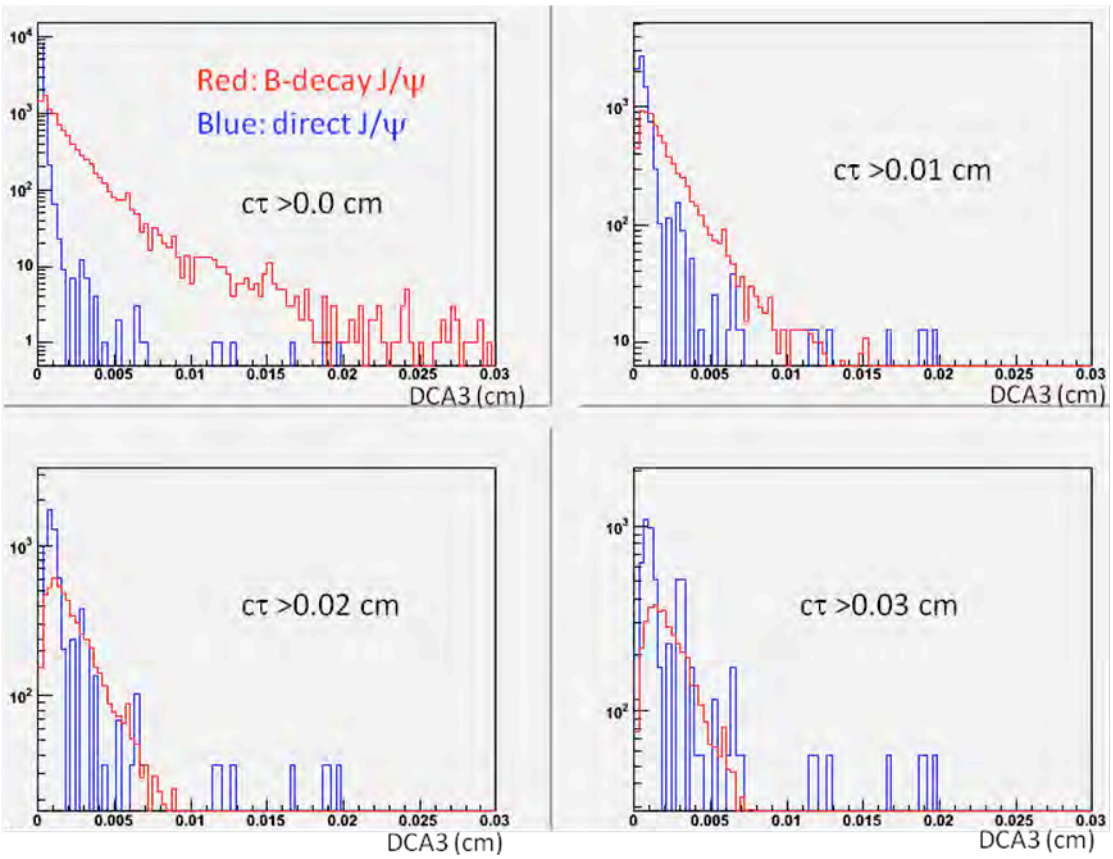


Figure 14: Distribution of the minimum distance of closest approach between a third charged particle to the reconstructed production point of J/ψ under different pseudo-cτ cut. Red histogram is for B-decay J/ψ and blue histogram is for direct J/ψ.

One possible way to improve the S/B is by applying the cut on the distance of closest approach on a third charged particle (DCA3) to the reconstructed J/ψ production point. A large fraction of 'X' particles from B → J/ψ+ X are charged. In large cτ region, ideally after applying a small DCA3 cut, namely DCA3 < cut, most of the direct J/ψ which come from collision point were expected to be rejected while a large fraction of B-decay J/ψ should be kept. It turns out that the small DCA3 cut can't improve the S/B ratio. Figure 14 shows the DCA3 distribution under different pseudo-cτ cut. When no pseudo-ct cut is applied, the direct J/ψ DCA3 distribution is much narrower than the B-decay J/ψ since at collision vertex there are thousands of charged particles can be used as a third particle to reconstruct DCA3 and it is very likely for a randomly associated third particle to be closer than the reconstructed position of the actual third partner. When the pseudo-cτ cut is larger, this probability becomes smaller and the distribution becomes wider. In large ct region, as shown in the figure, the results for direct and B-decay J/ψ become very similar, therefore cutting on DCA3 can't improve the S/B ratio. However, based on Figure 14, applying a large DCA3 cut, for example DCA3 > 20 μm will enhance the S/B especially when small pseudo-cτcut is applied. Figure 15 shows the result after this cut without including the PIXEL detector RHIC-II pile-up effect. One can see that the DCA3 cut

dramatically improved the S/B ratio in the small pseudo-cτ cut region but have little effect in the large pseudo-cτ cut region. In the mean time, the B-decay J/ψ suffers significant efficiency loss. Therefore, the analyses with and without DCA3 cut can be used to cross check each other to understand systematic uncertainties.

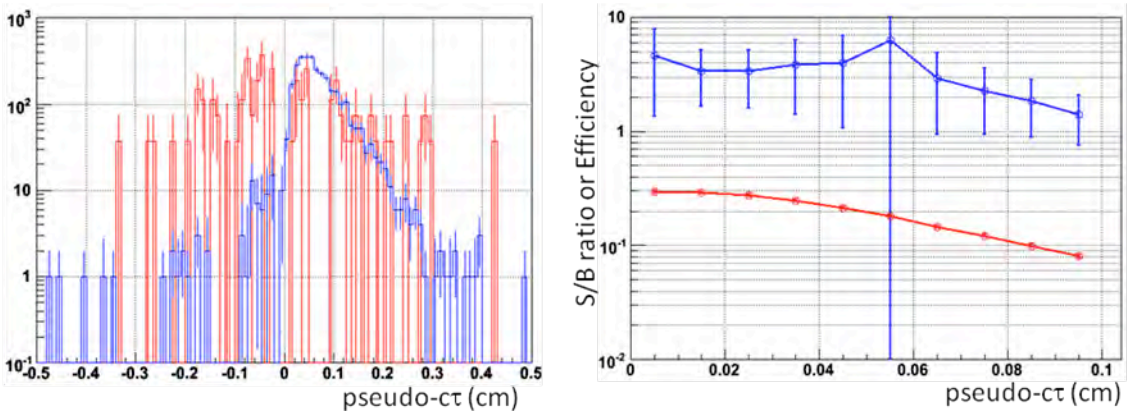


Figure 15: Results after applying the DCA3 cut; Left panel is pseudo-cτ distribution for direct J/ψ (red) and B-decay J/ψ (blue); right panel is the S/B (blue) and efficiency (red) as a function of pseudo-cτ cut.

We also did a consistency check between our results and CDF measurements. Figure 16 shows CDF measurements on B → J/ψ. The left panel presents the breakdown of pseudo-cτ distribution for different components in RUN-I where only high p_T J/ψ (p_T > 5GeV) are measured. One can see the shape for direct and B-decay J/ψ are similar to what we observed including the tail represented by an exponential curve due to the misassociation of tracks and their silicon detector hits. One can estimate from the figure that without including the "background", the S/B ratio is about 10 compared to about 2 at RHIC. The right panel shows that the relative yield of direct J/ψ over B-decay J/ψ is about 15 compared to 65 at RHIC. Assuming the CDF detector and the STAR detector have similar performance in measuring B → J/ψ, these two results are consistent with each other. The "background" indicated in the figure comes from the continuum and Drell/Yan which is about 10% of direct J/ψ in terms of production yield judging from the figure. However, they produce comparable tails in the large pseudo-cτ region to those from direct J/ψ. The inclusive p_T J/ψ measurements from PHENIX indicate a similar relative yield of charm continuum and Drell/Yan over direct J/ψ. We therefore can expect they have similar level of contribution as direct J/ψ in the large pseudo-cτ region at RHIC.

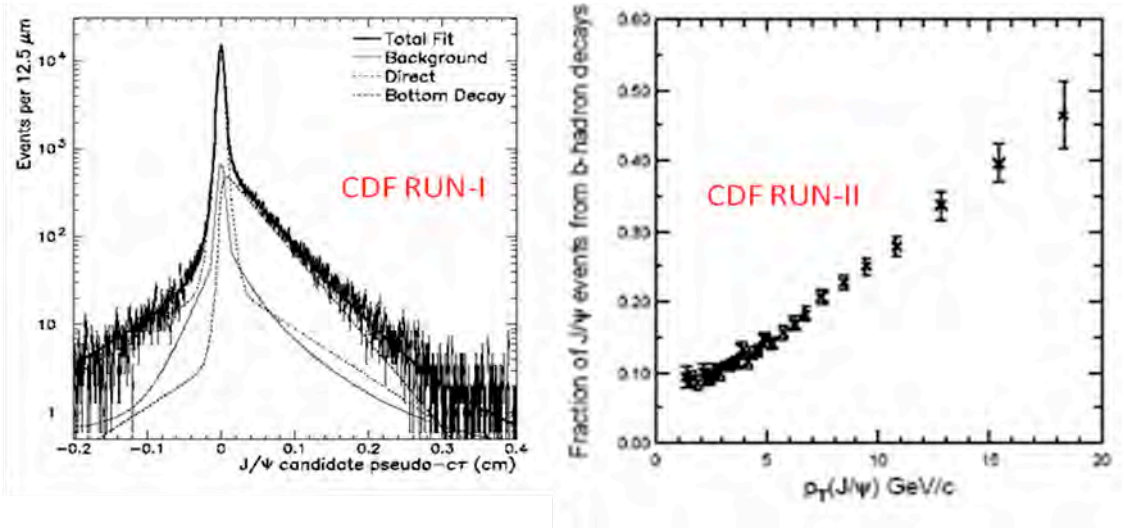


Figure 16: CDF measurements on B→J/ψ decay. Left panel shows the pseudo-cτ distribution in RUN-I with breakdown of different source of contribution; right panel shows the ratio of B-decay J/ψ over the direct J/ψ in RUN-II.

The number of B-decay J/ψ recorded in STAR during each RHIC-II week without including the trigger efficiency is:

$$N(B \to J/\psi) = \sigma(B) \cdot BR(B \to J/\psi) \cdot BR(J/\psi \to e^+e^-) \cdot AccpEff(recon) \cdot eff(p_T\ cut) \cdot eff(c\tau\ cut) \cdot eff(analysis\ cut) \cdot dutyFactor \cdot luminosity(RHIC - II)$$

, where $\sigma(B)$ is the B meson cross section; $BR(B \to J/\psi)$ and $BR(J/\psi \to e^+e^-)$ are branching ratio for each of the decay channels; $AccpEff(recon)$ is the product of J/ψ acceptance and reconstruction efficiency in full phase space; $eff(p_T\ cut)$ is the efficiency due to the p_T >1.25GeV cut; $eff(c\tau\ cut)$ is the efficiency due to pseudo-cτ cut; $eff(analysis\ cut)$ is the efficiency for all the analysis cut including track quality, electron pair DCA and J/ψ mass window, etc; $dutyFactor$ is the expected STAR duty factor during the run; $luminosity(RHIC - II)$ is the expected delivered luminosity in a 12-week RHIC-II run in 2013.[28] The value for each of above variable is listed in the following table:

Variables	Single p+p collision	Au+Au collisions
$\sigma(B)$	3.7 μb	0.14b (assuming binary scaling)
$BR(B \rightarrow J/\psi)$	1.094%	1.094%
$BR(J/\psi \rightarrow e^+e^-)$	5.94%	5.94%
$AccpEff(recon)$ |collision Zvtx| <5cm	17.4% (direct J/ψ), 19.4% (B→J/ψ).	12.2% (direct J/ψ.)[a] 13.6% (B→J/ψ)[a]
$AccpEff(recon)$ without collision Zvtx cut .30 cm diamond Zvtx	3.1% (direct J/ψ) 3.5% (B→J/ψ)[b]	2.2% (direct J/ψ)[b] 2.5% (B→J/ψ)[b]
$eff(p_T\ cut)$	76.0%	76.0%
$eff(c\tau\ cut)$	30%	30%
$eff(analysis\ cut)$	59%	59%
$dutyFactor$	70%	70%
$luminosity\ (RHIC-II)$ Maximum per 12 weeks Minimum per 12 weeks	 360pb^{-1} 46pb^{-1}	 19nb^{-1} 3.3nb^{-1}

a: Loss of efficiency compared to that in a single p+p collision due to high multiplicity.

b:Only the efficiency for direct J/y is from the simulation. All the tagged number are derived from the relative ratio calculated in AccpEff(reco) with 5cm Z vertex cut.

The total number of B → J/ψ → e^+e^- per RHIC-II 12-week run recorded at STAR *assuming 100% trigger efficiency* and neglecting TPC pile-up effect in high collision rates:

- In p+p collisions,
  - Maximum: 2858±93 J/ψ at $p_T \geq 1.25$GeV/c
  - Minimum: 365±33 J/ψ at $p_T \geq 1.25$GeV/c
- In Au+Au collisions
  - Maximum: 4066±110 J/ψ at $p_T \geq 1.25$GeV/c
  - Minimum: 706±46 J/ψ at $p_T \geq 1.25$GeV/c

Based on these numbers, we then calculated the number of J/ψ recorded at |Z vertex|<5cm by multiplying the efficiency (13.2%) of the vertex cut estimated from a Gaussian distribution with σ=30cm and *assuming 100% trigger efficiency:*.

- In p+p collisions
  - Maximum: 2084±79 J/ψ at $p_T \geq 1.25$GeV/c.
  - Minimum: 266±28 J/ψ at $p_T \geq 1.25$GeV/c.
- In Au+Au collisions
  - Maximum: 2926±94 J/ψ at $p_T \geq 1.25$GeV/c
  - Minimum: 508±39 J/ψ at $p_T \geq 1.25$GeV/c.

Therefore, about 70% of the observed J/ψ are from $|Z_{vertex}|<5$cm due to the configuration of the PIXEL detector.

However, the J/ψ trigger performance in STAR will have to be significantly improved to make it possible to measure B → J/ψ. In p+p collisions, the current J/ψ trigger efficiency based on an estimate from the 2006 p+p run is only about 10% at $p_T(J/\psi) > 6$ GeV/c. If the trigger performance persist at RHIC-II, the maximum number of observed B → J/ψ → ee per 12-week run is ~2858*10%*3% = 9, where 3% is the fraction of J/ψ at $p_T >$ 6 GeV/c relative to the number of J/ψ at $p_T > 1.25$ GeV/c. This means B → J/ψ → ee channel cannot be used to measure B mesons without improved trigger. In Au+Au collisions, the expected collision rate is ~50 kHz. Considering the 1 kHz STAR DAQ bandwidth, we will also need a very good J/ψ trigger to carry on this measurement. With the TOF and DAQ1000 upgrade, the J/ψ trigger is expected to be significantly improved. New studies are needed to estimate the improvement. One the other hand, when the Muon Telescope Detector (MTD) upgrade is accomplished, we can study B meson using the B → J/ψ → $\mu^+\mu^-$ channel with a high performance MTD trigger with a very high rejection power.

3. Functional Requirements

3.1. General Design Considerations

STAR is a large acceptance experiment with full azimuthal coverage at mid-rapidity in the pseudo-rapidity range $|\eta| < 1$. With the TPC as a central detector and a current read-out speed of about 100 Hz STAR is considered to be a "slow" detector as far as single particle observables are concerned. Even after the DAQ upgrade to 1000 Hz in 2009 the read-out speed will be limiting the single particle capabilities of STAR. The real strength of STAR, good particle identification and full azimuthal coverage, come into play when correlations or multi-particle final states are studied. Good particle identification and full azimuthal coverage have been the bases for the enormous success of the STAR physics program.

It is obvious that when it comes to identifying rare processes, like heavy flavor production with multi-particle final states, full azimuthal coverage will be of utmost importance. Thus, full azimuthal coverage is a prime design requirement for the HFT.

Another important requirement is to keep a very low overall material budget in order to limit the effects of multiple scattering and of conversions. Our goal is to overall reduce the radiation length of the inner tracking and support system compared to the status when the SVT was the STAR inner tracking detector.

The performance requirements listed below are selected so that if those requirements are met by the detector, the detector will be able to achieve the physics requirements. Fulfillment of the performance requirements can be completely determined shortly after the installation of the HFT.

3.2. Pointing Resolution

Heavy flavor hadrons have extremely short life times ($c\tau \sim 50$ μm). Identifying such a short displaced vertex requires extremely good pointing resolution. This is especially important for the identification of low transverse momentum decays where small gains in pointing resolution lead to large gains in detection efficiency. (maybe we can add a graph of efficiency at 1 GeV as fuction of pointing resolution?). The efficiency of D^0 detection is given in Figure 17 as a function of p_T.

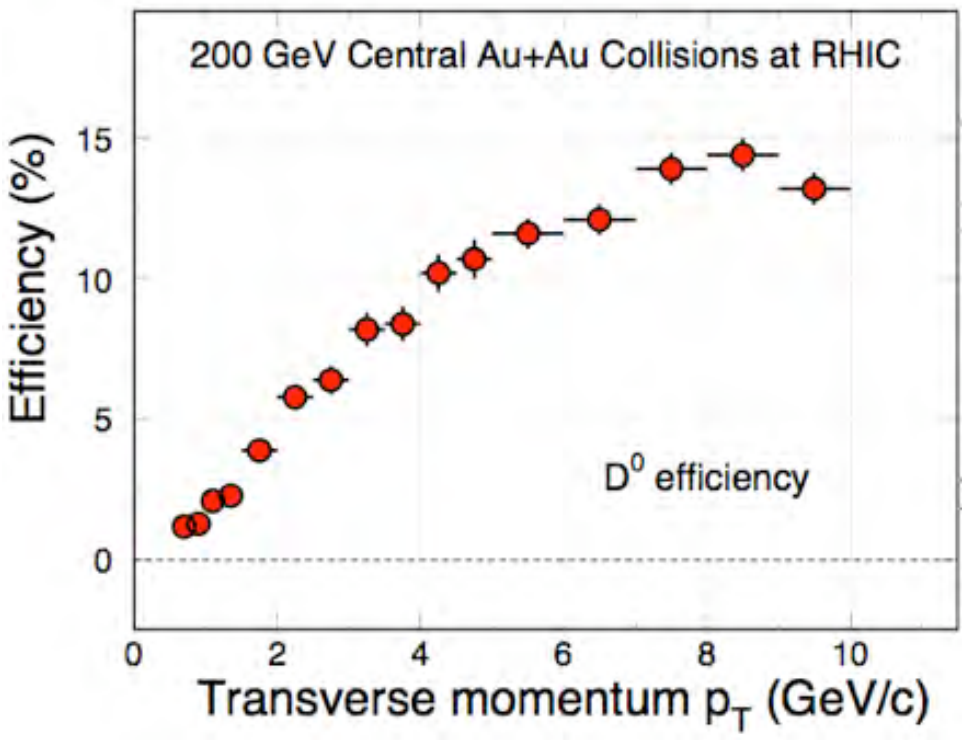


Figure 17: D^0 efficiency.

We require a pointing resolution of better than 50 μm for kaons of 750 MeV/c. 750 MeV/c is the mean momentum of the decay kaonskanos from D mesons of 1 GeV/c transverse momentum, the peak of the D meson distribution.

The pointing resolution that will be achieved by the HFT can be calculated from the design parameters.

3.3. Multiple Scattering in the inner Layers

The precision with which we can point to the interaction vertex is determined by the position resolution of the pixel detector layers and by the effects of multiple scattering in the material the particles have to traverse. The beam pipe and the first pixel layer are the two elements that have the most adverse effect on pointing resolution. Therefore, it is crucial to make those layers as thin as possible and to build them as close as possible to the interaction point.

We have chosen a radius of 2 cm for a new beam pipe. Making this radius even smaller would make the STAR beam pipe the limiting aperture of the RHIC ring. This is not a desirable situation. The central section of the beam pipe will be fabricated from Beryllium. Such a beam pipe can have a minimal wall thickness of xx μm, equivalent to 0.xx % of a radiation length.

The two pixel layers will be at a radius of 2.5 cm and 8 cm, respectively. The sensors will be thinned down to 50 μm and the ladders will be fabricated in ultra-light carbon

fibre technology. The total thickness of the beam pipe and the fist pixel layer will be the equivalent of 0.xx % of a radiation length. With those parameters, the contributions to the pointing resolution from multiple scattering and from detector resolution will be about equal.

The radiation lengths of the two innermost structures, the beam pipe and the first pixel layer, are design parameters.

3.4. Internal Alignment and Stability

The Pixel and the IST positions need to be known and need to be stable over a long time period in order not to have a negativean effect on the pointing resolution. The quality of the data will depend on alignment and long term stability. This is especially important for the Pixel detector that needs to be installed and removed on a short time scale.

The alignment and stability need to be better than 300 μm for the IST and better than 20 μm for the Pixel.

Those parameters can be determined from a survey.

3.5. Pixel Integration Time

Compared to the strip detectors, the Pixel is a slow device with a long integration time. All events that occur during the integration or life time of the Pixel will be recorded. This makes assigning Pixel hits to a particular track in the TPC a difficult pattern recognition problem.

From detailed simulations we have concluded that at RHIC II luminosities the detection and reconstruction efficiency for D-mesons is not appreciably degraded due to multiple events and tracks in the Pixel if the integration time of the detector is smaller than 200 μs.

The Pixel integration time is a design parameter.

3.6. Read-out Speed and Dead Time

In the absence of a good trigger for D-mesons it is imperative for the measurement of rare processes to record as many events as possible and as required by the physics processes. In STAR the speed of the DAQ is the limiting factor for the number of events recorded.

In order not to slow down the STAR DAQ, the HFT read-out speed needs to be compatible with the STAR DAQ speed and the HFT needs to be dead time free.

Read-out speed and dead time are design parameters.

3.7. Detector Hit Efficiency

The hit efficiency of the Pixel and IST detectors is essential for good detection efficiency. In the case of secondary decay reconstruction, the hit inefficiency of each detector layer enters with the power of the number of reconstructed decay particles into the total inefficiency.

In order to keep inefficiency low, we request that each individual detector layer has a hit efficiency of better than 95%.

The hit efficiency of each detector layer can be measured on the bench before installation.

3.8. Life Channels

Dead channels in the Pixel and IST will cause missing hits on tracks and thus lead to inefficiencies in the reconstruction of decay tracks. Therefore, the number of dead channels needs to be as low as possible.

The impact of dead channels on the overall performance will be minimal if more than 97% of all channels are alive at any time.

The number of dead channels can be determined immediately after installation of the detectors.

4. Technical Design

4.1. Overview

4.2. Pixel

4.2.1. Introduction

4.2.2. Detector Parameters

The relevant performance parameters for the Pixel detector are shown in Table 3.

Pointing resolution	(13 ⊕ 19GeV/p·c) μm
Layers	Layer 1 at 2.5 cm radius Layer 2 at 8 cm radius
Pixel size	18.4 μm × 18.4 μm
Hit resolution	10 μm rms
Position stability	6 μm (20 μm envelope)
Radiation thickness per layer	X/X0 = 0.28%
Number of pixels	436 M
Integration time (affects pileup)	0.2 ms
Radiation tolerance	300 kRad
Rapid installation and replacement to cover rad damage and other detector failure	Installation and reproducible positioning in a shift

Table 3: Performance parameters for the pixel detector.

4.2.3. Sensors and Readout

Development and Deployment Plan

We intend to approach the completion of the Pixel detector for STAR as a two stage development process with the readout system requirements tied to the stages of sensor development effort. The sensor development is taking place at the Institut Pluridisciplinaire Hubert Curien (IPHC) in Strasbourg, France where we are working in collaboration with Marc Winter's group. In the current development path, the first set of prototype sensors to be used at STAR will have digital outputs and a 640 μs integration time. We will use these sensor prototypes to construct a limited prototype detector system for deployment at the STAR detector during the summer of 2010. This prototype system will employ the mechanical design to be used for the final Pixel detector as well as a readout system that is designed to be a prototype for the expected final readout system to be deployed with the final Pixel sensors in a complete detector in the 2012 time frame.

Monolithic Active Pixel Sensor (MAPS) Development at IPHC

The sensor development path for the Pixel detector sensors is tailored to follow the development path of the technology as it was set by the IPHC group. In this path, MAPS sensors with multiplexed serial analog outputs in a rolling shutter configuration are envisioned as the first generation of sensors followed by a more advanced final or ultimate sensor that had a digital output(s). The analog MAPS have been produced and tested and our sensor development path moves to digital binary readout from MAPS with fine grained threshold discrimination, on chip correlated double sampling (CDS) and a fast serial LVDS readout. A diagram showing the current development path and with the attendant evolution of the processing and readout requirements is shown in Figure 18.

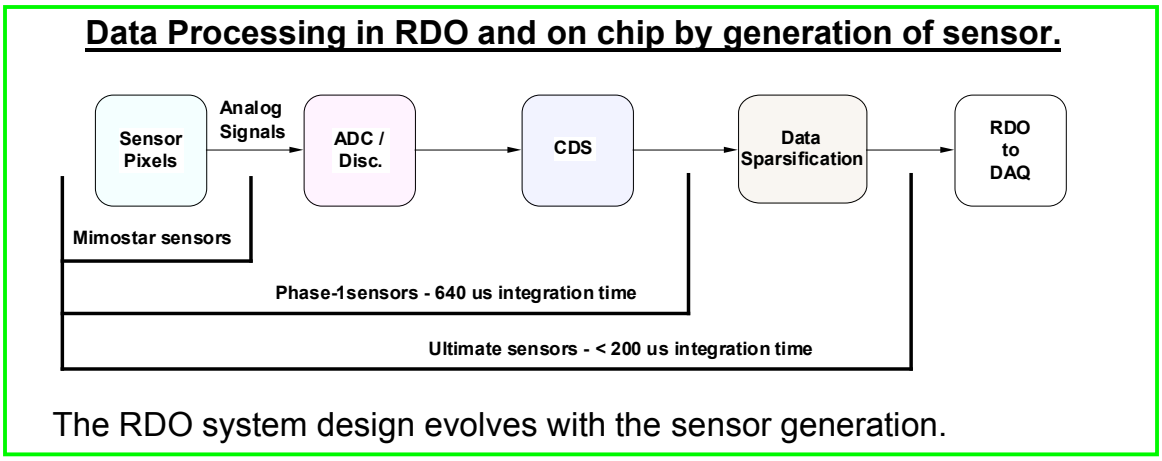


Figure 18: Diagram showing the sensor development path of sensors for the STAR Pixel detector at IPHC in Strasbourg, France. The readout data processing required is shown as a function of sensor generation. The first generation Mimostar sensors are read out via a rolling shutter type analog output. The next generation Phase-1 sensor integrates CDS and a column level discriminator to give a rolling shutter binary readout with a 640 μs integration time. The final generation Ultimate sensor integrates data sparsification and lowers the readout time to < 200 μs.

The Mimostar series sensors are the generation of sensors that have been fabricated and tested. These are 50 MHz multiplexed analog readout sensors with 30μm × 30μm pixels in variously sized arrays depending on generation. This generation has been tested and characterized and, with the exception of some yield issues, appears to be well understood. Testing with these sensors is well described in a NIM paper reference.

The next generation is named "Phase-1". This sensor will be based on the Mimosa-8 and Mimosa-16 sensors and will contain on-chip correlated double sampling and column level discriminators providing digital outputs in a rolling shutter configuration. The Phase-1 will be a full sized 640 × 640 array resulting in a full 2 cm × 2 cm sensor size. In order to achieve a 640 μs integration time, the Phase-1 sensor will be equipped with four LVDS outputs running at 160 MHz. The first delivery of wafers of this sensor design is expected in late 2008.

The final sensor is named "Ultimate". The Ultimate sensor includes all of the attributes of the Phase-1 sensor with the pixel sub-arrays clocked faster to give a <200 μs integration time and the integration of a run length encoding based data sparsification and zero suppression circuit. The pixel size has been reduced to 18.4 μm × 18.4 μm to increase the sensor radiation tolerance in the higher luminosity RHIC II environment. There are two data output lines from the sensor and the data rates are low thanks to the newly included data sparsification circuitry. The first prototypes of this design are expected to be delivered in the 2010 time frame.

Sensor Series Specifications

The specifications of the sensors under development are shown in Table 4.

	Phase -1	**Ultimate**
Pixel Size	30 μm × 30 μm	18.4 μm × 18.4 μm

Array size	640 × 640	1024 × 1088
Active area	~ 2 × 2 cm	~ 2 × 2 cm
Frame integration time	640 μs	100 – 200 μs
Noise after CDS	10 e-	10 e-
Readout time / sensor	640 μs	100 – 200 μs
Outputs / sensor	4	2
Operating mode	Column parallel readout with all pixels read out serially.	Column parallel readout with integrated serial data sparsification.
Output type	Digital binary pixel based on threshold crossing.	Digital addresses of hit pixels with run length encoding and zero suppression. Frame boundary marker is also included.

Table 4: Specifications of the Phase-1 and Ultimate sensors.

The Phase-1 is a fully functional design prototype for the Ultimate sensor which results in the Phase-1 and Ultimate sensors having very similar physical characteristics. After successful development and production of the Phase-1 sensors, a data sparsification system currently under development at IPHC will be integrated with the Phase-1 design. With the additional enhancement of design changes allowing for faster clocking of the sub-arrays, the resulting sensor is expected to be used in the final Pixel detector. In addition to the specifications listed above, both sensors will have the following additional characteristics;

- Marker for first pixel
- Register based test output pattern JTAG selectable for binary readout troubleshooting.
- JTAG selectable automated testing mode that provides for testing pixels in automatically incremented masked window to allow for testing within the overflow limits of the zero suppression system.
- Independent JTAG settable thresholds
- Radiation tolerant pixel design.
- Minimum of 3 fiducial marks / sensor for optical survey purposes.
- All bonding pads located along 1 side of sensor
- Two bonding pads per I/O of the sensor to facilitate probe testing before sensor mounting.

Architecture for the Phase-1 Sensor System

The requirements for the Phase-1 prototype and final readout systems are very similar. They include;

- Triggered detector system fitting into existing STAR infrastructure and to interface to the existing Trigger and DAQ systems.
- Deliver full frame events to STAR DAQ for event building at approximately the same rate as the TPC (~ 1 KHz for the STAR DAQ1K upgrade).
- Reduce the total data rate of the detector to a manageable level (< TPC rate)

We have designed the prototype data acquisition system to read out the large body of data from the Phase-1 sensors at high speed, to perform data compression, and to deliver the sparsified data to an event building and storage device.

The proposed architecture for the readout of the Phase-1 prototype system is shown in Figure 19 with the physical location and separation of the system blocks shown in Figure 20.

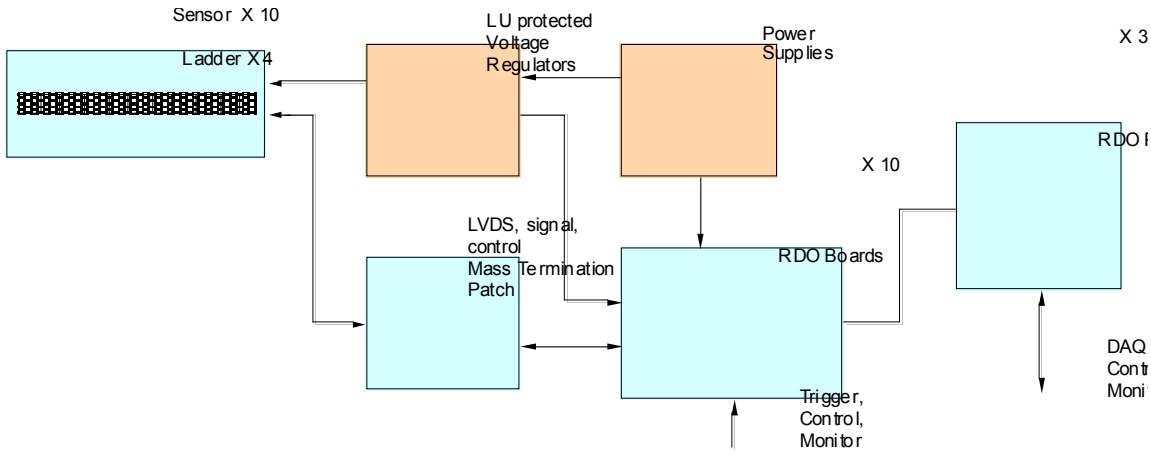


Figure 19: Functional block schematic for the readout for the Phase-1 prototype system. The detector ladders and accompanying readout system have a highly parallel architecture. One system unit of sensor array / readout chain is shown. There are ten parallel sensor array / readout chain units in the full system.

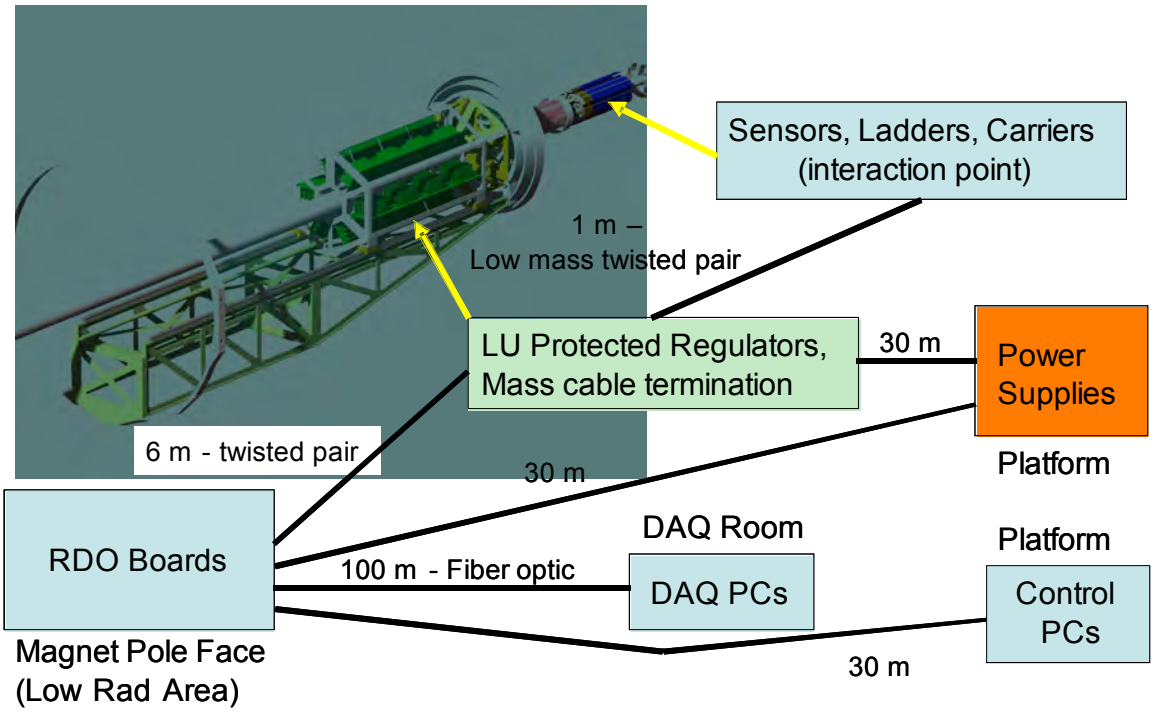


Figure 20: Physical layout of the readout system blocks. This layout will be the same for both the Phase-1 based patch and the final Pixel detector system.

The architecture of the readout system is highly parallel. Each independent readout chain consists of a four ladders mechanical carrier unit with each ladder containing ten Phase-1 sensors. The current plan is to install a patch of Phase-1 sensors consisting of at least two carrier units mounted with the final mechanical positioning structure and positioned with a 120 degree separation. The readout system will be described as if all carriers will be installed since this architecture also extends to the final Pixel system.

The basic flow of a ladder data path starts with the APS sensors. A Pixel ladder contains 10 Phase-1 APS sensors, each with a 640 × 640 pixel array. Each sensor contains four separate digital LVDS outputs. The sensors are clocked continuously at 160 MHz and the digital data containing the pixel threshold crossing information is read out, running serially through all the pixels in the sub-array. This operation is continuous during the operation of the Phase-1 detectors on the Pixel ladder. The LVDS digital data is carried from the four 160 MHz outputs in each sensor in parallel on a low mass flex printed circuit board to discrete LVDS buffers located at the end of the ladder and out of the low mass detector region. This electronics portion of the ladder also contains the buffers and drivers for the clocks and other control signals needed for ladder operation.

Each Phase-1 sensor requires a JTAG connection for register based configuration, power, ground, a 160 MHz readout clock and a synchronization signal to begin the readout. These signals and latch-up protected power as well as the LVDS outputs and synchronization and marker signals from the detectors are carried via low mass twisted pair cables from the discrete electronics at the end of the ladder to a power / mass termination board located approximately 1 meter from the Pixel ladders. There is one readout board per Pixel carrier (40 sensors). A diagram of a ladder is shown in Figure 21.

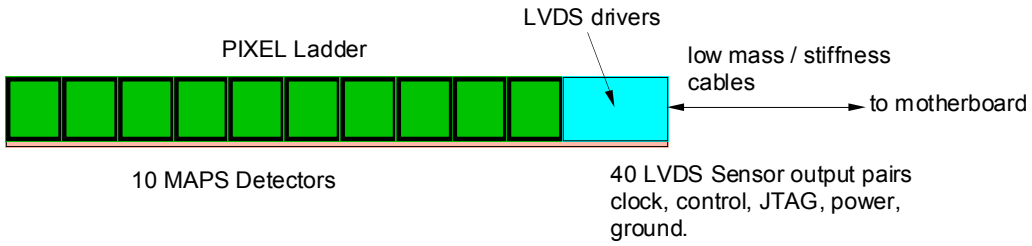


Figure 21: Assembly of sensors on a low radiation length kapton flex cable with aluminum conductors. The sensors are connected to the cable with bond wires along one edge of the ladder.

The flex cable parameters are shown below;

- 4 layer - 150 micron thickness
- Aluminum Conductors
- Radiation Length ~ 0.1 %
- 40 LVDS pair signal traces
- Clock, JTAG, sync, marker traces.

The connection to the driver end of the ladders will be made with very fine 150 μm diameter twisted pair wire soldered to the cable ends. These wires are also very low stiffness to avoid introducing stresses and distortions into the mechanical structure. The other ends of these fine twisted pair wires will be mass terminated to allow connection to the Power / Mass-termination (PM) board located approximately 1 meter away.

Latch-up protected power is provided to the sensors from the PM boards. Each ladder has independently regulated power with latch up detection circuitry provided by a power daughter card that plugs into the PM board. There are four regulation and latch-up daughter cards per PM board and a total of ten PM boards are needed for the complete detector system readout. A block diagram for the PM board is shown in Figure 22.

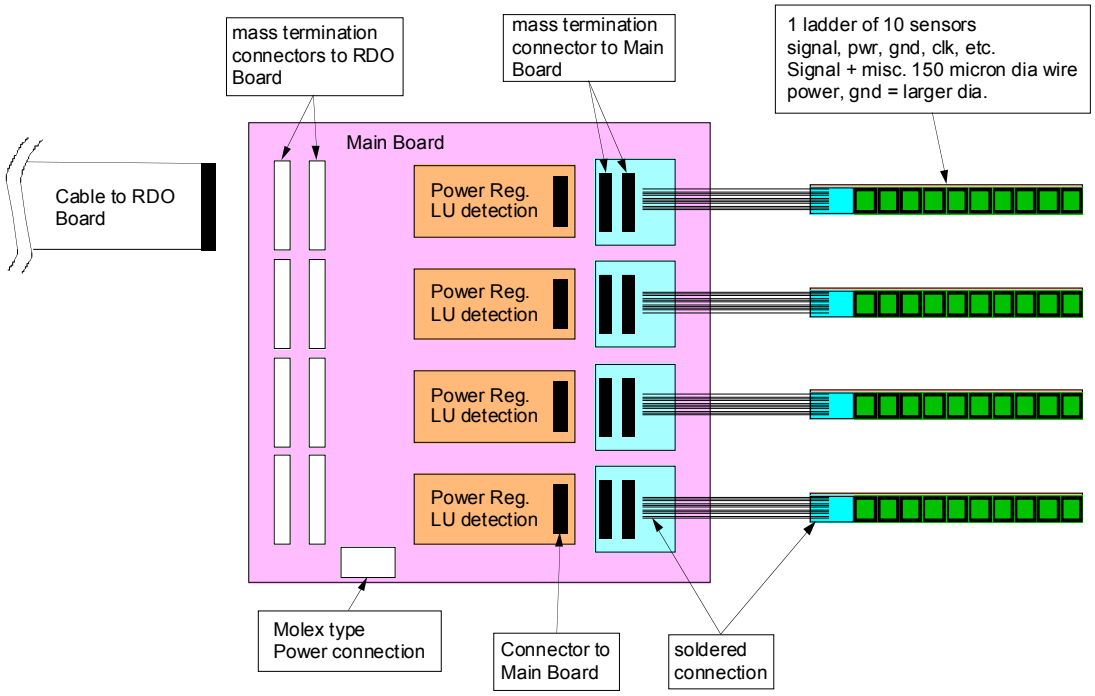


Figure 22: Power and mass-termination board block diagram. The digital signals to and from the sensors are routed through the main board and carried to mass termination connectors for routing to the readout boards. Latch-up protected power regulation is provided to each ladder by a power daughter card mounted to the main board. The main power supplies are located in the STAR racks.

The digital sensor output signals are carried with a 160 MHz clock to from the PM board to the readout boards (RDO) which are mounted on the magnet iron of the STAR magnet structure approximately 6 meters away. A diagram describing the attributes of the two PCBs that make up the RDO system can be seen in Figure 23. A functional block diagram of the RDO can be seen in Figure 24.

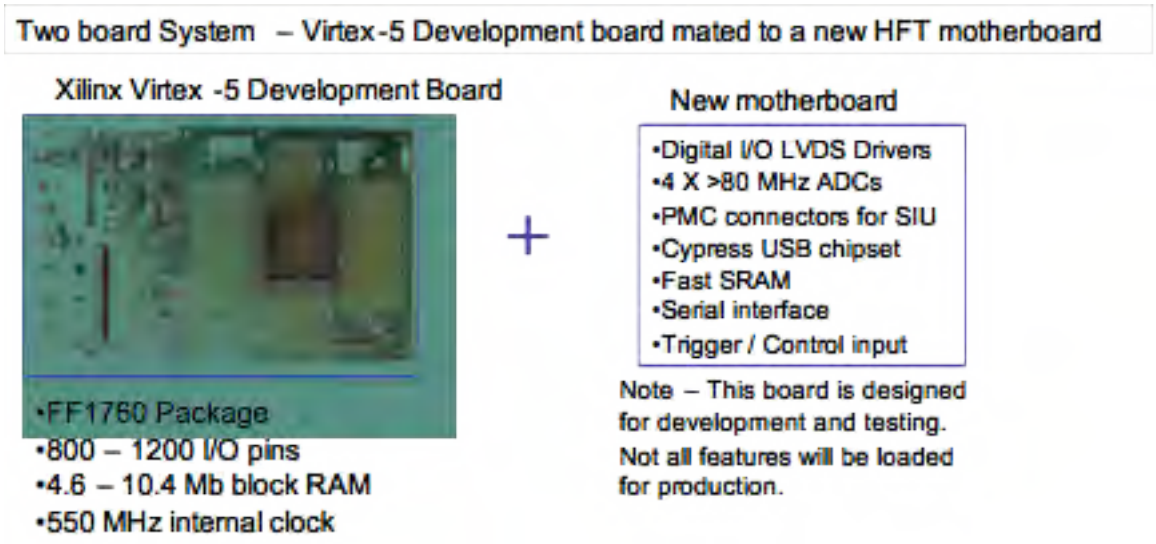


Figure 23: Readout board(s). The readout system consists of two boards per carrier of 40 sensors. A commercial Xilinx Virtex-5 development board is mated to a custom motherboard that provides all of the I/O functions including receiving and buffering the sensor data outputs, receiving the trigger from STAR and sending the built events to a STAR DAQ receiver PC via fiber optic connection.

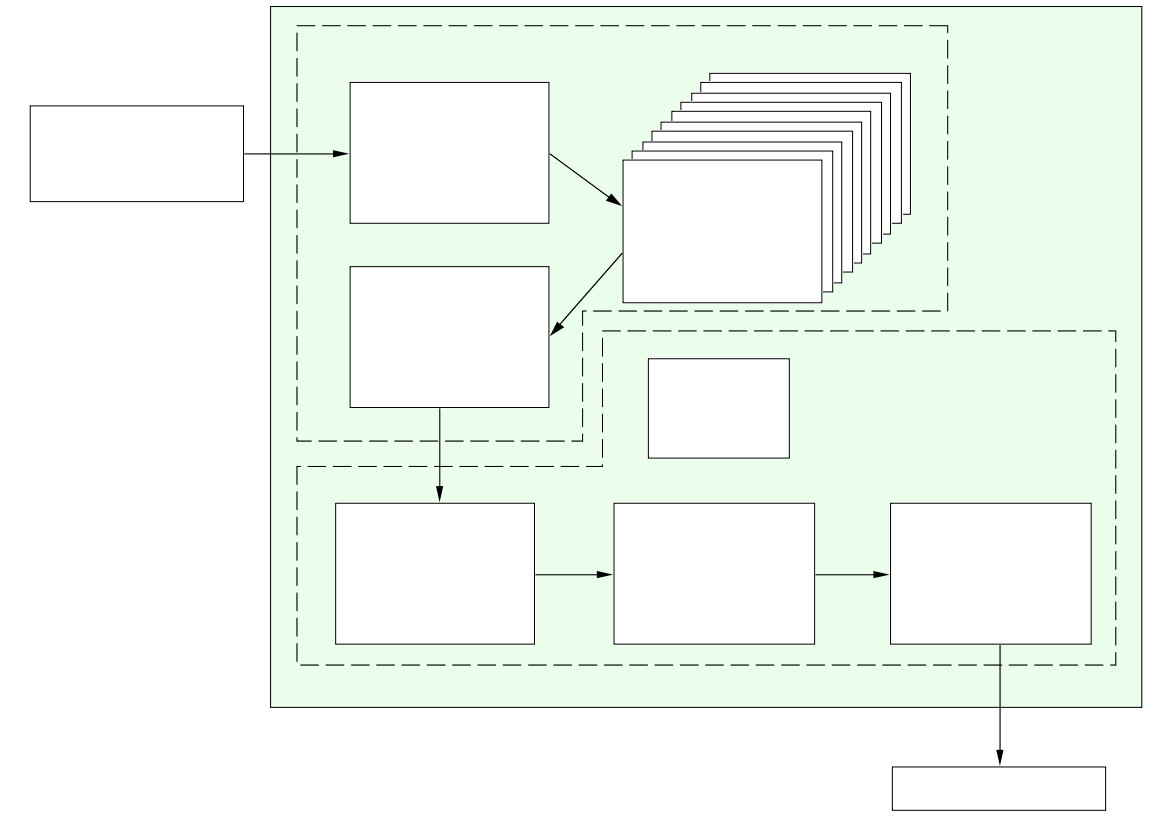


Figure 24: Functional block diagram of the data flow on the RDO boards.

The RDO boards are based on a fast Xilinx Virtex-5 FPGA development board which is mated to a custom motherboard that provides LVDS buffering into the FPGA, the STAR trigger input, PMC connectors for mounting the CERN developed fiber optic Detector Data Link (DDL), SRAM, and various ADCs and I/O to be used in testing. The data processing path is as follows. The sensor output signals are buffered and then fed into the FPGA. In the FPGA the data is resorted to give a raster scan, after which hits registered on pixels are converted to pixel addresses using an address counter. This mechanism of zero suppression, the conversion of hits to addresses in a relatively low multiplicity environment, is the main mechanism for data reduction used in this readout system. The efficiency and accidental rate of a simple threshold on pixel signal is shown in Figure 25.

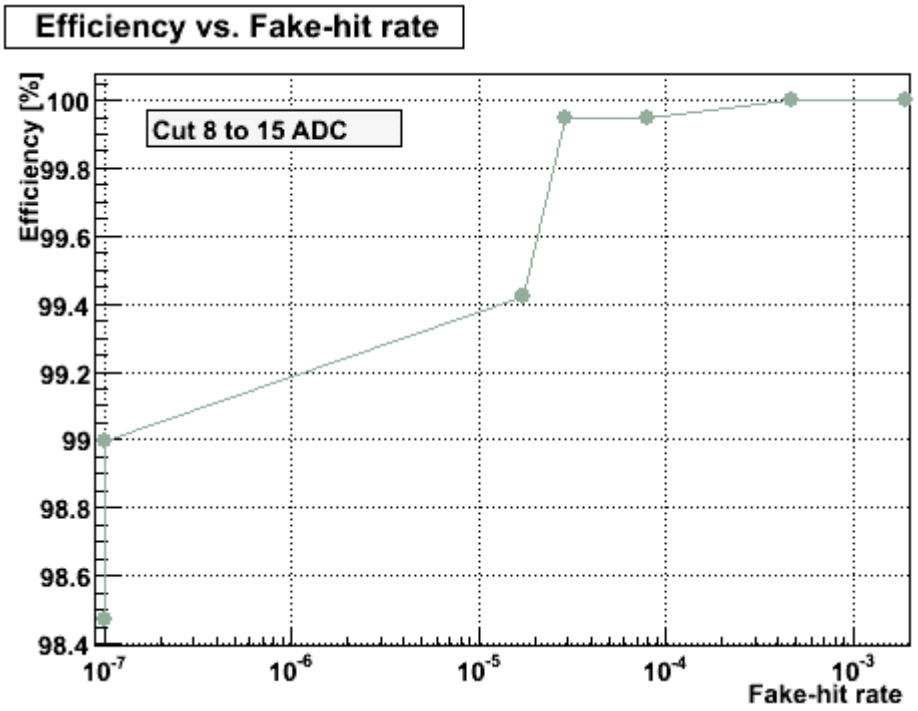


Figure 25: Efficiency and fake hit rate for a simple threshold cut on pixel signal level. This figure is obtained from beam data taken with Mimostar-2 sensors.

When a trigger is received, one of a bank of event buffers is enabled for one frame (409,600 pixels). After the frame has been recorded in the event buffer, the results of that frame are sent to an event builder. The event builder gathers all of the addresses on the RDO from that trigger and builds them into an event which is then passed via fiber optic links to the STAR DAQ receiver PCs. We intend to use the Source Interface Unit (SIU) and Readout Receiver Cards (RORC) developed for ALICE as our optical link hardware to transfer data to and from the STAR DAQ system. These links have been chosen as the primary readout connections for the new STAR TPC FEE. Leveraging existing hardware and expertise in STAR allows for a faster and more reliable design than developing our own custom solution. The complete system consists of a parallel set of carrier (4 ladder /

carrier) readouts consisting of 10 separate chains. A system level functionality block diagram is shown in Figure 26.

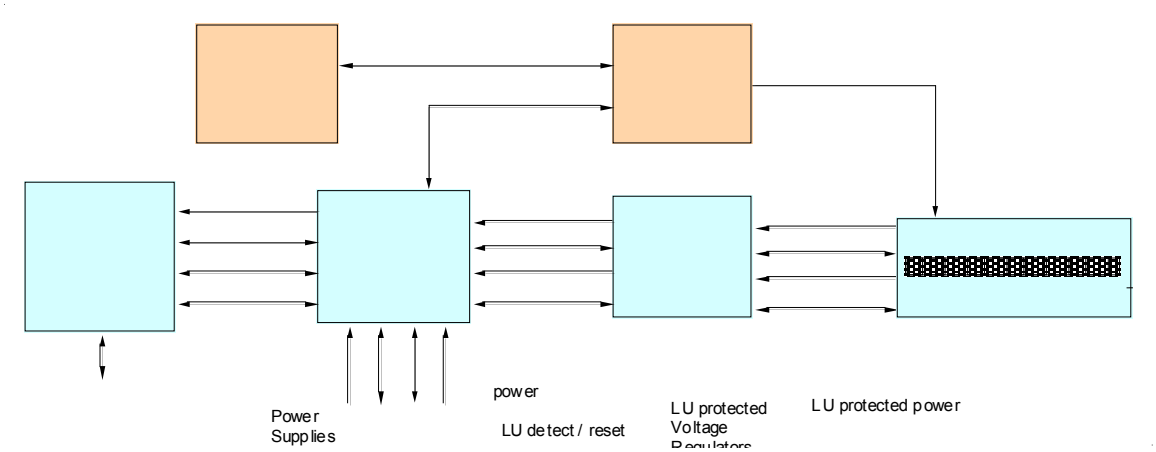


Figure 26: System level functionality diagram of the readout of the Pixel sensors. One of the ten parallel readout chains is shown.

Data Synchronization, Readout and Latency

The readout of the prototype Phase-1 Pixel sensors is continuous and hit-to-address processing is always in operation during the normal running of the detector. The receipt of a trigger initiates the saving of the found hit addresses into an event buffer for 1 frame (409,600 pixels). The Pixel detector as a whole will be triggered via the standard STAR Trigger Clock Distribution (TCD) module. Since 640 μs are required to read out the complete frame of interest, the data will be passed to DAQ for event building ~ 640 μs after the trigger is received. We will provide for multiple buffers that will allow the capture of temporally overlapping complete frames. This will allow us to service multiple triggers within the 640 μs readout time of the sensor. In this system, the hit address data is fanned out to 10 event buffers. A separate event buffer is enabled for the duration of one frame upon the receipt of a trigger from the TCD. Subsequent triggers enable additional event buffer until all of the event buffers are full and the system goes busy. The resulting separate complete frames are then passed to the event builder as they are completed in the event buffers. This multiple stream buffering gives a system that can be triggered at a rate above the expected average rate of the STAR TPC (approximately 1 kHz) after the DAQ1K upgrade. Furthermore, since the addition of buffers is external to the sensors, the capability for the addition of large amounts of fast SRAM will be included in the RDO board design allowing for flexibility in our readout system configuration. This multiple event buffer architecture will result in the duplication of some data in frames that overlap in time, but our data rate is low and the duplication of some data allows for contiguous event building in the STAR DAQ, which greatly eases the offline analysis. In addition, synchronization between the ladders/boards must be maintained. The Pixel will receive triggers and the STAR clock via the standard STAR Trigger and Clock Distribution module (TCD). We will provide functionality to allow the motherboards to be synchronized at startup and any point thereafter.

Triggering Considerations

The primary tracking detector of the STAR experiment is the TPC with the Heavy Flavor Tracker upgrade designed to add high resolution vertex information. The Pixel detector is part of a larger group of detectors that make up the HFT upgrade at STAR. The other tracking detector components of the HFT include the Silicon Strip Detector (SSD) and the Intermediate Silicon Tracker (IST). Since the HFT is a system of detectors, in order to maximize efficiency, the trigger response and dead time characteristics of the each detector in the HFT system should be matched, as much as possible, to the others. As the main detector, the post DAQ-1K TPC sets the effective standard for the other detectors in the system. In the current understanding of the system, the Pixel detector information is only useful in conjunction with the external tracking detectors and thus the Pixel detector will only be triggered when the TPC is triggered.

The triggers in STAR are produced essentially randomly with a 110 ns crossing clock spacing. The behavior of the TPC is to go dead for 50 μs following the receipt of a trigger. This means that the TPC, and by extension the Pixel detector, will receive random triggers spaced by a minimum of 50 μs. An additional constraint is imposed by the fact that the DAQ 1K contains 8 buffers at the front end. This allows for the capability of the TPC to take a quick succession of 8 triggers (separated by 50 μs) but then the TPC will go busy until the data has been transferred and buffers cleared. The time required for this depends on the event size. (Some of these numbers can be found at http://drupal.star.bnl.gov/STAR/daq1000-capabilities others are private communication with the STAR DAQ group (Tonko Ljubicic)). This behavior provides the basis for the assessment of the trigger response characteristics of the detectors in the HFT system. In general, HFT detector readout systems should provide for the acquisition of up to 8 successive triggers separated by 50 μs with some, as yet uncharacterized, clearing time. The goal is to have the HFT detectors "live" whenever the TPC is "live". In appendix 1 we show some analysis of the trigger response characteristics of the Pixel detector.

System Performance for the Phase-1 Prototype Sensor System

The raw binary data rate from each Phase-1 sensor is 80 MB / s. For the 400 sensors that make up the Pixel detector this corresponds to 32GB / s. This raw data rate must clearly be reduced to allow integration into the overall STAR data flow. Zero suppression by saving only addresses of hit pixels is the main mechanism for data volume reduction. The parameters used to calculate the data rates are shown below in Table 5.

Item	Number
Bits/address	20
Integration time	640 μs
Luminosity	3×10^{27}
Hits / frame on Inner sensors (r=2.5 cm)	295
Hits / frame on Outer sensors (r=8.0 cm)	29
Phase-1 sensors (Inner ladders)	100
Phase-1 sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5
Average Trigger rate	1 kHz

Table 5: Parameters used to calculate data rates from a Phase-1 based system.

Based on the parameters given above, the average data rate (address only) from the sensors in the prototype Phase-1 detector is 237 kB / event which give an average data rate of 237 MB / s. It is possible to reduce the data rate further using a run length encoding scheme on the addresses as they are passed from the event buffer to the event builder as indicated in Table 5. We are currently investigating this option, though the data rate reduction from this approach is expected to be moderate. The raw data rate reduction from the hit pixel to address conversion is given graphically below as Figure 27.

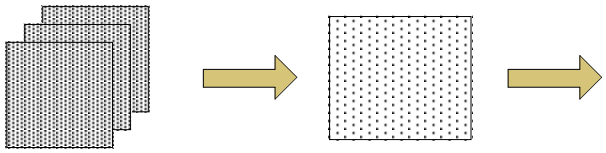


Figure 27: Data rate reduction in the Phase-1 readout system.

Architecture for the Ultimate Sensor System

The most significant difference between the Phase-1 and Ultimate sensors is the integration of zero suppression circuitry on the sensor. The ultimate sensors provide zero suppressed sparsified data with one LVDS output line per sensor. In addition, the sub-frame arrays are clocked faster to give a <200 μs integration time and a frame boundary marker is added to the data stream to allow for the demarcation of frame boundaries in the absence of hits in the sensor and to allow for synchronization with the RDO system.

The upgrade from the Phase-1 to the Ultimate sensors in the system is expected to involve the fabrication of new sensor ladders using the same mechanical design used in Phase-1 but with the addition of new Ultimate series sensors and a redesign of the kapton readout cable. The Ultimate sensor kapton readout cable will require significantly fewer (20 LVDS pairs instead of 40) traces for readout and the new cable design should have a lower radiation length. The task of reading out the Ultimate series sensors is actually less challenging than the readout of the Phase-1 sensors since the data reduction functionality is included in the sensor. **The readout hardware described above for the Phase-1 readout system remains the same for the Ultimate readout system.** Some reconfiguration of the functionality in the FPGA is required for readout of the Ultimate sensor Pixel detector. A functional block diagram for the RDO boards is shown in

Figure 28.

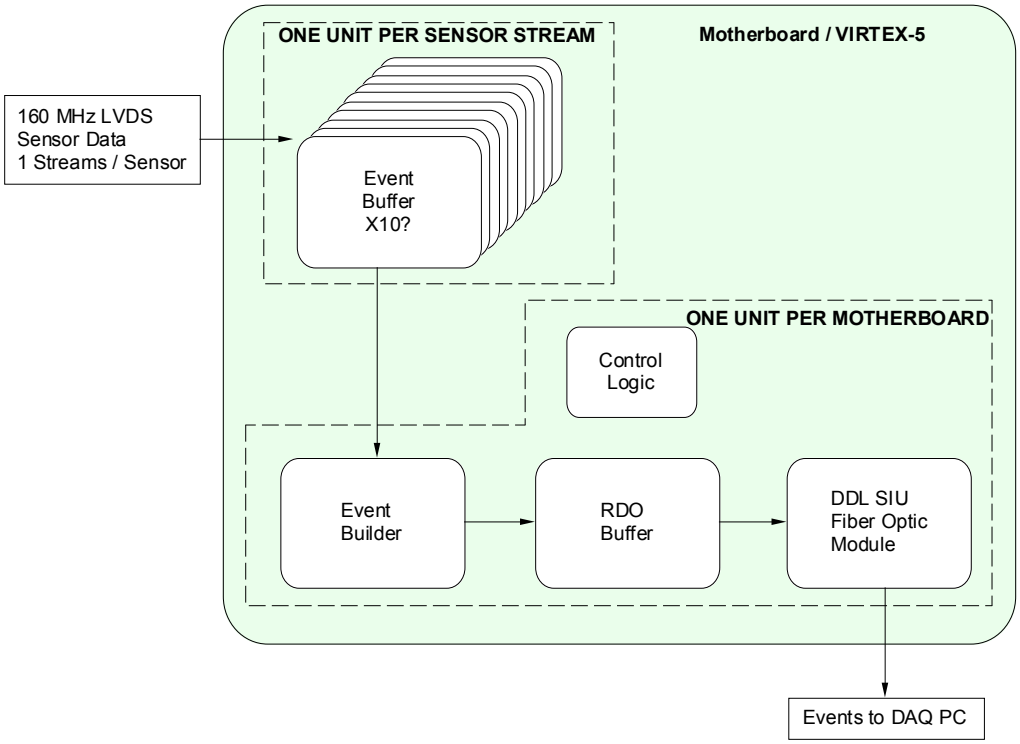


Figure 28: Functional block diagram of the RDO boards for the readout of the Ultimate detector based Pixel detector.

The Ultimate sensor operates in the same rolling shutter readout mode as the PHASE-1 sensor. The address data clocked out of the Ultimate chip has understood latencies that we will use to keep track of triggered frame boundaries and will be able to verify using synchronization markers from the sensors. The first pixel marker from the sensor corresponds to the actual scan of pixels through the sensor. The frame boundary marker delineates frame boundaries in the sparsification system on the sensor. Using this information and knowing the internal latencies in the sensor, we can generate the internal

logic in the FPGA to implement the same multiple buffering technique that was previously described.

System Performance for the Ultimate Sensor System

The parameters used to calculate the data rates for the system are shown in Table 6.

Item	Number
Bits/address	20
Integration time	200 μs
Luminosity	8×10^{27}
Hits / frame on Inner sensors (r=2.5 cm)	246
Hits / frame on Outer sensors (r=8.0 cm)	24
Phase-1 sensors (Inner ladders)	100
Phase-1 sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5
Average Trigger rate	1 kHz

Table 6: Parameters used to calculate data rates from a Ultimate sensor based system.

From these parameters, we calculate an average event size of 199 kB giving an address data rate of 199 MB / s from the Ultimate sensor based Pixel detector.

A more detailed analysis of the readout chain including parameters such as the size of buffers and the internal FPGA functions is included as appendix 1.

4.2.4. Sensors and Readout Simulation and Prototyping

Mimostar-2 based telescope test at STAR

Using a preliminary system design for analog readout, we have taken data with a set of Mimostar-2 sensors at STAR. This system is an early prototype whose performance is evaluated as part of the overall vertex detector development effort. We have successfully implemented a continuous readout 50 MHz data acquisition system with on-the-fly data sparsification that gives near three orders of magnitude data reduction from the raw ADC rates. This readout system has been mated with prototype Mimostar2 sensors and configured as a telescope system to measure the charged particle environment in the STAR environment near the final detector position. This telescope is shown in Figure 29.

Figure 29: Three Mimosrat-2 sensors in a telescope configuration used in a beam, test at STAR.

We find that the system works well, gives reasonable efficiency and accidental hit rates, and measures an angular distribution of tracks consistent with imaging the interaction diamond and with imaging beam-gas interaction type background. The prototype readout system integrated well into the existing STAR electronics and trigger infrastructure and functioned successfully as another STAR detector subsystem. This prototype readout system and the results obtained are described in a NIM paper[29].

LVDS Data Path Readout Test

As a necessary part of the design validation, we have performed a test of the high speed LVDS data path. The

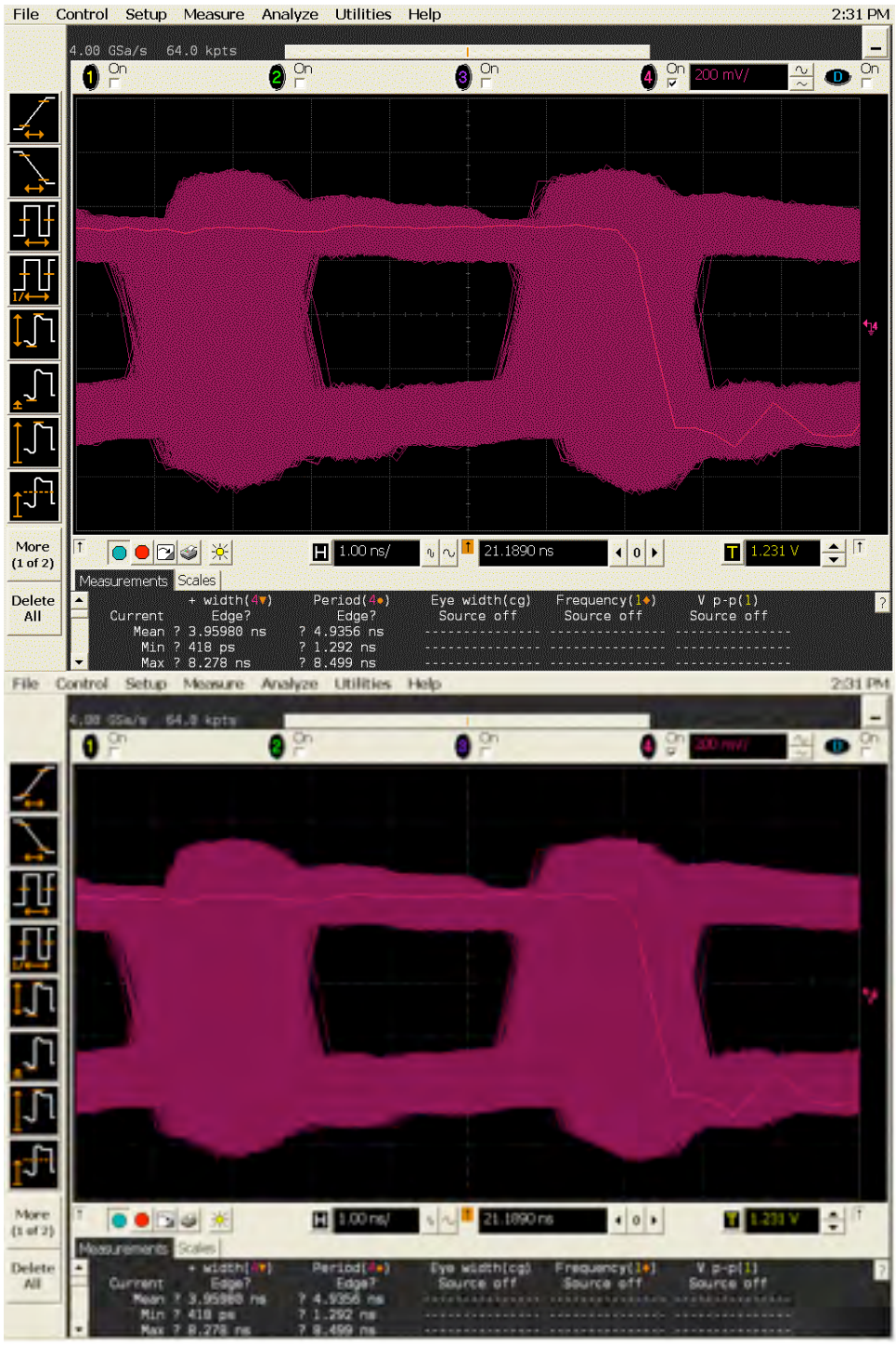


Figure 30: 200 MHz Data eye pattern measured at the RDO motherboard input to

the FPGA (after all buffers) and triggered on the output data from the FPGA. Full width opening in system is ~ 2.3 ns.

4.2.5. Mechanical Design

Design Overview

The mechanical design has been driven by the following design goals:

Minimize multiple coulomb scattering, particularly at the inner most layer

Locate the inner layer as close to the interaction region as possible

Allow rapid detector replacement

Provide complete spatial mapping of the pixels from the beginning

The first two goals, multiple coulomb scattering and minimum radius, set the limit on pointing accuracy to the vertex. This defines the efficiency of D and B mesons detection.

The third goal, rapid detector replacement, is motivated by recognition of difficulties encountered in previous experiments with unexpected detector failures. This third goal is also motivated by the need to replace detector that are radiation damaged from operating so close to the beam.

The fourth goal, complete spatial mapping, is important to achieve physics results in a timely fashion. The plan is to know at installation where the pixels are located with respect to each other to within 20 microns and to maintain the positions throughout the operation.

The pixel detector (see Figure 31) consists of two concentric barrels of detector ladders 20 cm long. The inner barrel has a radius of 2.5 cm and the outer barrel has an 8 cm radius. The barrels separate into two halves for assembly and removal. In the installed location both barrel halves are supported with their own 3 point precision kinematic mounts located at one end close to the detector barrel. During installation, support is provided by the hinge structures mounted on a railed carriage. Cooling is provided by air flowing in from one end between the two barrel surfaces and returning in the opposite direction over the outer barrel surface and along the inner barrel surface next to the beam pipe.

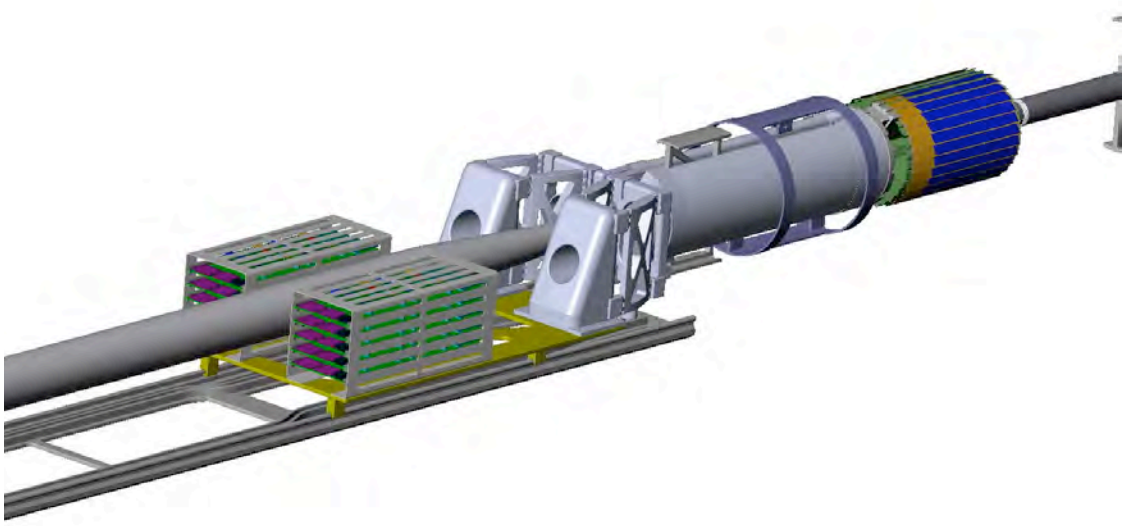


Figure 31 Pixel detector mechanics showing detector barrel, support structures and insertion parts plus interface electronics boards.

The design of the components is presented in the following section. Related structural and cooling analysis is covered in Appendix 2.

Detector ladder design

As previously mentioned (section 0) the detector chips are arranged 10 in a row to form a ladder. An exploded view of the mechanical components is shown in Figure 32. The thinned silicon chips are bonded to a flex aluminum Kapton cable which is in turn bonded to a thin carbon composite structure. All electrical connections from the chips to the cable are done with a single row of wire bonds along one edge of the ladder. The carbon composite sheet which is quite thin will only be sufficient for handling and heat conduction. The primary stiffness and support of the ladder is provided by the support beam. This particular ladder structure has not been built yet, but it will utilize construction methods that we have developed in our previous prototype designs which included gull wing and foam laminate designs. Parts are aligned and held in place with vacuum chuck tooling for bonding. Fifty micron soft, pressure sensitive acrylic adhesive 200MP by 3M is used to make the bonds. A method has been developed which uses a 4 bar pressure chamber to remove bond voids and to stabilize the bond. The low elastic modulus of the adhesive is an important component in the design as it greatly reduces bi metal type deformations stemming from differential expansion caused by thermal changes and humidity changes. This will be discussed in more detail in Appendix 2.

The next step in the ladder development will be to build mechanical prototypes to verify the mechanical design both structurally and thermally.

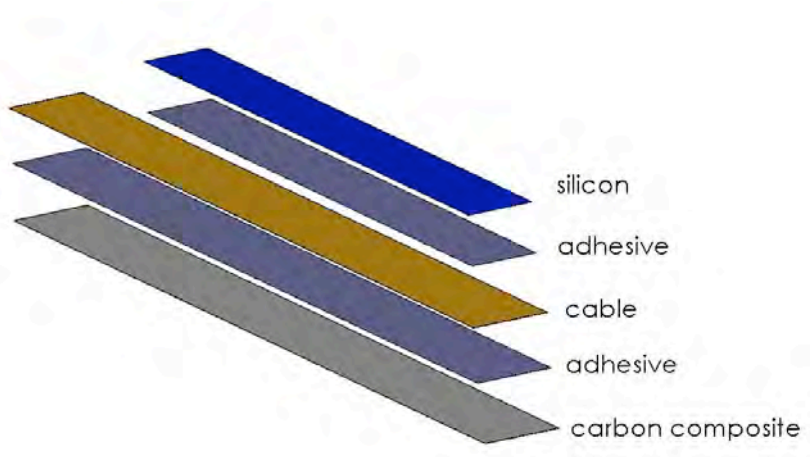


Figure 32 Exploded view of the ladder showing components. The silicon is composed of 10 ~square chips, bit it is shown hear as continuous piece of silicon as it has been modeled for analysis.

Ladder support system

A critical part of the ladder support is the thin carbon composite beam which carries one inner ladder and three outer ladders as shown in Figure 33. This beam which is an adaptation of the ALICE pixel detector design provides a very stiff support while minimizing the radiation length budget. Significant stiffness is required to control deformations from gravity, cooling air forces and differential expansion forces from both thermal and humidity variations. The composite beam carries a single inner ladder and three outer ladders. Ten of these modules form the two barrel layers. The beam in addition to its support function provides a duct for cooling air and adds cooling surface to increase heat transfer from the silicon chips. By making the beam from high strength and high thermal conductivity carbon fiber the wall thickness can be as thin as 200 microns and still satisfy strength and heat transfer requirements. The final thickness however, will probably be limited by fabrication challenges. Forming methods under consideration are a single male mandrel with vacuum bagging or alternatively nested male and female mandrels.

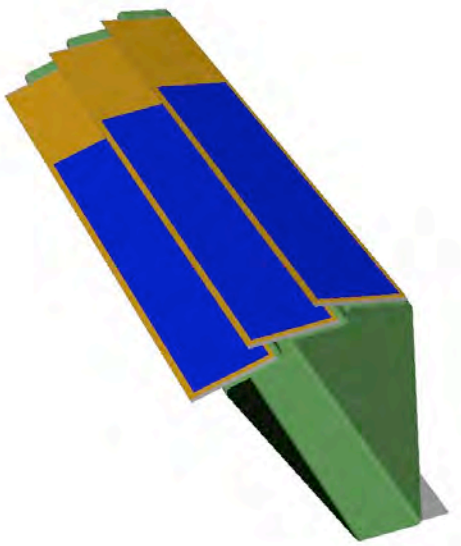


Figure 33 Thin wall carbon support beam (green) carrying a single inner barrel ladder and three outer barrel ladders. The beam in addition to supporting the ladders provides a duct for conducting cooling air and added surface area to improve heat transfer to the cooling air.

The ladders will be glued to the beam using a low strength silicon adhesive as was done in the ATLAS pixel design. This adhesive permits rework replacement of single ladders.

Support of the sectors (beam with ladders) is done in two halves with 5 sector beams per half module (see Figure 34). The sector beams are attached to carbon composite "D tube" with precision dove tail mounts for easy assembly and replacement.

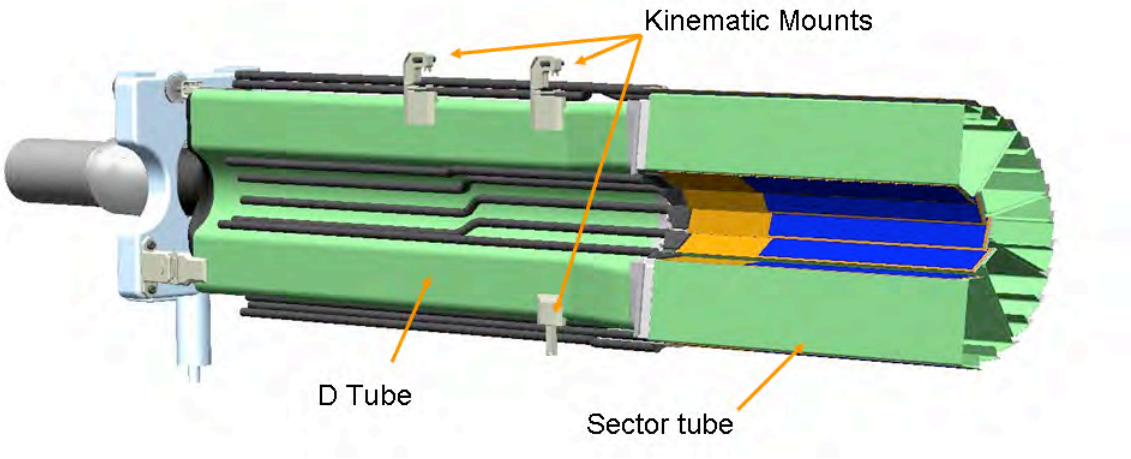


Figure 34 Half module consisting of 5 sector beam modules. The sector beam modules are secured to a carbon composite D tube using a dove tail structure which permits easy replacement of sector modules. Carbon composite parts are shown in green for greater visibility.

The "D tube" supports the 5 sector beams and conducts cooling air to the sectors.

Kinematic support and docking mechanism

When the pixel detector is in its final operating position it is secured at 3 points with precision reproducible kinematic mounts to the Inner Support Cylinder (ISC) as shown in Figure 35.

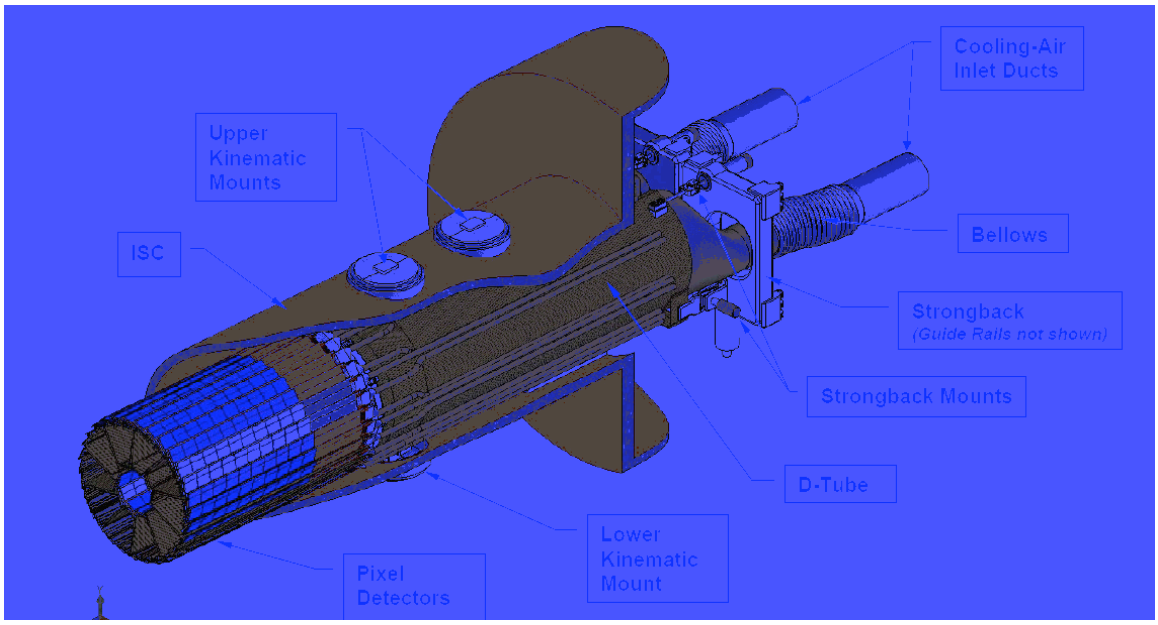


Figure 35 Detector assembly in the installed position supported with three kinematic mounts

A more detailed view of the kinematic mounts is shown in Figure 36. The mounts provide a 3-2-1 constraint system which should allow repeatable installation to within a few microns.

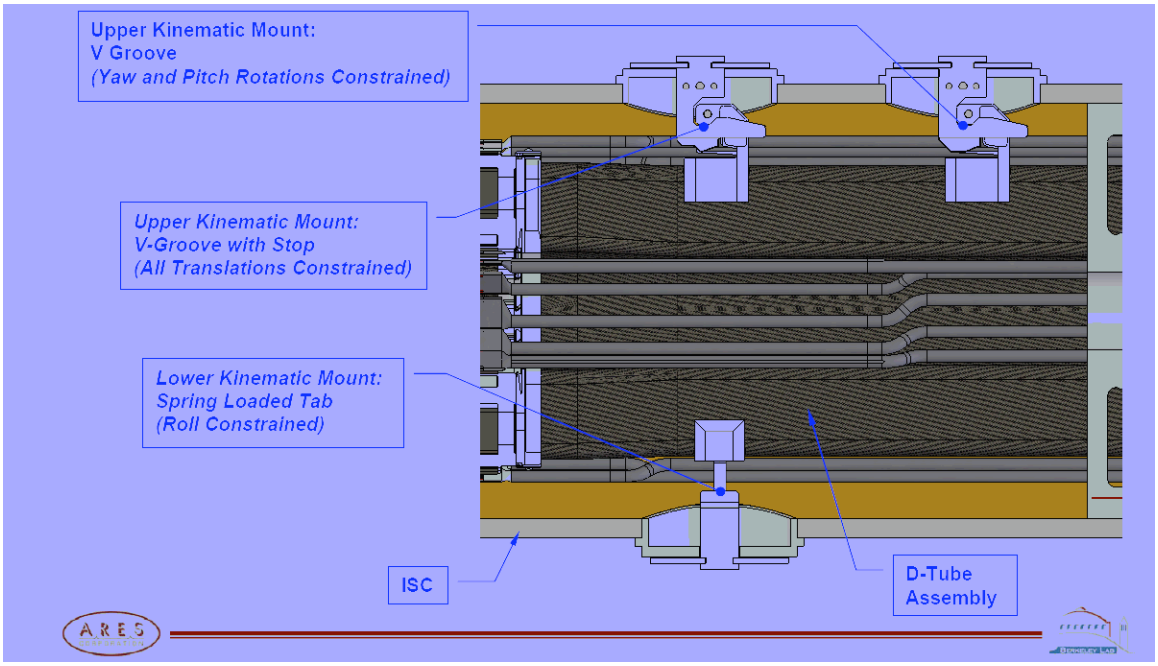


Figure 36 Detailed view of the kinematic docking mounts for the pixel detector. The mounts provide a fully constrained support and operate with a spring loaded over center lock down.

Insertion mechanism and Installation

The mechanics have been design for rapid installation and replacement. Instillation and removal of the pixel detector will be done from outside of the main STAR system with minimum disruption to other detectors systems. This will be done by assembling the two halves of the detector on either side of the beam pipe on rails outside of the STAR magnet iron. The detector carriage will be pushed into the center of STAR along the rails until it docks on the kinematic mounts. As shown in Figure 37 and Figure 38 the hinged support structure is guided by cam followers to track around the large diameter part of the beam pipe and close down at the center into the final operating position. Once the detector is docked in the kinematic mounts the hinged support from the carriage is decoupled allowing the kinematic mounts to carry the light weight detector system with a minimum of external forces affecting the position of the detector barrels. The external loads will be limited to the cables and the air cooling ducts. The cables are loosely bundled twisted pairs with 160 micron conductor plus insulation, so this load should be minimal. The two inch cooling ducts will be the greater load and may require additional design effort to isolate their effect so that the 20 micron position stability for the pixels can be maintained.

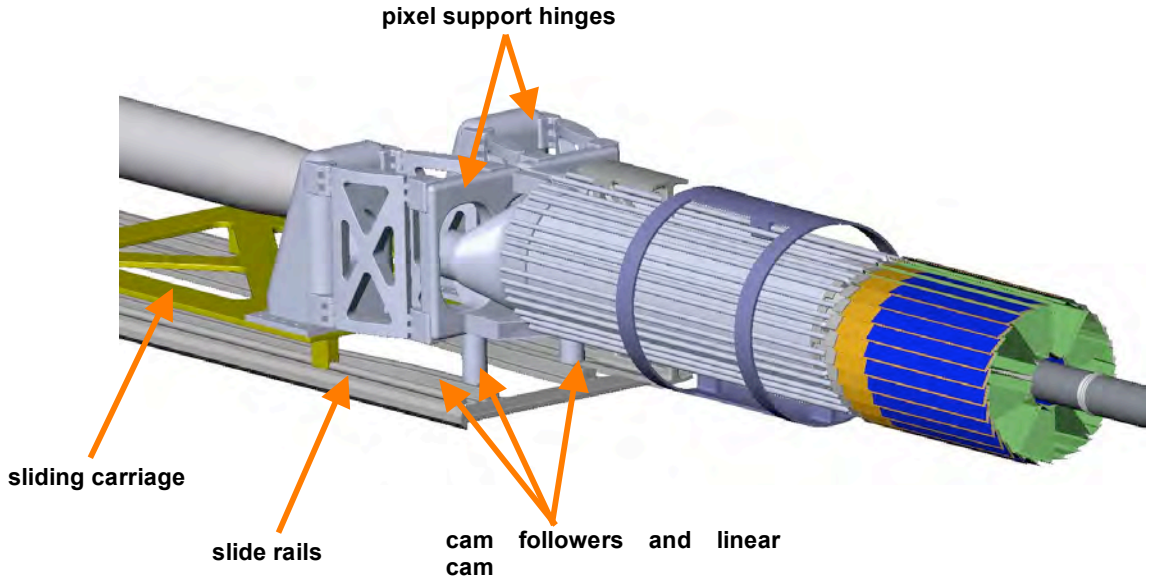


Figure 37 Track and cam guide system for inserting the detector.

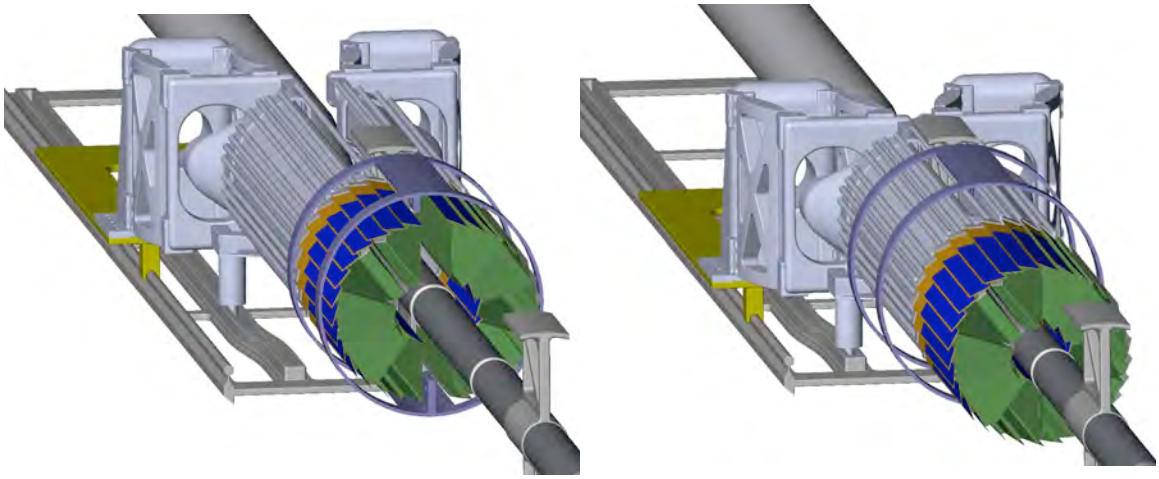


Figure 38 Initially the detector halves have to be sufficiently open to clear the large diameter portion of the beam pipe. It then closes down sufficiently to fit inside the IFC while clearing the beam pipe supports and then finally it closes down to the final position with complete overlapping coverage of the barrels.

Kinematic support

Cooling system

Cooling of the detector ladders with pixel chips and drivers is done with forced air. The pixel chips dissipate a total of 160 watts or 100 mW/cm^2 and an additional 80 watts is required for the drivers. In addition to the ladder total of 240 watts some fraction of this is required for voltage regulators and latch up electronics that are off the ladder but reside in the air cooled volume. The temperature of operation is still under consideration. An optimum temperature for the detectors is around 0 deg C, but they can be operated at 34 deg C without too much noise degradation. The cooling system design is simplified if we can operate at 24 deg C, slightly above the STAR hall temperature, however if the cooler temperature is required the cooling system will be equipped with thermal isolation and condensation control when the system is shut down. In any case the design will include humidity and temperature control as well as filtration. Cooling studies (see Appendix 2) show that air velocities of 8 m/s are required over the detector surfaces and a total flow rate of 200 cfpm is sufficient to maintain silicon temperatures of less than 12 deg C above the air temperature.

The detector cooling path is shown in Figure 39. Air is pumped in through the support beam. A baffle in the ISC forces the air to return back over the detector surfaces both along the beam pipe and along the ISC.

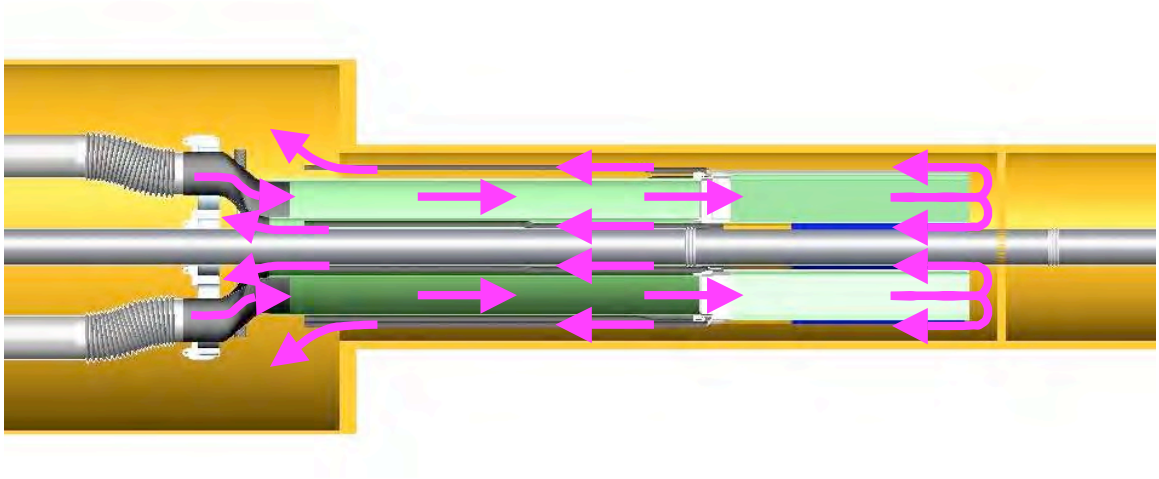


Figure 39 Pixel detector cooling air path. The air flows down the center of the sector modules and returns back over the detector ladders on the sector modules and into the larger ISC volume where it is ducted back to the air cooling unit.

The air chiller system providing the cooling air circulating through the pixel detector has not been completely specified yet, but sizing and ducting have been investigated for a system (see Figure 40) with 400 cfpm capacity (twice currently expected requirement). A commercially available centrifugal pump with a 5 horsepower motor is sufficient for this system. It is expected that the chiller would be located in the wide angle hall within 50 ft of the pixel enclosure and would be connected with 6 inch flexible ducts. An estimate of the required chiller heat capacity is given in Table 7.

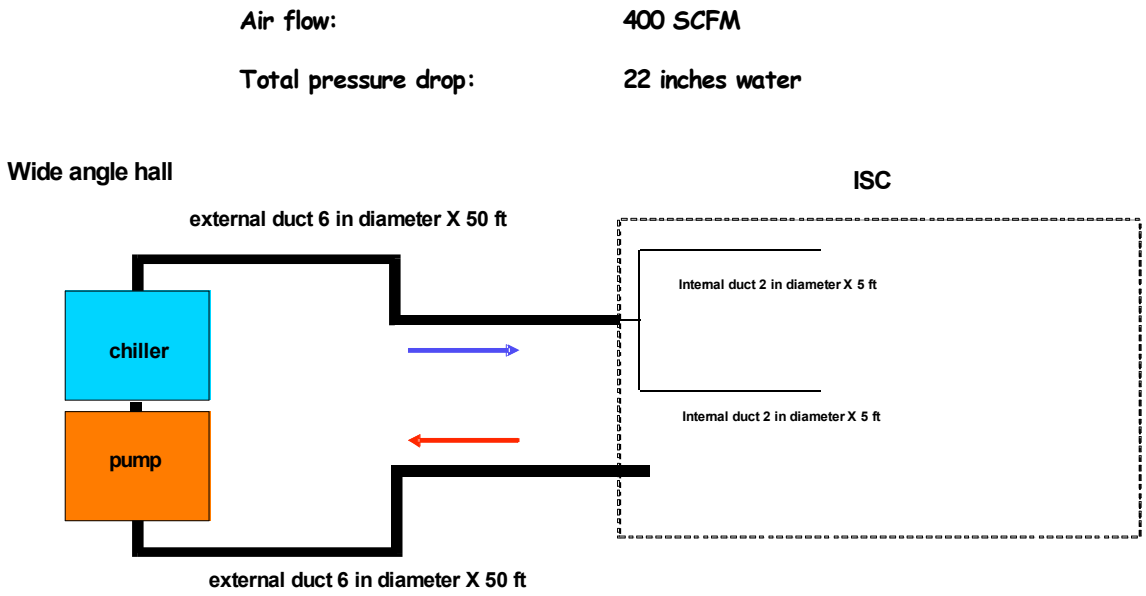


Figure 40 Schematic outline of air cooling system for the pixel detector

Heat source	Power (watts)
detector silicon	160
on ladder signal drivers	80
voltage regulators in ISC	24
heat influx through ducting and ISC if 35 deg C below ambient	600 - 2000
pumping	1000
Total load on chiller	1900 - 3300

Table 7 Preliminary estimate of heat load on the chiller for the pixel air cooling system

Cabling and Service system

The required wiring connections are identified in Figure 20. The 2 m fine wire twisted pair (pair diameter .32 mm) bundles leading from the ladders to the interface cards are designed to minimize mass, space and mechanical coupling forces that could disturb the pixel positions. The space envelope required for these bundles is illustrated in Figure 41.

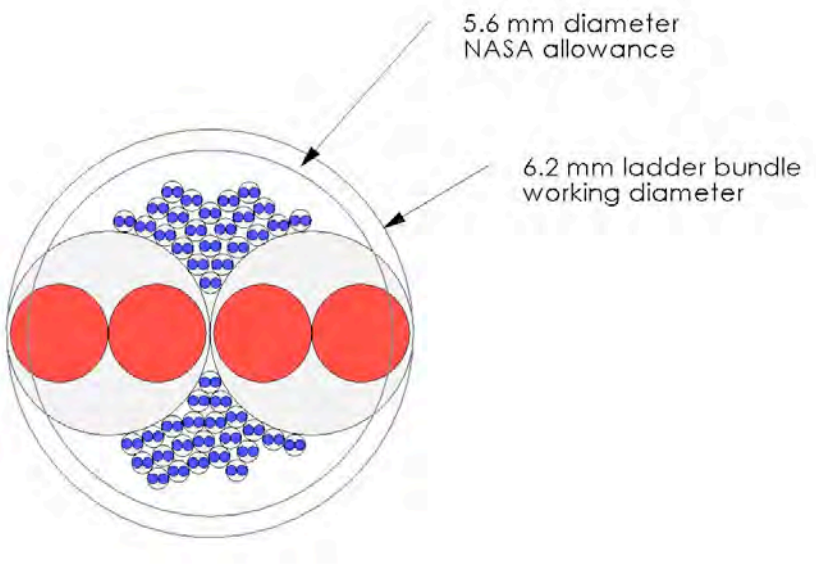


Figure 41 Cable bundle envelope for ladder connections. The blue pairs include 40 signal pairs, clock and trigger lines and JTAG communication. The red conductors are power.

There will be a 2'X2'X3' crate for the readout boards. This must be located outside of the main magnetic field and outside of the highest particle flux region. To achieve the required data transfer rates the LVDS signal cables running between this crate and drivers inside the ISC are limited to 6 meters. To meet these constraints the readout crate will a be located on the floor at the end of the magnet (there is no space on the magnet end ring for mounting the readout box). This will allow operation of the pixel system both with and without the pole tip in place (there is no space on the magnet end ring for mounting the readout box). The crate will be portable on wheels to accommodate end cap access requirements. Compared to the cables running to the detector the power and fiber optic cables from the readout crate to the outside are relatively small and provide little handling burden.Installation

Alignment and spatial mapping

The pixel system is being designed to have full pixel to pixel spatial mapping at installation with a 3D tolerance envelope of 20 microns. This will eliminate the need for spatial calibration with tracking other than determining the 6 parameters defining the pixel detector unit location relative to the outer tracking detectors. Tracking, however, can used with the pixel detector to spatially map the outer detectors if required.

The mapping and alignment will be done by using a vision coordinate machine to determine the detector locations on the fully constructed 20 ladder half modules. A full 3D map of the ladders is necessary since the manufactured ladder flatness will exceed the 20 micron envelope. After mapping the half modules will be installed in STAR without disturbing the relative positions of the pixels.

Addressing this in more detail, a support fixture for the half modules will be used in the vision coordinate machine which has kinematic mounts identical to the kinematic mounts in the ISC for securing the half module. The pixel chips will be manufactured with reference targets in the top metal layer that can be picked up by the vision coordinate machine and the ladders will be mounted such that there is an unobstructed view. The fixture will be rotated for each ladder measurement. Full 3D measurements of the chips on the ladder are required since the ladder flatness will lie outside of the 20 micron envelope. The fixture will have precision reference targets on each ladder plane so that the ladder points can be tied together into a single coordinate frame. The map of the fixture targets can be measured once with a touch probe measuring machine and thus avoid extreme machining tolerance requirements for the fixture. Precision machining, however, will be required, for the kinematic mounts and their placement tool.

For this approach to work the ladders must hold to their mapped position within 20 microns independent of changes in temperature, humidity and gravity direction.

The detector ladders have 1 mm overlapping active regions with their neighbors, so a check of the mapping accuracy will be done with tracking.

4.2.6. Mechanical Design Simulation and Prototyping

Ladder support Structural analysis

Ladder support prototype development

Ladder cooling analysis

Ladder cooling prototype tests

Insertion prototype tests

Kinematic support tests

4.3. IST

4.4. The Silicon Strip Detector

The STAR Silicon Strip Detector (SSD) is an existing detector that will enhance the performance of the HFT. It was originally designed to work with the TPC and the STAR Silicon Vertex Tracker (SVT); however these detectors were designed to take data at 200 Hz and so the SSD was designed and built to that specification as well. In order to match the goals of the HFT project, the SSD needs an upgrade in order to allow it to take data at 1000 Hz to match the new TPC electronics DAQ rate and the HFT detector DAQ rate. The upgrade will ensure that the SSD does not become a bottleneck in the HFT data acquisition system. The upgrade will be done with STAR capital funds (rather than HFT construction funds) but we describe it here because the success of the SSD upgrade is an important element in the success of the HFT.

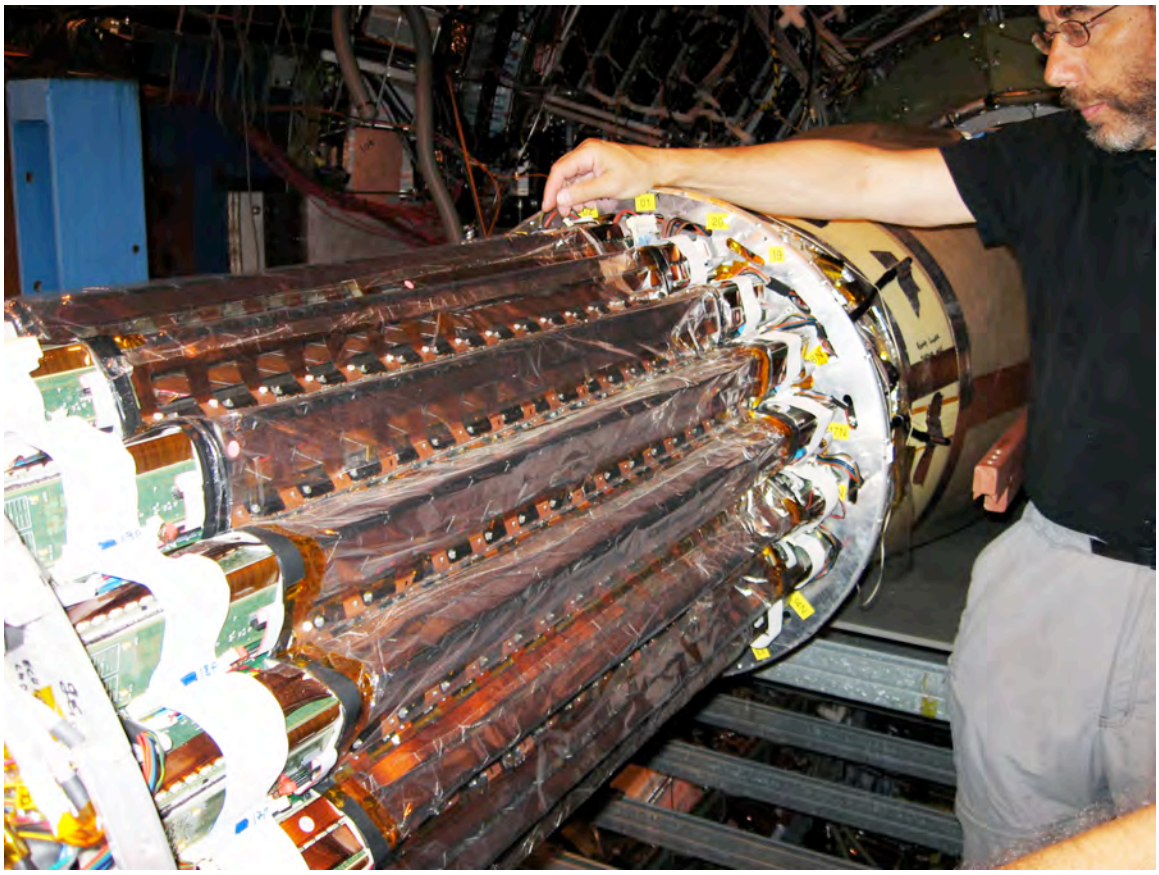


Figure 42: The photo shows the roll-out of the Silicon Strip Detector for routine maintenance.

The SSD is a high resolution Si detector, that is mounted inside the inner radius of the STAR TPC and lies at a radius of 23 cm. See Figure 43. It has the same ϕ and rapidity coverage as the TPC meaning that it offers full 2π azimuthal coverage and extends over a pseudo rapidity range of $|\eta| < 1.2$. Its radial location puts it midway between the event vertex and the TPC. Thus it is ideally suited for the purpose of improving the TPCs pointing and momentum resolution; and extending the physics program of both detectors.

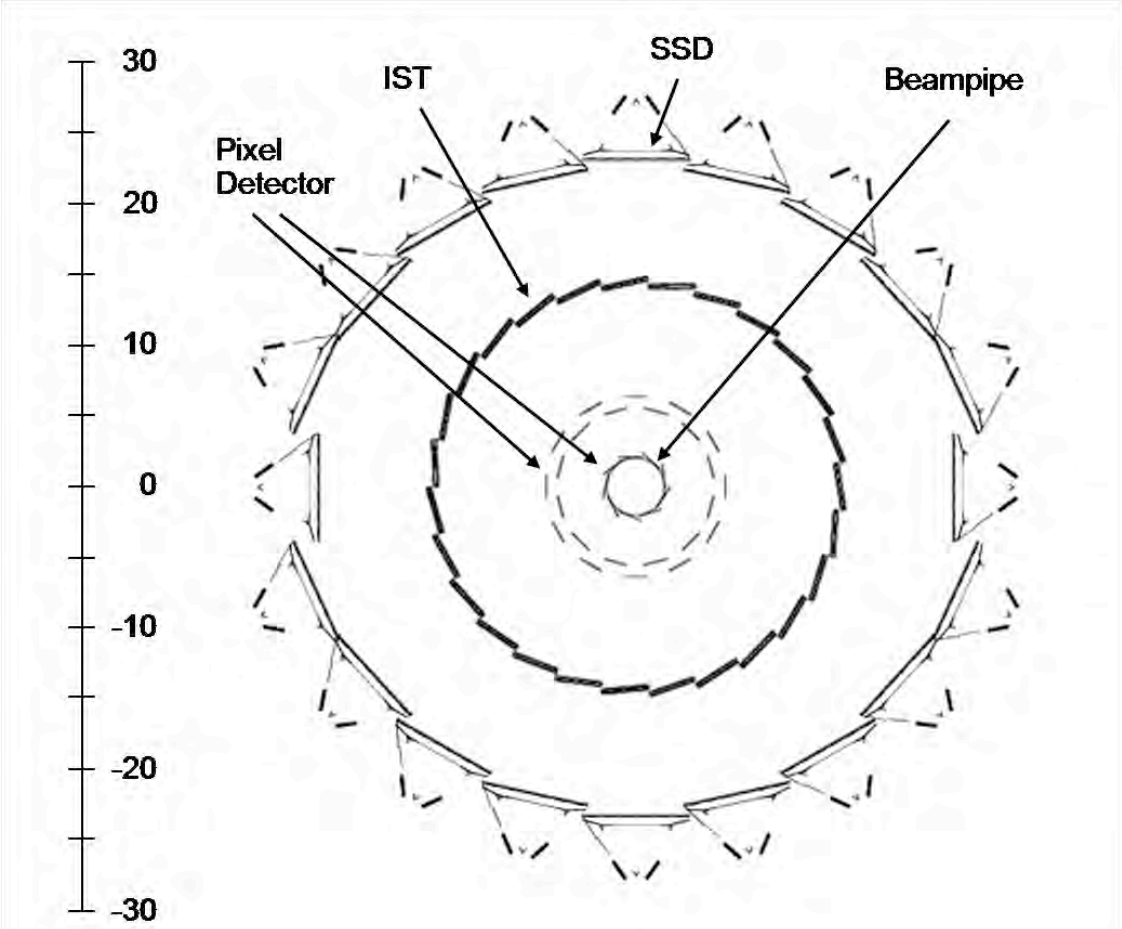


Figure 43: The SSD is shown surrounding the inner silicon tracking layers of the HFT.

The SSD is capable of locating a point on a track with a resolution of 30 μm in the R-ϕ direction and 850 μm in the Z direction[30,31]. This is a considerable improvement over the resolution of the TPC pointing at the SSD (which is greater than 1 mm in both directions) and so it enhances the overall pointing resolution of the combined system at the vertex. The excellent special resolution of the SSD is achieved by using double sided Si with a layer of strips on each side of the same piece of Si. The strip layers cross and are inclined by 35 mRad with respect to each other and are placed symmetrically with respect to the edge of the wafer. Because of this unique double-sided feature, the SSD is a thin detector and is only ~1% radiation length thick. This ensures that the multiple Coulomb scattering is kept as low as possible for charge particle traversing the detector, but it also means the detector can be used to tag non-photonic electrons while generating a minimum amount of background due to photon conversions.

The SSD enhances the physics program of the TPC and the DAQ upgrade will:

Improve the reconstructable yield of the strange mesons and baryons; especially the K, Λ, Ξ, and Ω.

Improve the invariant mass resolution for resonances and spectra measurements

Improve single track high p_T resolution by approximately a factor of 2

In addition, the SSD is also an integral part of the proposed Heavy Flavor Tracker (HFT) and it will enhance the efficiency for doing the topological reconstruction of open charm and beauty decays with the HFT. The performance of the SSD is similar to, and nearly redundant with, the performance of the IST. However, this is the only redundancy in the system and the redundancy is needed in order to ensure efficient track matching with the hits on the pixel layers in a high multiplicity environment. The SSD sits at an ideal location, with excellent performance characteristics, to be a critical element in the track matching algorithm for the HFT.

4.4.1. How the SSD affects the performance of the TPC

The excellent special resolution of the SSD, and its ideal location, means that it is suitable to extend and improve STAR tracking from the TPC to the vertex. For example, the SSD improves the single track DCA resolution, at the vertex, from a few mm to less than 1 mm in the R-ϕ direction without using a vertex constraint.[32] See Figure 44.

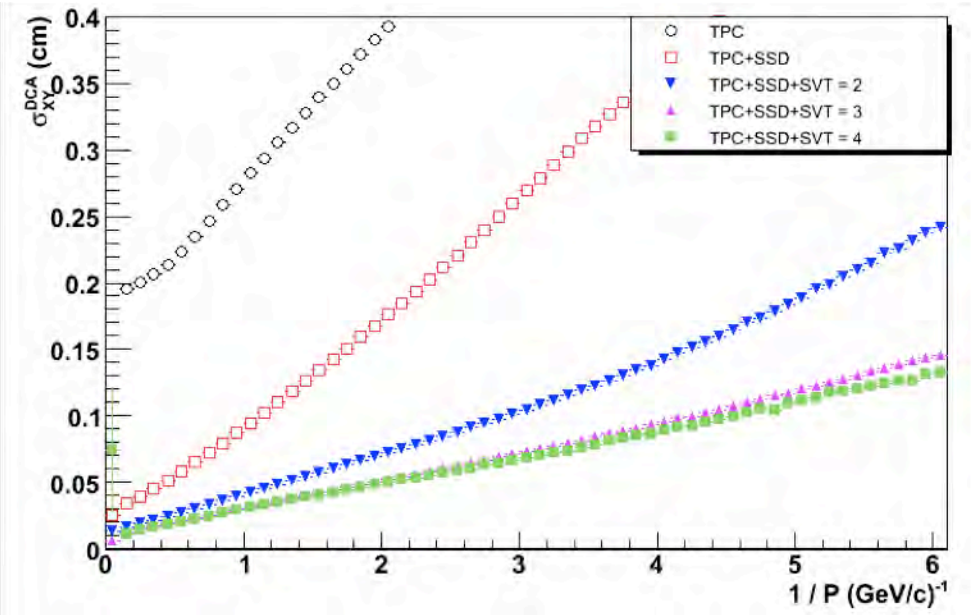


Figure 44: The DCA resolution of the TPC and the SSD versus the inverse momentum of the track. The top line shows the DCA resolution of the TPC, acting alone, for all tracks entering the TPC (i.e. no track cuts) during the high intensity Cu-Cu run at RHIC. The red line demonstrates how the pointing resolution of the TPC can be improved by including the SSD hits on tracks. The results are quoted for 200 GeV minBias Cu-Cu collisions with $|Z_{vertex}| < 5$ cm and $|\eta| < 1$. The remaining lines on eh plot show the performance of the old STAR Silicon Vertex Tracker and are not relevant here.

The improved pointing resolution provided by the SSD will yield important improvements in the reconstructable yield of neutral and charged particles that decay within a few cm of the event vertex; in particular the strange mesons and baryons (K, Λ, Ξ, and Ω). Figure 45 shows a sample of K^0 mesons measured in the Cu-Cu beam with and without the use of the SSD. The improved signal to noise ratio (due to the improved background rejection) for the detection of baryons, mesons and resonances, will be important in our upcoming heavy ion runs and especially in the proposed low energy scan, where the integrated luminosity (and thus statistics to tape) will be limited.

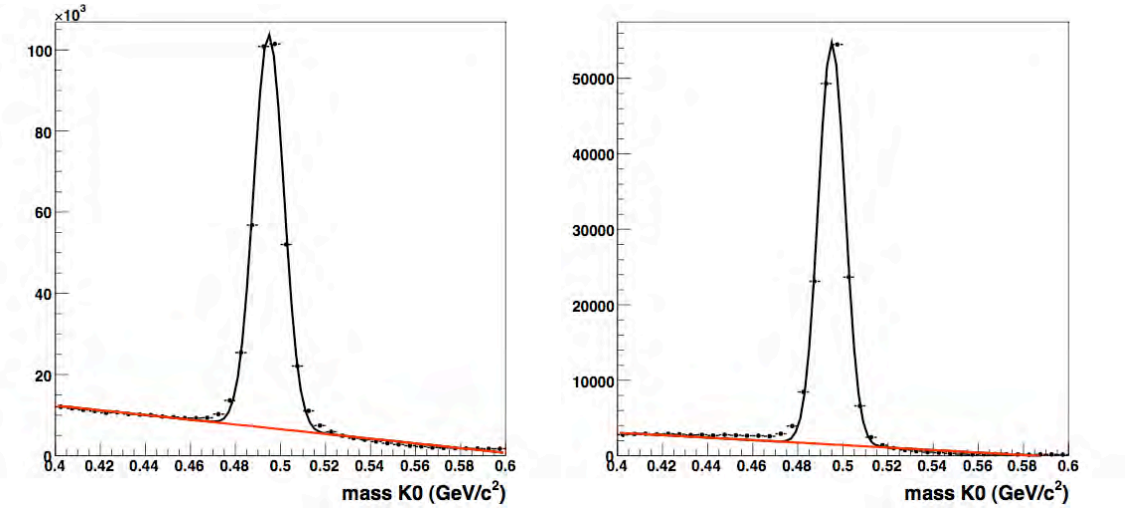


Figure 45: K^0 spectra for the high intensity Cu-Cu run at 200 GeV. The left panel shows the reconstructed K^0s using the TPC alone. The right hand panel the improvement in the signal to noise ratio when the SSD hits are included in the track fitting algorithm.

Figure 46 shows that the SSD improves the momentum resolution of the TPC by a factor of 2 at high p_T without the use of a vertex constraint. As a result, it improves the invariant mass resolution for resonances that decay into multiple charged particles (eg. $\phi(1020)$, Λ). It is important to point out that the improvement in momentum resolution is achieved on a track by track basis and does not require a beamline or vertex constraint to achieve these results.

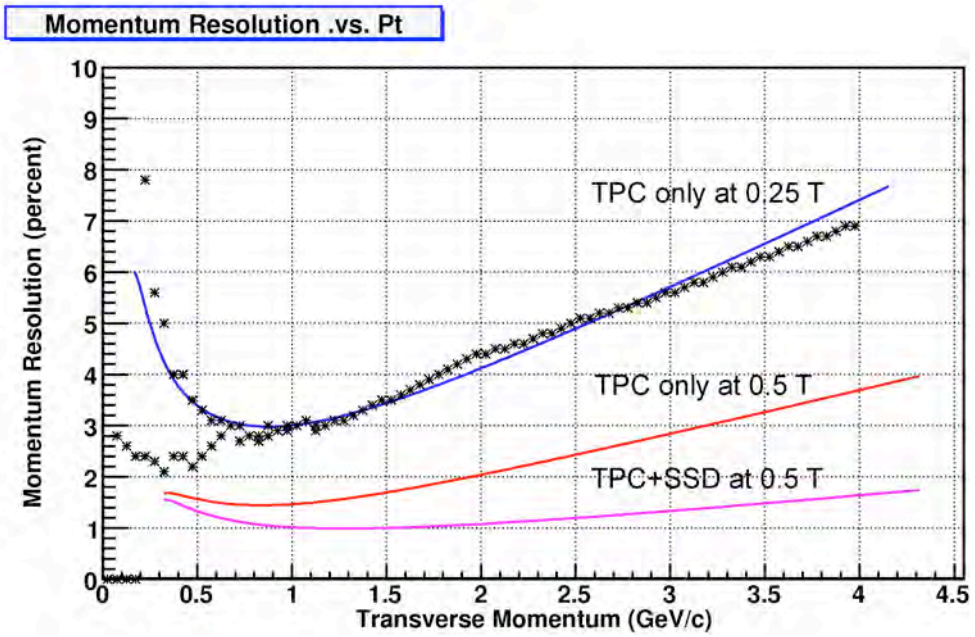


Figure 46: Data compared to simulated momentum resolution of the TPC and SSD detectors in STAR. The data points show a superposition of measured pion and antiproton spectra[33] at 0.25 Tesla in the STAR TPC. The blue line (top) is the simulated 0.25 Tesla p_T spectrum for anti protons, while the red (middle) and pink (bottom) lines show the simulated momentum resolution for the TPC and TPC+SSD at 0.5 T, respectively.

The improved momentum resolution will be useful in our future studies of intermediate to high p_T hyperon production. For example (anti-)Λ production whose longitudinal spin transfer is sensitive to the helicity distribution function of strange quarks in the nucleon[34]. Figure 47 shows a Monte Carlo simulation of high p_T Λ spectra that can be observed in polarized p-p collisions at RHIC. There is a cut on the data to ensure that the Λ decays inside the SSD radius. The simulations[35] show that the width of the peak is improved substantially when the SSD is included in the tracking algorithm. It should be noted that an increasing fraction of Λ's decay at radii larger than the SSD radius as the p_T increases. (The two panels in the figure are different simulations and have a different number of events thrown in each simulation. The reader should focus on the width of the peaks as a measure of the improved quality of the tracking.)

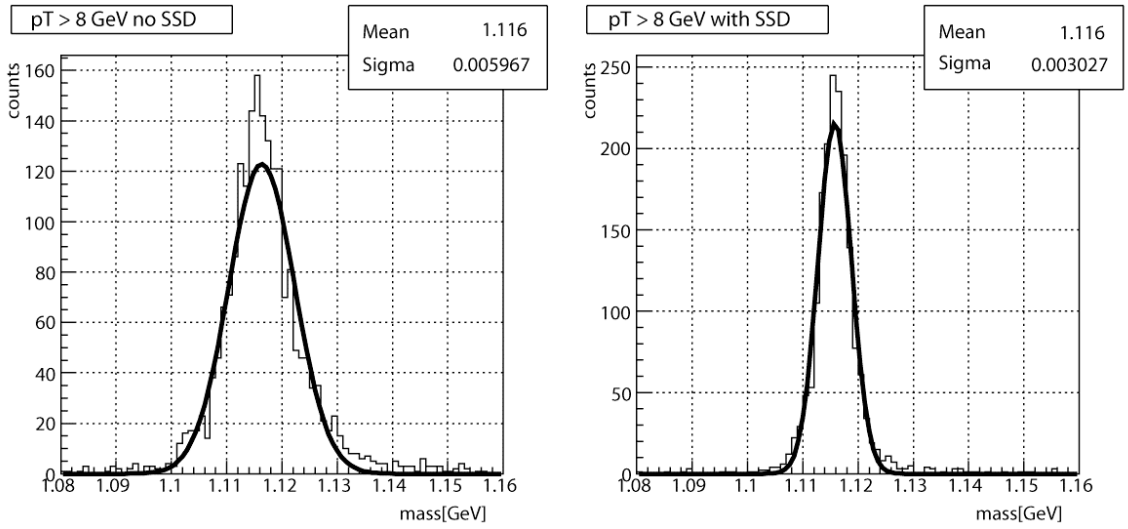


Figure 47: Simulated high p_T Λ spectra using the TPC alone (left panel) or the TPC+SSD (right panel) at 0.5 Tesla. The statistics boxes in each panel document the improved width of the peak when the SSD is included in the tracking algorithm. The simulations were performed by Qinghua Xu.

The SSD is also a relatively fast detector and so it is only sensitive to tracks for 1.5 μs whereas the TPC is sensitive to tracks crossing its fiducial volume for 36 μs. This is important in p-p collisions where multiple events pile-up in the TPC and these piled up events must be distinguished on an event by event and vertex by vertex basis. The SSD can help to resolve the ambiguities due to multiple vertices because there is no appreciable pile-up in a fast Si detector, even for p-p collisions at 500 GeV.

Table 8 shows a self consistent simulation of the pointing resolution of the HFT detector sub-system at various points along the path of a kaon as it is tracked from the outside going in towards the event vertex.

Graded Resolution from the Outside - In		Resolution(σ)
TPC pointing at the SSD	(23 cm radius)	~ 1 mm
SSD pointing at IST	(14 cm radius)	~ 400 μm
IST pointing at PIXEL-2	(8 cm radius)	~ 400 μm
PIXEL-2 pointing at PIXEL-1	(2.5 cm radius)	~ 125 μm
PIXEL-1 pointing at the vertex		~ 40 μm

Table 8: A calculation of the pointing resolution of the TPC+SSD+IST+PIXEL detectors at intermediate points along the path of a 750 MeV kaon as it is tracked from the outside – in. Good resolution at the intermediate points is needed to resolve ambiguous hits on the next layer of the tracking system.

A more detailed look at the resolution of the HFT system is described in the HFT proposal[23] and an updated figure from that proposal is shown in Figure 48. The top panel shows the r-ϕ pointing resolution and the bottom panel shows the z pointing resolution at different places in the system. The beam pipe is included in the calculations. Due to the different geometry of the detectors, the r-ϕ and z resolutions are different in different places but, typically, the average pointing resolution improves for each of the layers at smaller radii.

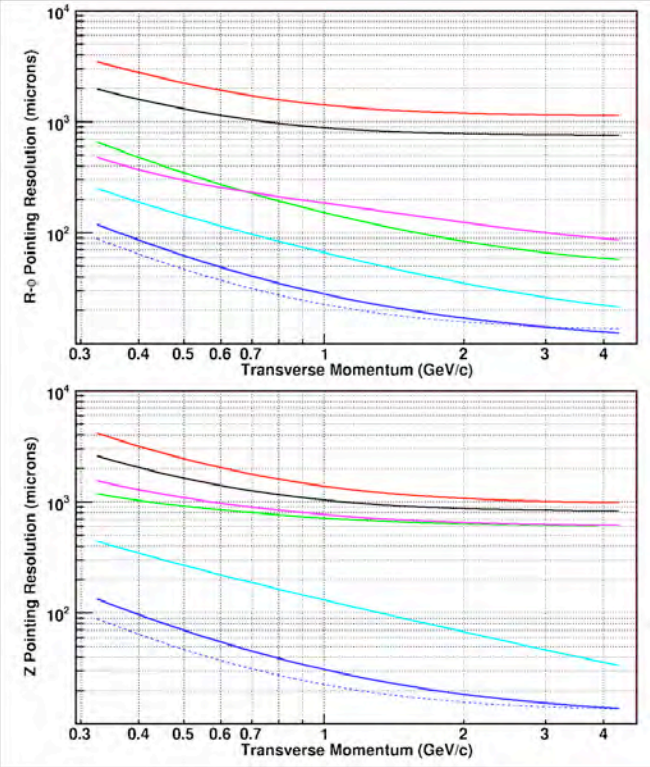


Figure 48: The simulated pointing resolution of the HFT detector system (σ); where the r-ϕ and z pointing resolutions are plotted separately (top and bottom, respectively). The calculations assume a kaon passing through the system. The pointing resolution of the TPC onto the vertex is shown by the red line. The pointing resolution of the TPC onto the SSD is shown by the black line. The TPC+SSD pointing at the IST is the green line. The TPC+SSD+IST pointing at PXL2 is magenta, TPC+SSD+IST+PXL2 pointing at PXL1 is cyan, and the full system pointing at the vertex is blue. The blue dashed line is the theoretical limit; it shows the idealized HFT performance without beam pipe or other sources of MCS except in the PXL layers.

The red line (top) in Figure 48 shows the simulated pointing resolution of the TPC (acting alone) at the vertex, while the black line shows the pointing resolution of the TPC onto the SSD. The pointing resolution onto the SSD is better than at the vertex because the SSD is closer to the TPC.

The remainder of Figure 48 is devoted to showing the pointing resolution of the system at each layer of the system. A detailed examination of the figure shows a pattern of improvement in resolution that reflects the detailed design of each detector. For example, the SSD detector has an asymmetric resolution of approximately 30 μm in the r-ϕ direction and 850 μm in the Z direction. The resolution of the TPC+SSD pointing at IST is shown by the green line in the figures. The r-ϕ and z resolution are also different for the proposed IST detector, as shown by the magenta line, but the figure returns to a simply ordered pattern with the addition of the PIXEL layers because these detectors are symmetric systems with 9 μm resolution in both directions.

The net effect of the increased pointing resolution that is delivered by the SSD is that it increases the efficiency for reconstructing a D^0 meson by at least factor of 2, and probably more when systematic errors are figured into the problem.

In addition, the SSD is also an important element in the alignment and calibration of the TPC because it has different systematic errors than the TPC (e.g. no distortions due to spacecharge or gridleak). It provides an independent measurement to assure that the TPC is operating at its expected resolution. Thus the theoretical efficiencies described above could not be achieved in practice without the extra benefit of the SSD as a calibration device.

4.4.2. Existing SSD Hardware

The SSD will be the outermost layer of the Heavy Flavor Tracker. It is also the only *existing* device to be used in the HFT. It is located at a radius of 23 cm which is mid-way between the PXL layers and the TPC. Its relation to the HFT can be seen in more detail in Figure 43.

The SSD barrel is composed of 20 ladders. The total radiation length of each ladder is approximately 1%. See Figure 49. The ladders are made of carbon fiber and each ladder supports 16 detector modules. Each module is composed of one double-sided silicon strip detector and two hybrid circuits equipped with analogue readout electronics. On both ends of a ladder, two electronics boards are used to control the detector modules and convert the analogue signal which will be sent to readout boards that are located on the TPC end-wheel.

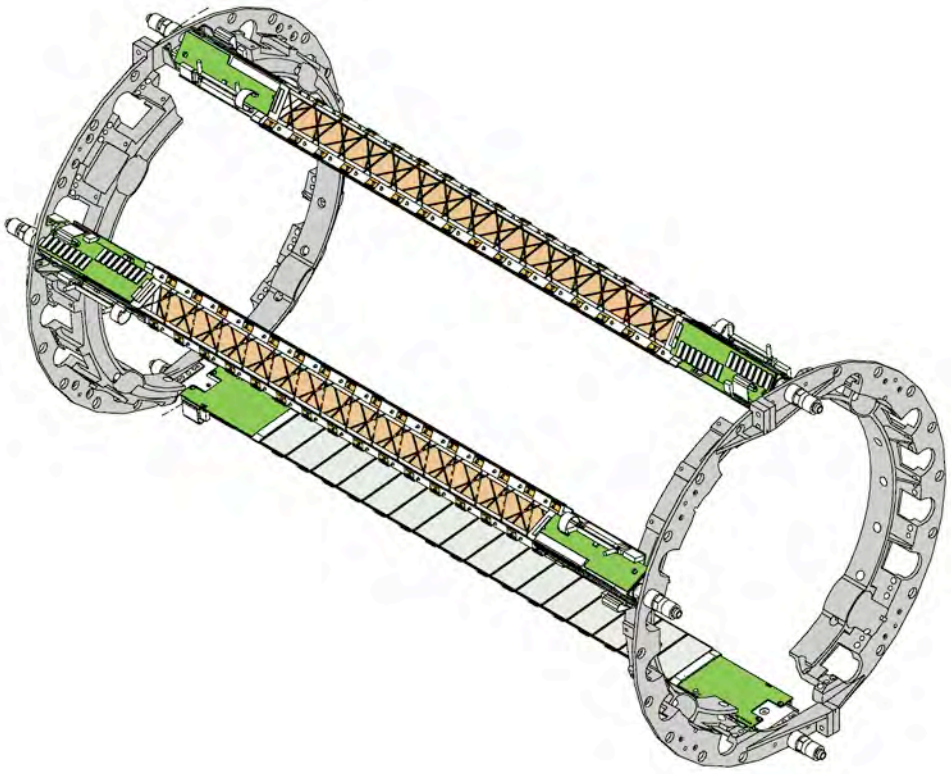


Figure 49: The end-rings for the SSD barrel are shown. The rings split into 4 sectors; the top and bottom sectors support 3 ladders each, while the sectors on each side support 7 ladders each. The complete detector has 20 ladders. In this figure, three ladders are mounted on the barrel at random locations.

One ladder is shown, in detail, in Figure 50. In the existing electronics, two cable busses (one per side of the Si wafers) transport the analog signals along the ladder to a pair of 10 bit ADC boards, which are located on each end. After digitization, the signals are sent to Readout Boards, which are linked to the DAQ system through Giga-link optical fibers.

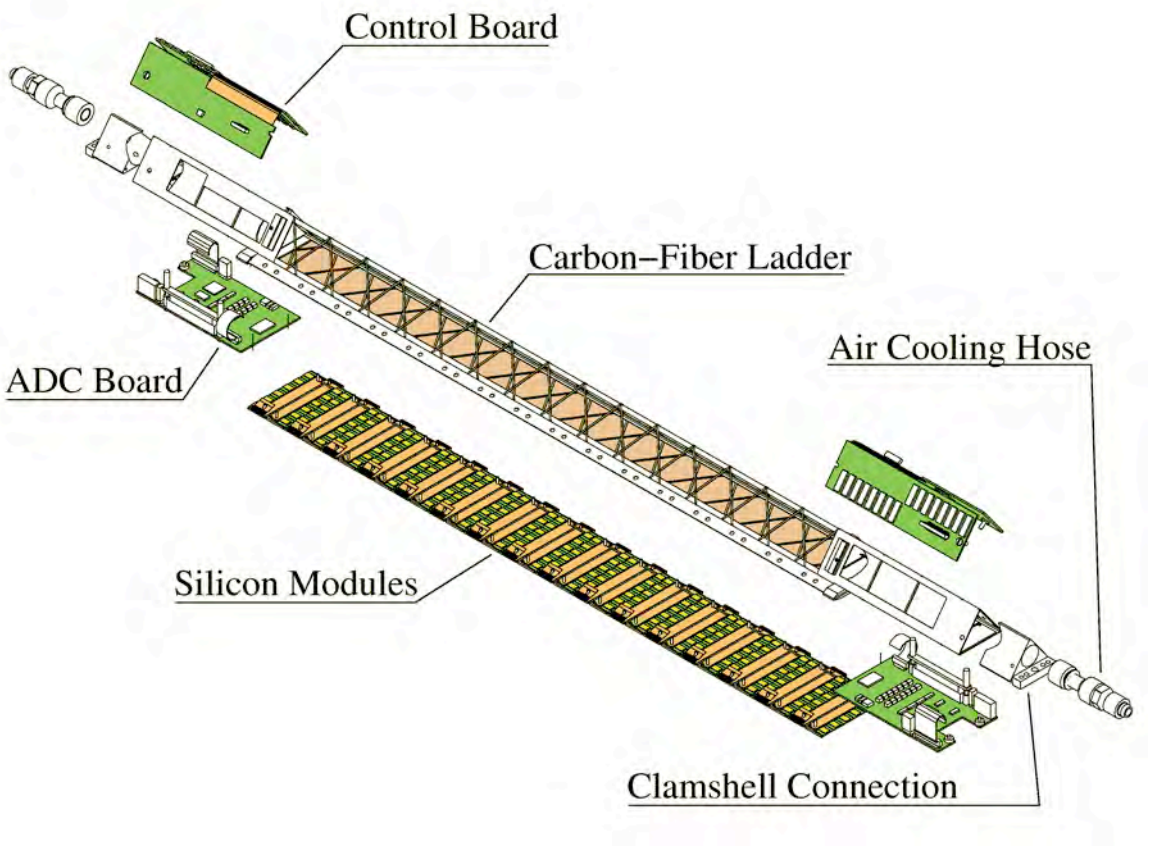


Figure 50: An SSD ladder showing its various components.

A detector module is the basic element of the SSD and it integrates a silicon wafer with its front-end electronics. One detector module is shown in Figure 51. Each module is composed of a silicon detector and two hybrid circuits. A silicon strip detector measures 42 mm by 75 mm and it is doubled sides with 768 strips on each side of the detector. The strips have a pitch of 95 μm, and are crossed with a 35mrad stereo angle between the strips on the P and N side of the silicon.

The two hybrid circuits are built on top of a flexible circuit made of kapton and copper which is, in turn, glued to a carbon fiber stiffener. The circuitry includes 6 analogue readout chips (the ALICE 128C), approximately 50 SMD components (resistors and capacitors) and 1 multi-purpose chip (COSTAR) dedicated to temperature measurements and low and high voltage monitoring.

The SSD is remotely controlled using JTAG for the power settings and temperature readings and also to calibrate and tune the front-end electronics. Each ladder dissipates about 20 Watts of power: 8 watts from the Si wafers and 6 watts from the electronics on each end of a ladder. The total heat dissipated by the system is 400 watts.

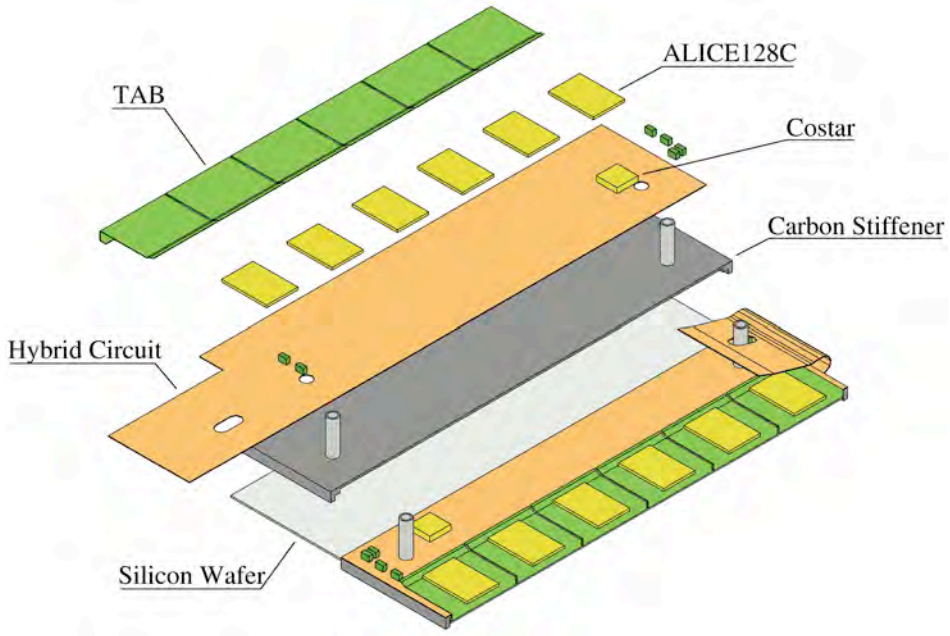


Figure 51: Exploded view of one detector module. It takes 16 modules to fill a ladder.

A schematic view of the electronics readout chain can be seen in Figure 52. The existing SSD electronics is capable of running at 200 Hz and this limit is determined by the availability of ADCs and readout boards. In the existing design, a group of ten ADC boards are daisy chained together to feed one readout board (RDO). Since each of the twenty ladders has two ADCs, a total of four RDO boards are needed to digitize the output of the full detector.

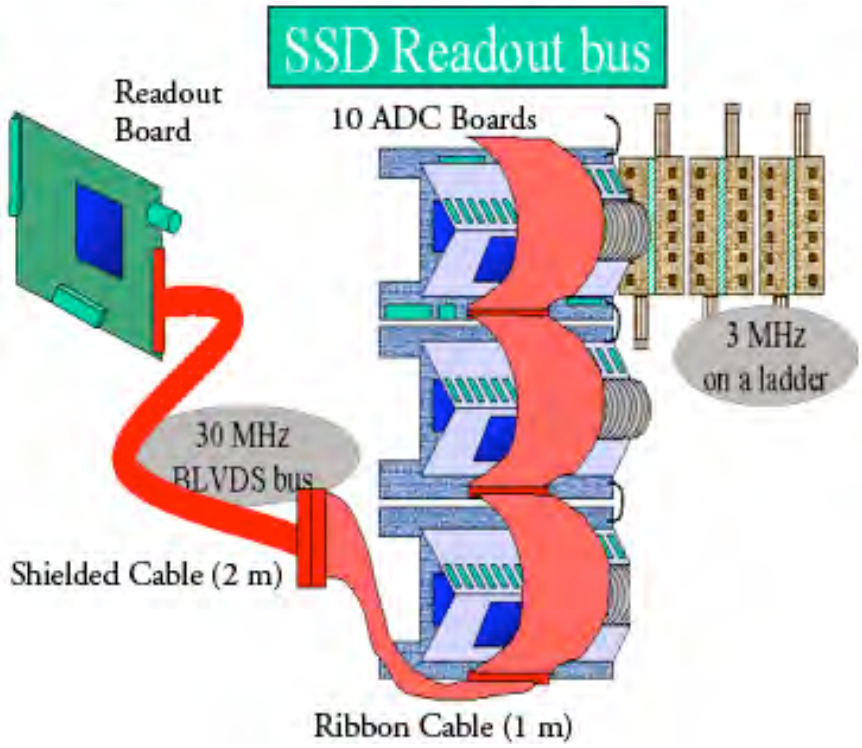


Figure 52: Module layout of the existing electronics (before upgrade).

The existing FEE electronics runs at a 3 MHz clock rate and, because there are 768 strips per wafer and 16 wafers to be read sequentially by a single ADC board, it takes 4.1 ms to read a ladder into the ADC Board. Each RDO runs at 30 MHz and controls ten ADC boards. Therefore it takes a similar time, 4.1 ms, to read out each RDO.

4.4.3. SSD Ladder Status

(Vi Nham)

The SSD detector was stable and used during Run7. At the beginning of the run, several ladders were known to be inoperable. Due to hardware issues, two ladders did not provide useful data and were turned off at the beginning. Four other ladders were not stable when they were operated at the nominal HV configuration, They needed to operated at a lower voltage and therefore were less efficient. During the run, it was believed that there was inadequate cooling. Upon inspection after the run, several kinked cooling hoses were found. When the SSD will be upgraded, the cooling system will be designed so that this problem will not reoccur.

After the run, the SSD was removed and returned to Subatech Laboratory in Nantes. There the engineers tested each ladder and made a few repairs. Their final conclusion was that the SSD could be fully operational with an average of efficiency of at least 93%.

Among the 22 ladders (the 20 ladders that compose the SSD and 2 spare ladders), there are 6 fully good ladders. Eleven ladders have a few hybrid circuits that cannot be fully tested with the Subatech test bench. However the data acquired with these hybrid circuits may be completely usable. It was observed during the last data taking at STAR, that most of them produce good data. Nevertheless, due to some cooling failures and to reduce the heat load, a few of the hybrid circuits were turned off. At this time, it is not possible to give a definitive status of these hybrid circuits. However, a software upgrade is planned to enable testing of these circuits. For a conservative estimate, we assume these hybrid circuits are bad. Using these assumptions, we obtain:

- 7 ladders with one hybrid circuit (out of 32 per ladder) not fully tested,
- 1 ladder with 2 hybrid circuits not fully tested,
- 2 ladders with 3 hybrid circuits not fully tested, and
- 1 ladder with 8 hybrid circuits not fully tested. (This was the first ladder produced so assembly techniques evolved during its assembly.)

In addition, a few inoperable hybrid circuits have been identified in five ladders. During data acquisition, these hybrids circuits had to be bypassed and thus did provide data.

- One ladder had two partially damaged hybrids. One hybrid circuit had one chip (out of 6) dead. The other chip had 5 out of 6 chips damaged. This results in an effective inactive area of one hybrid.
- One ladder with 1 dead hybrid circuit and 2 not fully tested hybrid circuits. If the 2 not fully tested hybrids are considered as bad, this leads to an electronic

coverage of 91% and for data use 81%. It is worthwhile to mention that the two hybrids could provide good data but have not been checked yet.

- Three ladders, known to have frequent HV trip during data taking, have been diagnosed to have some of the modules/hybrid circuits that cause a high leakage current. In that state, the culprit hybrid circuits are disconnected. This leads for 1 ladder with 2 hybrid circuits off, another ladder can also be used with 4 hybrid circuits turned off, and the last ladder is operational with 2 modules turned off. In addition, some chips are missing (5 in total) and 1 hybrid circuit is not operational.

A repair of some of the ladders is under investigation. Figure 53 shows a thermal image (right) of the hybrid circuit with high leakage current. The leakage current has been identify to come from the hot spot which is at the location of a capacitor. It may be possible to replace these capacitors and return the hybrid to a working state However this procedure is a delicate operation and needs some special tooling.

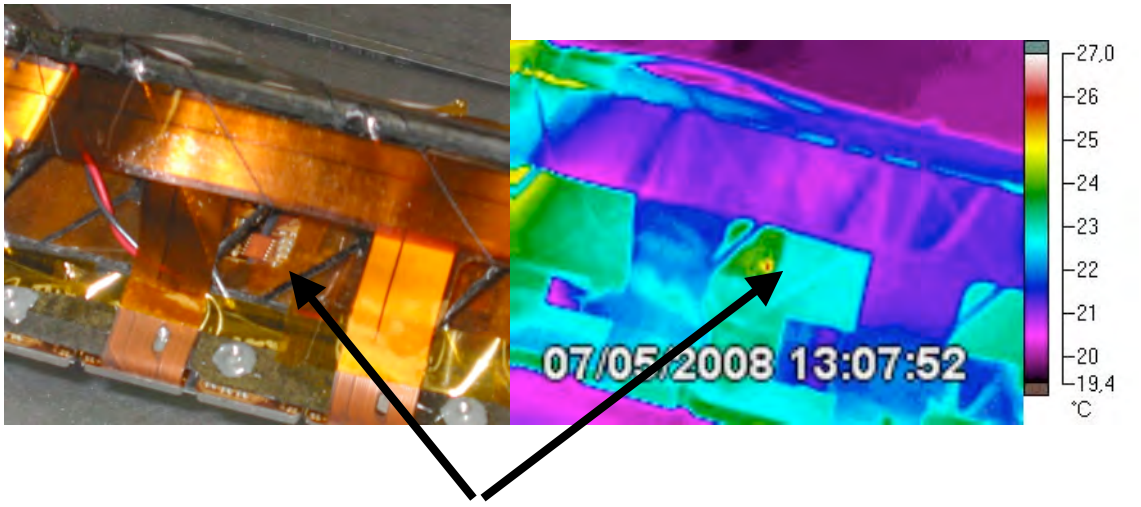


Figure 53. Left: photograph of the hybrid. Right: infrared image of the same hybrid. An arrow points to the capacitor on the left and another shows the hot spot on the right. As the hot spot is at the same position of the capacitor, we conclude that the capacitor is operating at a high current (several 100 μA) and is therefore leaking.

Figure 54 shows a summary of the current status of the best twenty ladders is detailed. It assumes that the hybrid circuits that cannot be fully tested are bad. This figure shows the lower limit of the active coverage. The red marker represents the electronic coverage for each ladder. Since the SSD tracking software has been designed to use both the p and n side to determine a particle's position, one single side hybrid failure will result in the whole module being declared unusable. The blue triangle marker in Figure 54 shows the active area taking into account this effect. The average coverage is represented by the blue dotted line. If the leaking capacitors can be removed, the overall coverage would reach 94%. This is represented with blue solid line.

It is worthwhile to note that only one side of the module can detect a particle when the other hybrid of the module is not operational. This change would degrade the spatial resolution, but it would increase the spatial coverage to 99%. Studies are needed to determine whether this change to STAR tracking is significant.

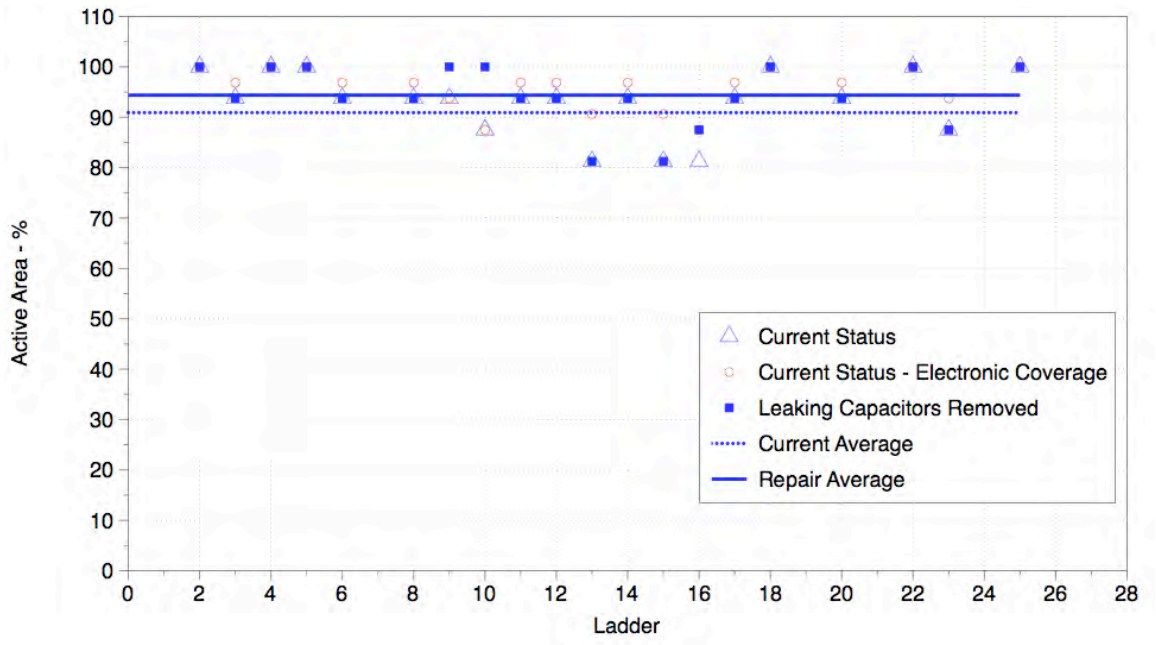


Figure 54. The percent active area of the SSD at the present and with the proposed removal of the leaking capacitors. The curves are explained in the text.

4.4.4. SSD Upgrade Design

4.4.5. Silicon description

4.4.6. Digitization of the data at the end of the ladder

4.4.7. Slow Controls

4.4.8. Power

4.4.9. DAQ1000

4.4.10. Cooling

4.4.11. SSD Upgrade

The current speed of the SSD system is too slow to meet the TPC DAQ1000 specifications so it will be necessary to upgrade the SSD DAQ and RDO system to ensure that it is a viable detector in the future and a good partner for the HFT.

The silicon wafers can be reused, but the readout electronics on each end of the ladders must be upgraded. In addition, the cooling system that has been in use for the SSD has proven to be inadequate, and has been removed. A new cooling system must be designed and installed.

Upgrade plans for the SSD electronics

The present SSD readout is limited to slightly more than 200 Hz trigger rate due to a number of factors. The ADCs which digitize the signals from the modules are limited in sampling rate, and each ADC is responsible for an entire ladder (16*768 samples). The fiber link to the DAQ receiver board is limited to 1 Gb/s (120 MB/s), and the data are required to be formatted in a somewhat inefficient way in order to be compatible with the existing DAQ TPC receiver boards.

The upgrade addresses these issues as follows:

A ladder will be digitized by 16 ADCs in parallel
TPC receiver cards are not used, removing the backward-compatible formatting constraint
The readout board (RDO) will perform zero suppression, reducing the data burden on the fiber link to DAQ

Multiple event buffers will exist on the RDO, reducing effective dead time due to the bandwidth limit of the DDL fiber link.

ADC and connection cards

The new electronics architecture reads the ladder modules in parallel. New ADCs, each reading a single module, sampling at 5 Msps, are read out in parallel and brought to the readout card via an optical fiber pair.

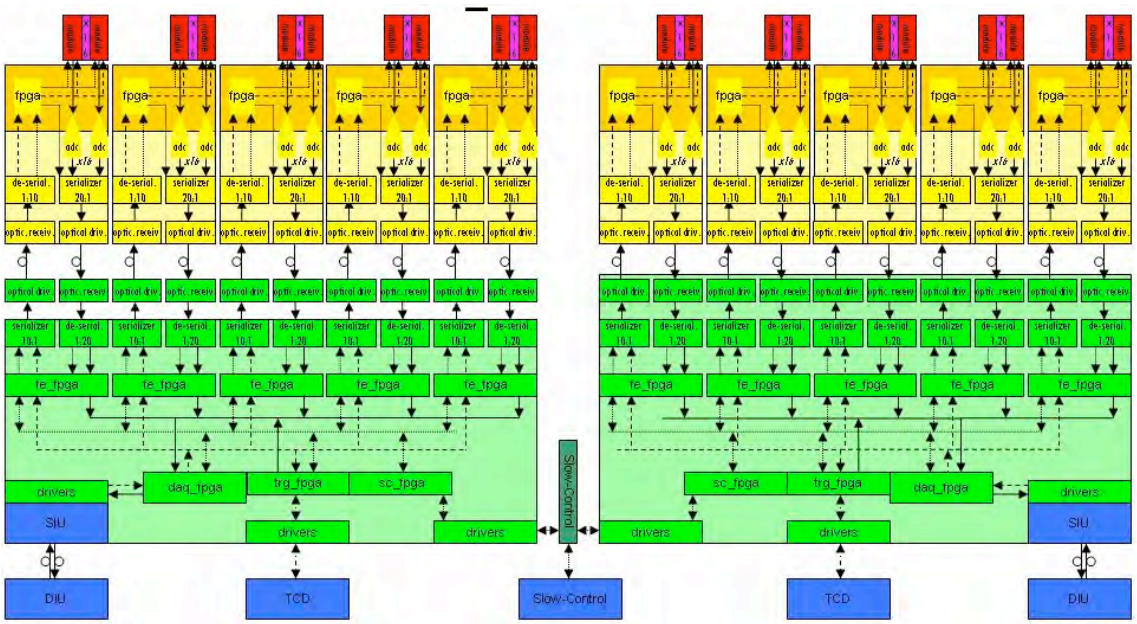
A readout card accepts 5 such fiber optic inputs; it is responsible for 5 ladders. A readout card is connected to the DAQ SSD PC by a DDL fiber link (160 MB/s) identical to those in use in the TPX. Four readout cards reside in a 6U crate. A readout crate is associated with each end of the SSD; there are, therefore, 8 fibers connecting the readout crates to the DAQ computer. The DDL links, together with their source interface to the SSD RDO and the PCI-X card residing in the SSD DAQ PC, are available through the ALICE collaboration.

The redesigned connection card will deliver the payload from each module to one of the 16 inputs of the ADC card. The ADC card contains 8 Analog Devices AD7356 dual ADC chips. Each chip contains two independent ADCs with 5MHz sampling rate and a bit-serial output. The serial output produces a 14-bit pulse train, of which only 10 bits are useful in this application. [The remaining bits will disappear in the RDO.] The outputs of the 16 ADCs are sent to the inputs of a parallel-serial converter, along with the slow control output of the FPGA. The parallel signals are clocked in to the serial converter at a 70MHz rate, resulting in a 1.4 Gbps pulse train, which is converted to optical and transmitted to one of the 5 inputs of the RDO board. The optical nature of this connection allows the RDO crate to be relocated outside the STAR magnet, since cable length is no longer a constraint. The cable cross section is also reduced from the twist-and-flat cables used previously.

The optical connection is bidirectional; the second fiber runs at a reduced clock rate since its purpose is to provide slow control information to the FPGA on the ADC card, which manages the analog circuitry on the ladder.

RDO card

At the RDO card, the 1.4Gbps bit train is converted by a deserializer to a 20-bit wide data path which is updated at a 50 MHz rate. The 1.4 Gbps pulse train is composed of 10 bits of data accompanied by 4 idle tokens, so the deserializer output is updated only at 50 MHz.



Sixteen of the 20 bits produced by the deserializer are delivered to a second bank of 16 10:1 deserializers, resulting in 16 10-bit wide replicas of the original ADC values produced on the ADC card. [The remaining bits are used for the slow control function.] This second bank of deserializers is contained in an array of 5 FPGAs, each one dedicated to the data delivered by the fiber from a single ADC card. These FE-FPGAs perform zero suppression and multi-event buffering on the 16 data streams produced in the last bank of deserializers.

The multi-event buffers and zero suppression both provide a means to reduce dead time due to data burden on the DDL optical fiber. Zero suppression provides the additional benefit that it relieves the SSD DAQ PC of the chore of having to find the above-pedestal strips. Delivering the unsuppressed data to the PC can result in a heavy computing and memory-access load on the PC, which may limit the number of DDL fibers which it can host, since the ADC value for each strip has to be extracted from the word in which it has been stored along with 2 other ADC values, pedestal subtracted, and possibly written back to memory. These steps become unnecessary if the data are zero suppressed at the RDO. When done in the FPGA on the RDO, zero suppression can be accomplished in real time.

Zero suppression is carried out in the simplest possible way: the ADC value for each strip is compared with a stored pedestal value corresponding to that strip. If the ADC value exceeds the pedestal, the strip number and ADC value are encoded into a 32-bit word and entered into the multi-event buffer.

The multi-event buffers are provided as a second means of reducing dead time. Simulation has shown that for randomly spaced triggers 4 buffers can keep the dead time to about 7 per cent for a trigger rate of 1 kHz. We expect about 3% of the strips to be hit in a central Au-Au event. If the SSD modules are sufficiently free from hot strips, the zero suppression technique is to be preferred. However, when there are enough hot strips

in a module, the event size can become excessive, and the multi-buffering provides a fallback technique.

There is sufficient on-chip RAM storage in the FE-FPGAs to implement buffers for 4 events that have not been zero-suppressed. In zero-suppressed mode, these buffers can be coalesced into a single event buffer large enough to handle largest zero-suppressed event.

It is expected that ladder occupancy will be monitored by the operator. When a ladder is observed to be producing large zero-suppressed events, the offending module will be masked off.

The ladders are read out by passing a token to the chain of 6 ALICE128 analog multiplexers handling the analog signals corresponding to the 768 strips of a single module. Once this process has started, it must continue until the token reappears, at the end of 768 clock cycles. In the event of an abort arrival, the clock speed will be doubled in order to minimize the time consumed by this process.

Slow control interface

The existing slow control system is based on software running on a VME-based Power PC running VxWorks. The CPU is obsolete and the VxWorks system is becoming more difficult to maintain.

In the upgraded system the slow control information to and from the ladders travels over the optical fibers to the readout cards. Each readout card forwards these data and commands via the DDL link to the host PC associated with that readout card. Thus the slow control master display will have to forward commands to and receive responses from the DAQ PCs. The added load on the PCs is negligible.

The top-level slow controls software generates the GUI and interprets user commands. The change in architecture necessitates a complete revision of this software, no matter which path the information follows, due to the change in organization of the intra-ladder components.

Trigger interface

Each readout card has its own interface to a trigger TCD. The interface will reflect the updated definition of the TCD (still in progress). The functionality of the trigger interface remains unchanged from the present system.

Plans for repair		SB
Upgrade of Electronics		SB
	ADC Board	CR+MJL
	Connection Board	CR+MJL
	RDO Board	CR+MJL
	Fiber Slow control interface	CR+MJL
Cable plant Design		HM + (CR)
	Data fibers	*
	Slow Control	*
	Power (LV, Bias, sense)	*
	Platform	*
Cooling system		JR

4.4.12. Current status

4.4.13. Refurbishing silicon

4.4.14. Upgrade for readout electronics

4.4.15. Design of cooling system

4.4.16. LV and Power

4.4.17. Slow controls

4.4.18. Incorporation into DAQ1000 data stream

4.4.19. Cable Design

4.4.20. Integration Issues

Requirements

Mounting precision JT

Temperature for running VN

Heat Load

The ADC chips selected for the ladders consume very little power (14 ma @ 2.5V). Taking into account the remaining components: FPGA, serializer, deserializer, and optical transmitter and receiver, each ladder's end electronics is expected to consume less than 2W. The existing ladder faces dissipate 6W each, with an additional 8W dissipated by the Si modules. Thus the estimated dissipation for a full ladder is expected to be 12W compared with 20W for the existing system. MJL

Readout Crate Location

The use of optical links between the ladder and readout crates makes the location of the readout crates non-critical. For that reason, it is expected that the crates will be located on the South platform, where space is available.

MJL

DAQ resources needed

The 8 SSD readout cards require 8 DDL fiber links to DAQ PCs. Each DDL receiver card (DRORC) MJL

	handles two fibers; thus, 4 DRORC cards are required to provide the necessary interface. This is best implemented in 2 PCs, each with 2 DRORCs. Each PC will be responsible for one-half of the SSD.	
	Space for cable removal	SB
	Mass of detector	HM + SB
	Mass of cables on cone	HM + SR
Alignment mounts on the Cone		SB
Space Needed		
	Edge of Cone (break out of cables)Cable paths on the cone	CRHM
	Edge of Cone (break out of cables)	CR
	Platform	HM
	Space for coolingSpace allocation in the Racks	JTHM
Interface issues with the FGT	Space for cooling	HMJT
Interface issues with the HFTInterface issues with the FGT		HMHM
Effect on cooling on other detectorsInterface issues with the HFT		JTHM
Effect on cooling on other detectors		JT

4.4.21. Resources for integration

4.4.22. Alignment mounts on the Cone

4.4.23. Cable paths on the cone

The SSD is readout separately on each side of STAR. Each ladder is a separate detector. Therefore there will be 20 cables of each type on both the East and West Cone. As each ladder requires only one HV bias cable, alternate ladders are fed from both the east and west side.

An estimate of the size of the cables is given in

System	Cable Type	#	Diam. mm	Area Rectangular cm^2	Total Area Rectangular cm^2
DAQ and Slow Control	Optical Fiber (dual)	20	3.0	0.1	1.8
Ladder power	Sense (4x AWG 24)	20	6.4	0.4	8.1
	LV (6x AWG 18)	20	8.1	0.7	13.2
	HV Bias (2x AWG 24)	10	4.3	0.2	1.9
Air Cooling	air cooling to end of cone	20	12.7	1.6	32.3
Contingency		0.15			8.6
				Total cm^2	**65.8**

Table 10. The power cables are the same size as the original design.

System	Cable Type	#	Diam. mm	Area Rectangular cm^2	Total Area Rectangular cm^2
DAQ and Slow Control	Optical Fiber (dual)	20	3.0	0.1	1.8
Ladder power	Sense (4x AWG 24)	20	6.4	0.4	8.1
	LV (6x AWG 18)	20	8.1	0.7	13.2

	HV Bias (2x AWG 24)	10	4.3	0.2	1.9
Air Cooling	air cooling to end of cone	20	12.7	1.6	32.3
Contingency		0.15			8.6
				Total cm²	**65.8**

Table 10. SSD Cables on the cone.

4.4.24. Space allocation

4.4.25. Interface with the FGT

4.4.26. Design responsibilities for cables on the cone

4.4.27. Cable breakout out at the cone boundary

4.4.28. Power (LV, Bias, feedback)

4.4.29. Data fibers

4.4.30. Slow Control

4.4.31. Location of the RDO Box

4.4.32. End of Magnet or

4.4.33. Platform

4.4.34. Space on the Platform

4.4.35. Cables from cone to the platform

4.4.36. Rack space

The SSD currently occupies one rack on the South Platform. This rack contains a VME crate, two CAEN power supply crates and two distributions boxes for the HV and power cables. This space will be maintained. The power supplies provides, +2 V, -2 V, and +5 V to the ladder.

The use of optical links between the ladder and readout crates makes the location of the readout crates non-critical. For that reason, it is expected that the crates will be located

on the South platform, where space is available. Therefore sufficient space will be needed for this item.

It will be necessary for the STAR Slow Control system to communicate with the RDO board. Thus an interface will be necessary. At this time a design has not been made. Therefore, we will need space in either the existing SSD slow control VME crate or a nearby one if a different VxWorks operating system is needed.

4.4.37. Cooling

4.4.38. Triggering

4.4.39. Staging Plan

Assembly and Test in Nantes	SB
Test fixtures at BNL	MJL
Three ladder prototype test	HM
Installation of full detector	HM
Schedule Summary	HM

4.4.40. Three ladder prototype test

4.4.41. Installation of full detector

4.4.42. Institutional Responsibilities

Management structure		
	Org chart	HM with HGR
STAR commitment		
	Cooling engineer	
	Digital designer to incorporate slow controls into fiber optical path used for data	
	Slow control software implementer	

Electronic engineering for readout upgrade
Integration
Software responsibility
Design responsibilities for cables on the cone
(Design of system, vacuum or forced air?, how much cooling? What components.)

Collaboration Commitment

Nantes	SB and CR
BNL	

The upgraded electronics design will be handled up to the schematic level by Subatech. At BNL, the schematics will be used to generate board layouts for the various components, and the boards will be fabricated and assembled under BNL responsibility. This will require an engineer and technician for 3 months.

A prototype of all firmware for programmable parts will be provided by Subatech. All upgrades and revisions will then become the responsibility of BNL.

The design and implementation of the cooling system will be the responsibility of a BNL mechanical engineer.

	MJL
LBNL	HM

Management structure

STAR commitment

Resources required

Cooling engineer

Slow control software implementer

Digital designer to incorporate slow controls into fiber optical path used for data

Electronic engineering for readout upgrade

BNL

LBNL

Software responsibility

Other collaboration contributed resources

HFT responsibilities for interface

4.5. Integration into STAR

4.5.1. Cone and support Structure

Overview

West-East Cone

ICS

OCS

Assembly procedure

Assembly area requirements

4.5.2. Beam Pipe

Mechanical

Bakeout Considerations

Support

4.5.3. Services

Summary of Air, Water and Power

Space requirements on Magnet and Platform

4.5.4. Controls

4.5.5. Data Acquisition

4.5.6. SSD

4.6. Software

4.7. Cost and Schedule

5. Resources

6. Appendix 1

6.1. Description of the Pixel RDO System

This document is an extension of the Pixel RDO addendum to the HFT proposal. It is intended to give detailed parameters of the function of the Pixel readout system that will allow for the understanding of the logic and memory and requirements and the functionality of the readout system. We will present the designs of the Phase-1 and Ultimate readout systems under periodic triggering conditions. The simulation of the system response to random triggering of the type expected to be seen at the STAR experiment is ongoing and will be available upon completion. The readout design is highly parallel and one of the ten parallel readout systems is analyzed for each system.

6.1.1. Phase-1 Readout Chain

The Phase-1 detector will consist of two carrier assemblies, each containing four ladders with ten sensors per ladder. The readout is via parallel identical chains of readout electronics. The relevant parameters from the RDO addendum are reproduced in Table 12.

Item	**Number**
Bits/address	20
Integration time	640 μs
Hits / frame on Inner sensors (r=2.5 cm)	295
Hits / frame on Outer sensors (r=8.0 cm)	29
Phase-1 sensors (Inner ladders)	100
Phase-1 sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5

Table 12: Parameters for the Phase-1 based detector system used in the example calculations shown below.

The functional schematic of the system under discussion is presented in Figure 55.

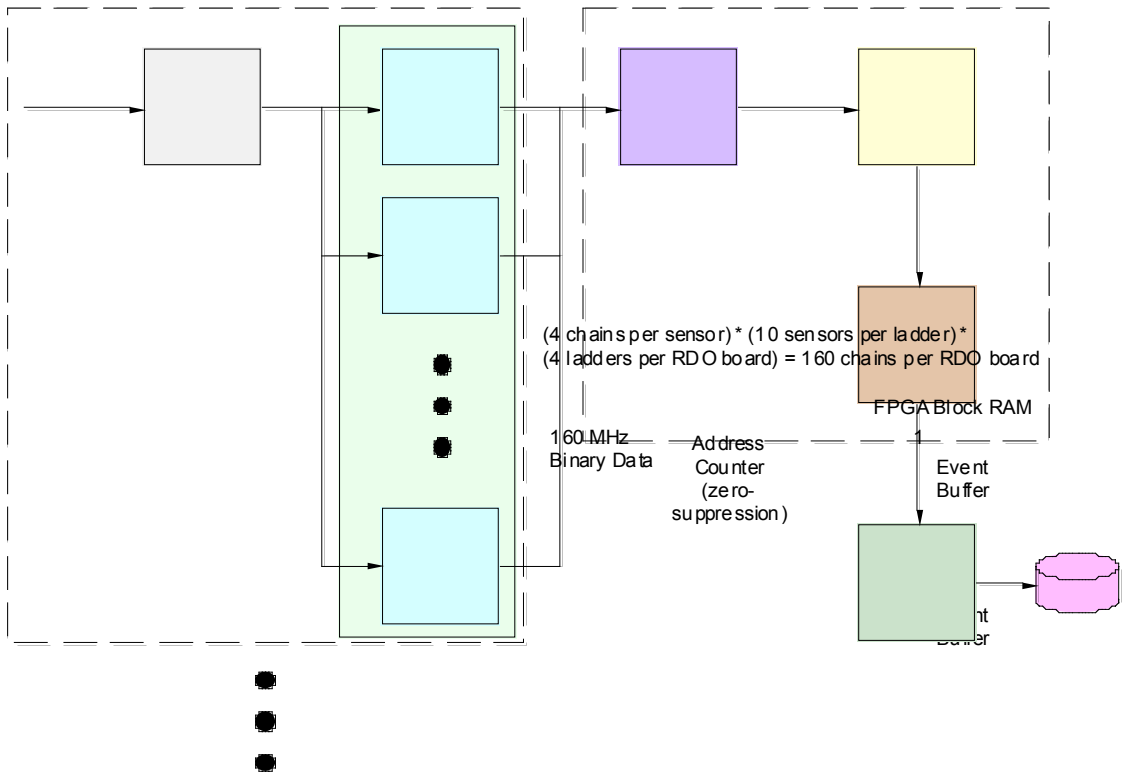


Figure 55: Functional schematic diagram for one Phase-1 sensor based RDO board. Each RDO board services one inner ladder and 3 outer ladders. Each ladder contains 10 sensors.

We will show the system function for two cases. The first is for a periodic trigger rate of 1 kHz. The second is for a periodic trigger rate of 2 kHz. These cases make the scaling clear. In both cases we will use the average (pile-up included) event size. We are currently simulating the dynamic response of the system to the triggering and event size fluctuations seen at STAR and will make this information available after the simulations are completed. It is important to note that the system is FPGA based and can be easily reconfigured to maximize the performance by the adjustment of buffer sizes, memory allocations, and most other parameters. The relevant parameters of the system pictured above are described below;

Data transfer into event buffers – The binary hit data is presented to the address counter at 160 MHz. The corresponding hit address data from the adders counter is read synchronously into the event buffers for one full frame of a 640 × 640 sensor at 160 MHz. This corresponds to an event buffer enable time of 640 μs.

Event Buffers – Each sensor output is connected to a block of memory in the FPGA which serves as the storage for the event buffers. Each block of memory is configured as dual ported RAM and. The overall FPGA block RAM used per sensor output is sized to allow for storage of up to ten average events with event size fluctuation. This leads to a total buffer size that is 20 × the size required for the average sized event (different for inner and outer sensors). The FPGA block RAM will be configured with pointer based

memory management to allow for efficient utilization of the RAM resources. The average inner sensor has 295 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (295 hits) × (20 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 7,375 bits**.** Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each inner sensor output is 73,750 bits or 3,688 20-bit addresses**.

For outer sensors, the event buffer size is calculated similarly. The average outer sensor has 29 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (29 hits) × (20 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 725 bits**.** Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each outer sensor output is 7250 bits or 363 20-bit addresses**.

Data transfer into the RDO buffer via the event builder – This process is internal to the FPGA, does not require computational resources, and can run at high speed. In the interests of simplicity, we will assume a 160 MHz clock to move data in 20-bit wide address words. The event builder first adds a 128 Byte header that contains the trigger ID and other identifying information into the RDO buffer, and then moves the address data from the event buffers into the RDO buffer in 20-bit words. The average carrier event size is [(29 hits / sensor (outer)) × (10 sensors) × (3 ladders) + (295 hits / sensor (inner)) × (10 sensors) × (1 ladders)] × (2.5 hits / cluster) = **9550 address words (20-bit)**. The RDO buffer is 5 × the size required for an average event and is thus **955 kb** in size. The full time required to transfer the address data into the RDO buffer (in 20-bit per clock transfers) is then **59.7 μs**.

Data transfer from the RDO buffer over the DDL link – The RDO buffer is dual-ported and thus readout from the SIU to the RORC can proceed as soon as the RDO buffer begins filling. The data transfer rates for the SIU – RORC combination as a function of fragment size are shown in Figure 56.

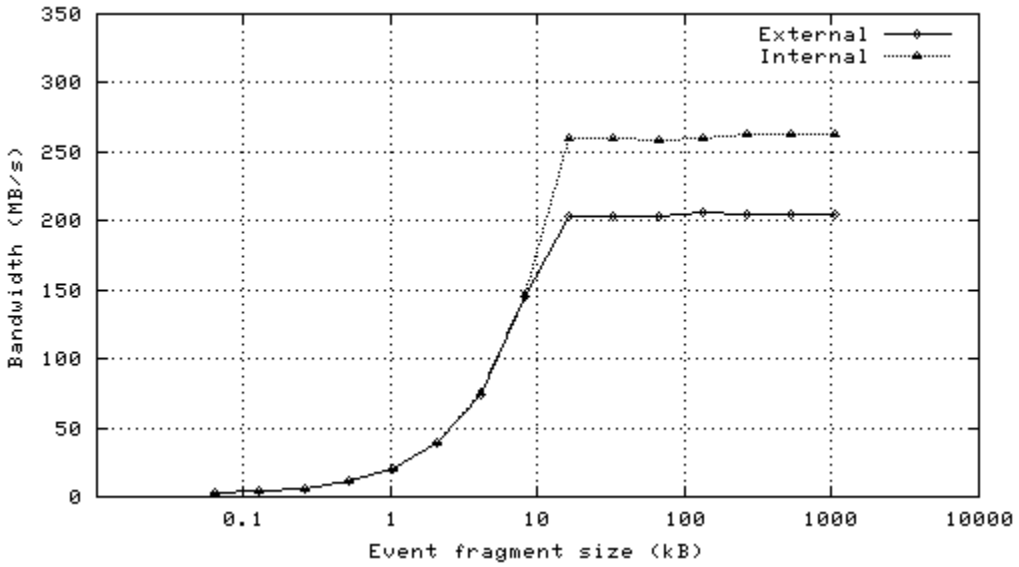


Figure 56: Bandwidth of a single channel of the SIU - RORC fiber optic link as a function of event fragment size with an internal and external (DDL) data source using two D-RORC channels. From the LECC 2004 Workshop in Boston.

In this case, we will assume that we are padding the 20-bit address data to 32-bit word lengths for DDL transfer. The event size is then (32 bits) **×** (9550 address words) **= 305.6 kb or 38.2 kB.** In this example, our transfer rate is ~ 200 MB / s. This transfer then takes **191 μs.**

Data transfer to the STAR DAQ for event building – The event data is buffered in the DAQ PC RAM (>4GB) until only accepted events are written to disk and then transferred via Ethernet to an event building node of the DAQ system. Level 2 trigger accepts are delivered to the RDO system and transferred via the SIU – RORC to the DAQ receiver PCs. Only the events that have been accepted by level 2 are then built into an event. In this way, the buffer provided by the DAQ PC RAM provides for the elasticity needed for an average event acceptance of 1 kHz

The results of these calculations and discussion are presented below in the chronograms in Figure 57 and Figure 58.

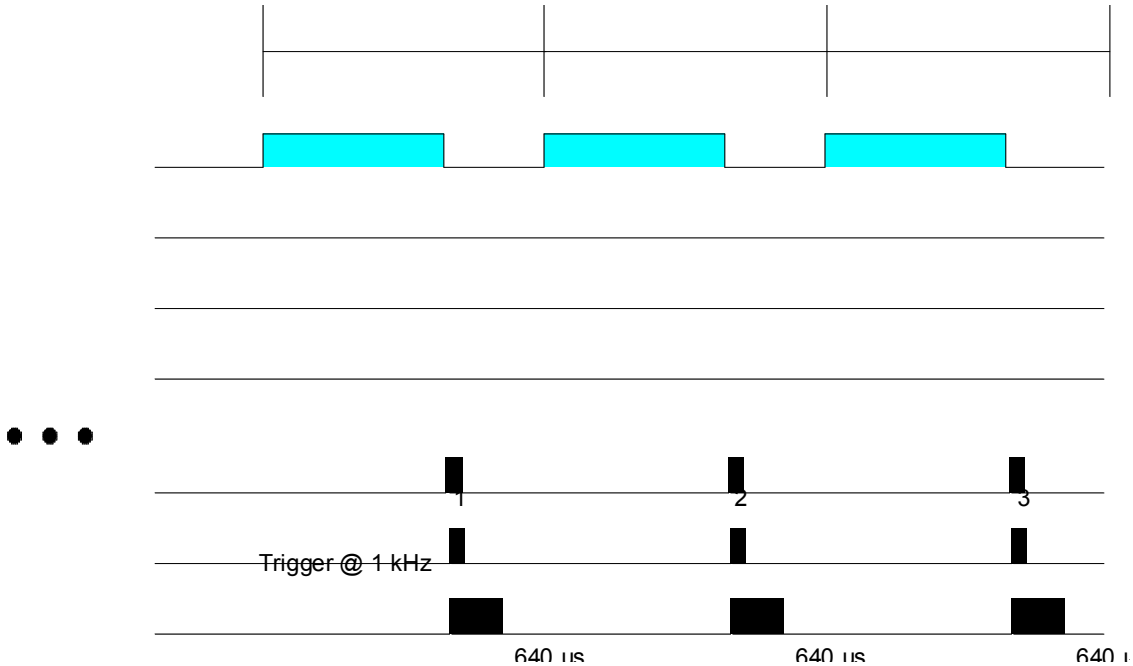


Figure 57: Chronogram of the Phase-1 based readout system functions for a 1 kHz periodic trigger.

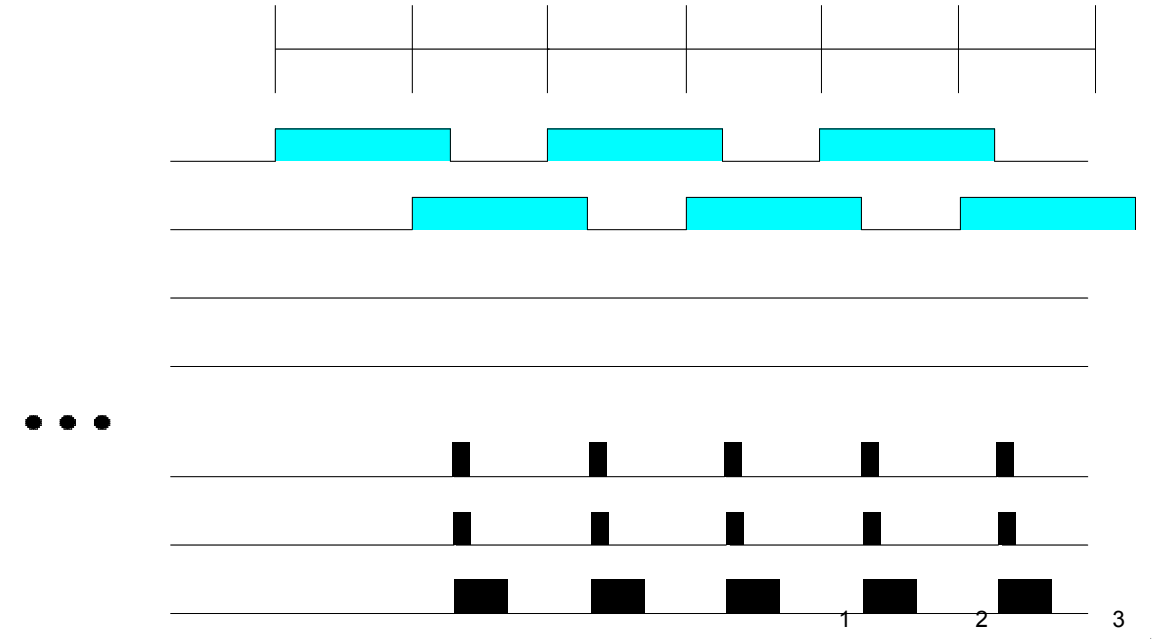


Figure 58: Chronogram of the Phase-1 based readout system functions for a 2 kHz periodic trigger.

The memory resources required in the FPGA / motherboard combination for this readout design are (120 outer sensor readout buffers) × (7.25 kb per event buffer) + (262.5 kb for the RDO buffer) + (40 inner sensor readout buffers) × (73.75 kb per event buffer) + (955 kb for the RDO buffer)= **4775 kb**. The Xilinx Virtex-5 FPGA used in our design

contains 4.6 – 10.4 Mb of block RAM so the entire design should fit easily into the FPGA.

Ultimate Sensor Detector Readout Chain

Again, the Ultimate sensor readout system consists of ten parallel readout chains. The main difference between the Phase-1 sensors and the Ultimate sensors is the inclusion of zero suppression circuitry in the Ultimate sensor, thus only addresses are read out into the RDO boards. In addition, the integration time of the Ultimate sensor is 200 μs and there is one data output per sensor. These differences lead to the functional schematic of the readout system shown in Figure 59.

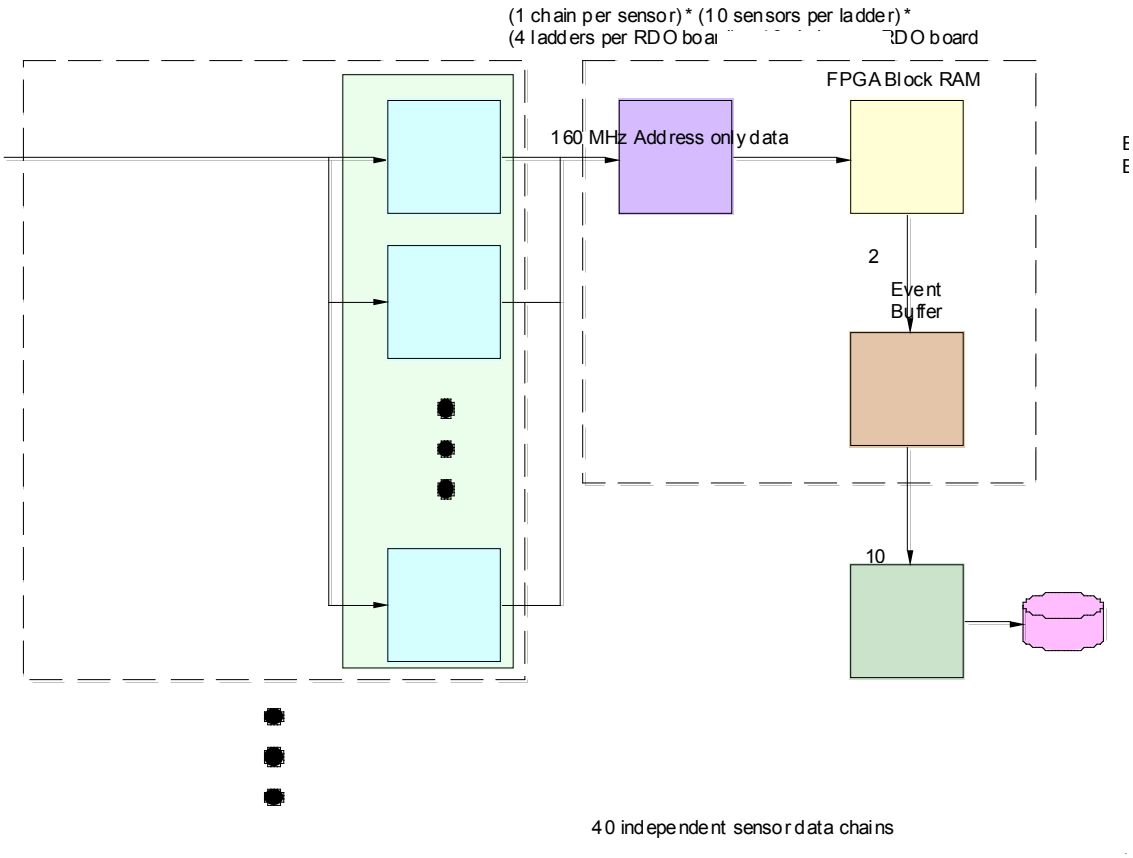


Figure 59: Functional schematic diagram for one Ultimate sensor based RDO board. Each RDO board services one inner ladder and 3 outer ladders. Each ladder contains 10 sensors.

We will show the system function for the same two cases as shown for the Phase-1 readout system. The first is for a periodic trigger rate of 1 kHz. The second is for a periodic data rate of 2 kHz. Again, in both cases we will use the average (pile-up included) event size. The relevant parameters of the Ultimate sensor based system pictured above are described in Table 13.

Item	Number
Bits/address	20
Integration time	200 μs
Hits / frame on Inner sensors (r=2.5 cm)	246
Hits / frame on Outer sensors (r=8.0 cm)	24
Ultimate sensors (Inner ladders)	100
Ultimate sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5
Average Trigger rate	1 kHz

Table 13: Parameters for the Ultimate sensor based detector system used in the example calculations shown below.

Data transfer into event buffers – The 20-bitaddress data is presented to the event buffer 160 MHz. The integration time is now 200 μs giving an event buffer enable time of 200 μs.

Event Buffers – Again, we will calculate the amount of FPGA block RAM required for the event buffering. The average inner sensor has 246 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (246 hits) × (20 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 6150 bits**.** Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each inner sensor output is 61,500 bits or 3,075 20-bit addresses**.

For outer sensors, the event buffer size is calculated similarly. The average outer sensor has 24 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (24 hits) × (20 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 600 bits**.** Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each outer sensor output is 6000 bits or 300 20-bit addresses**.

Data transfer into the RDO buffer via the event builder –We will again assume a 160 MHz clock to move data in 20-bit wide address words. The event builder first adds a 128 Byte header that contains the trigger ID and other identifying information into the RDO buffer, and then moves the address data from the event buffers into the RDO buffer in 20-bit words. The average carrier event size is [(24 hits / sensor (outer)) × (10 sensors) × (3 ladders) + (246 hits / sensor (inner)) × (10 sensors) × (1 ladders)] × (2.5 hits / cluster) = **7950 address words (20-bit)**. The RDO buffer is 5 × the size required for an average event and is thus **795 kb** in size. The full time required to transfer the address data into the RDO buffer (in 20-bit per clock transfers) is then **49.7 μs**.

Data transfer from the RDO buffer over the DDL link – The RDO buffer is dual-ported and thus readout from the SIU to the RORC can proceed as soon as the RDO buffer begins filling. Again, we will assume that we are padding the 20-bit address data to 32-bit word lengths for DDL transfer. The event size is then (32 bits) **×** (7950 address words) **= 254.4 kb or 31.8 kB.** In this example, our transfer rate is ~ 200 MB / s. This transfer then takes **159 μs.**

Data transfer to the STAR DAQ for event building – Again, only the events that have been accepted by level 2 are then built into an event. In this way, the buffer provided by the DAQ PC RAM provides for the elasticity needed for an average event acceptance of 1 kHz

The results of these calculations and discussion are presented below in the chronograms in Figure 60 and Figure 61.

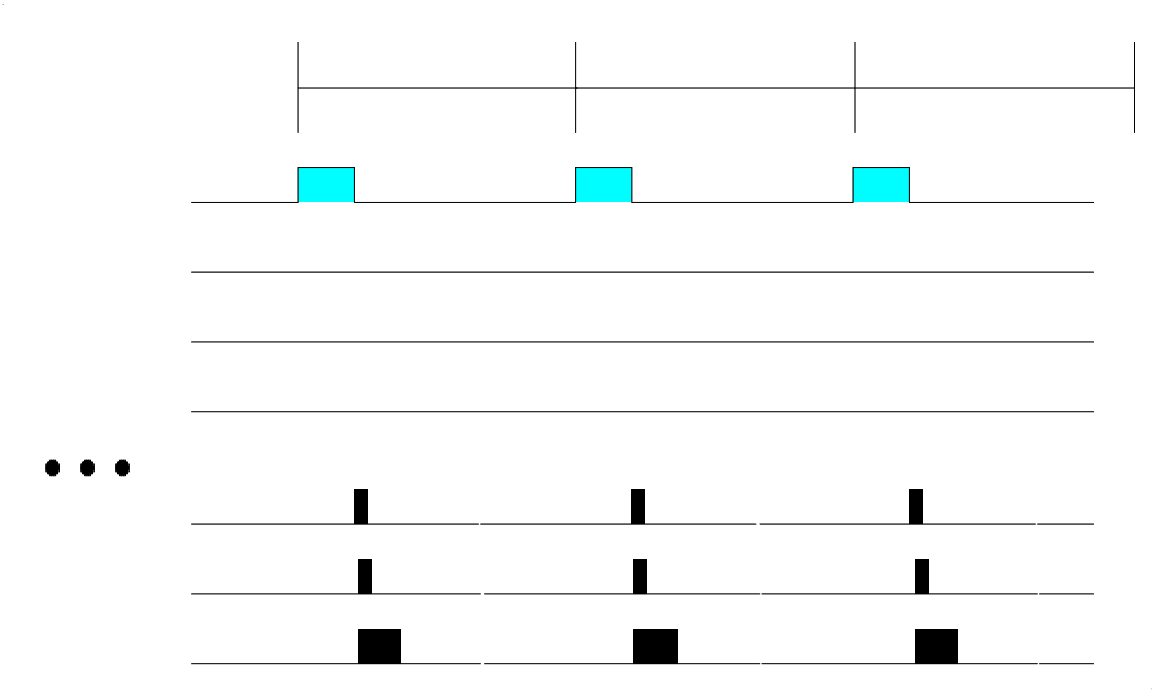


Figure 60: Chronogram of the Ultimate sensor based readout system functions for a 1 kHz periodic trigger.

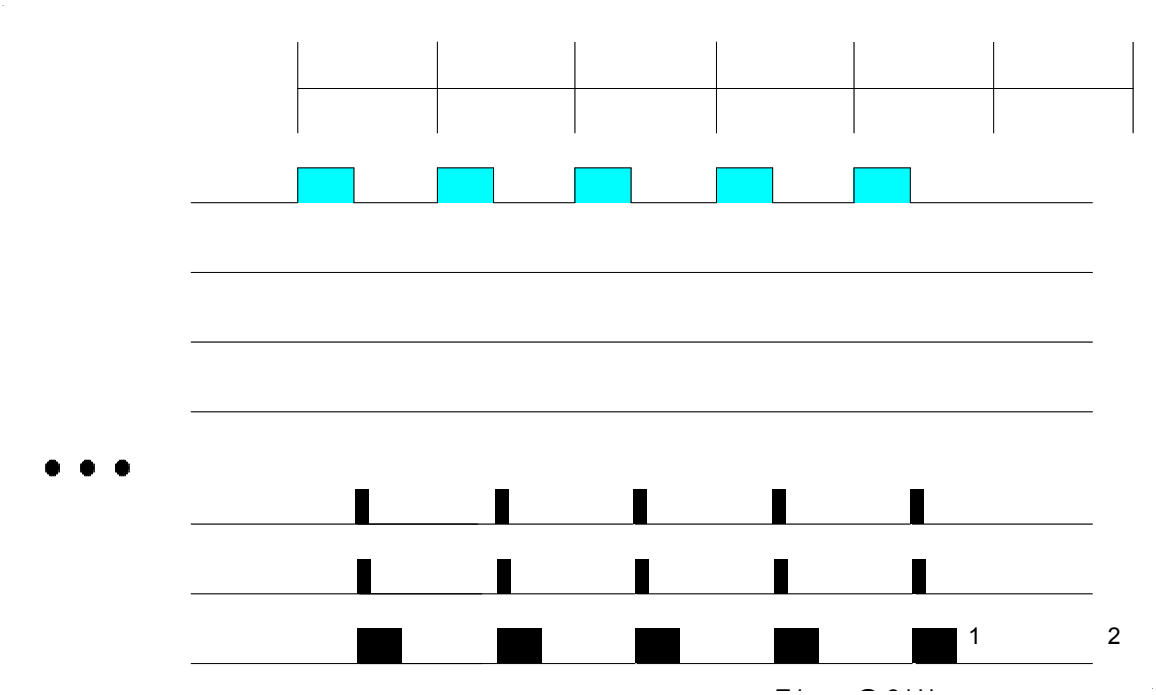


Figure 61: Chronogram of the Ultimate sensor based readout system functions for a 2 kHz periodic trigger.

The system memory resource requirements are somewhat less than those required for the Phase-1 RDO system. This fits easily into the memory resources of the Virtex-5 FPGA.

7. Appendix 2

7.1. Mechanical Design Simulation and Analysis

A number of mechanical design studies have been carried out to find designs that can meet requirements of stability and cooling. The work reported here has been carried out by either ARES corporation or us. These analyses are not complete at this time, but they provide a starting point for prototype work which can be expected to achieve the required performance.

7.1.1. Ladder support Structural analysis

The mechanical design of the pixel support system must meet stringent position stability requirements while also minimizing radiation length. The basic support design analyzed is pictured in Figure 33, but some analysis are also reported for alternative designs that have been considered.

The issues investigated are:

Ladder backing stiffness required to hold thinned silicon flat against it's tendency to curl

Support strength to control gravity sag

Support strength to control deformation from air flow pressures

Control of thermal expansion induced deformation

Control of moisture expansion induced deformation

Support strength to handle insertion loads

Control of Silicon Curl

The pixel chips are mounted on flex cables with a composite backing and these ladders are mounted on a thin large moment carbon composite tubes shown as green in Figure 33. The tubes are the primary source of support and the ladder backers provide support for handling plus these backers must also provide support for the 1 cm overhang of the ladders. In the overhang region the backer provides the only mean for holding the thinned silicon chips flat. Without backing the silicon chips tend to curl as a result of the stresses imposed in the silicon during chip fabrication. A simple analysis shows that a 2 mil thick carbon composite will allow the silicon to curve out of plain by 700 microns. A thicker but less dense backer of perhaps open weave carbon composite that is 10 mils thick will limit the deformation to 30 microns while maintaining a 0.02% X_0 budget for the backer, namely the equivalent of 2 mils carbon composite. This deformation is outside of the 20 microns envelope, but the deformation will be mapped and the stability should satisfy the 20 micron specification.

Control of Gravity Sag

The most critical component for controlling deformation from a variety of sources is the sector tube shown in Figure 33. This structure is in the tracking path and thus requires the most attention to radiation thickness. Analysis of the sector tube control of gravity sag has been carried out by us and by the ARES corporation. The ARES analyses, included details of the composite weave, and showed that a sector tube could be fabricated with a thickness of 120 microns and more than satisfy our 20 micron stability requirement giving a gravitational displacement of less than 6 microns. We have performed a similar analysis, but with an isotropic modulus representation of the composite. This work shows a 5 micron deformation for the detector elements and 35 microns for other parts of the structure, but with the addition of an end lip the analysis gives a gravitational detector displacement limited to 0.6 microns and the maximum displacement of the structure is 4 microns (see Figure 62). These results show that gravity induced distortions are not a problem with this design. As will be shown other contributions to deformation are more significant.

Control of Airflow Induced Deformation

The deformation and vibration induced on the detector support from the cooling air flow requires more study, but preliminary considerations indicate that the current structure could be adequate. The planned cooling air velocity, 8 m/s, has a dynamic pressure

$$p = \frac{1}{2}\cdot\rho_{air}\cdot v^2 = 6\times 10^{-3}\ \text{psi}$$

that acting on the area of the structure is 1.7 times the gravitational force. From the gravity analysis we conclude that the static deformation will be less than 2 microns. Again, vibration studies with prototype structures and possibly computational fluid dynamics (CDF) simulations will be done.

Control of Thermal Expansion Induced Deformation

One of the greatest potential sources of deformation is differential expansion resulting from changes in temperature between powered on and power off. It is planned to spatially calibrate or map the detector structures in a vision coordinate machine with the power off and the structure should not deviate from the map while powered on during operation by more than 20 microns. This requirement was one of the main reasons for choosing the current design with its large moment of inertia and consequently large stiffness. The ladder and beam structure being examined is illustrated in Figure 32 and Figure 33. It was found that the main issue requiring control is the bimetal thermostat effect from differential expansion. The problem is the result of the very large coefficient of thermal expansion (CTE) of the kapton cable compared to the rest of the structure. An analysis of a short section of the ladder shown in Figure 63 illustrates the problem where in this case the thermally induced displacement is 500 microns at the edge of the silicon.

A thermal expansion analysis of ladders plus support shows that by using a very compliant adhesive (3M 200MP) the kapton cable is largely decoupled from the structure greatly reducing the thermal induced bending. Simulation results shown in Figure 64 give a maximum deformation of 9 microns, well inside of the 20 micron requirement envelope.

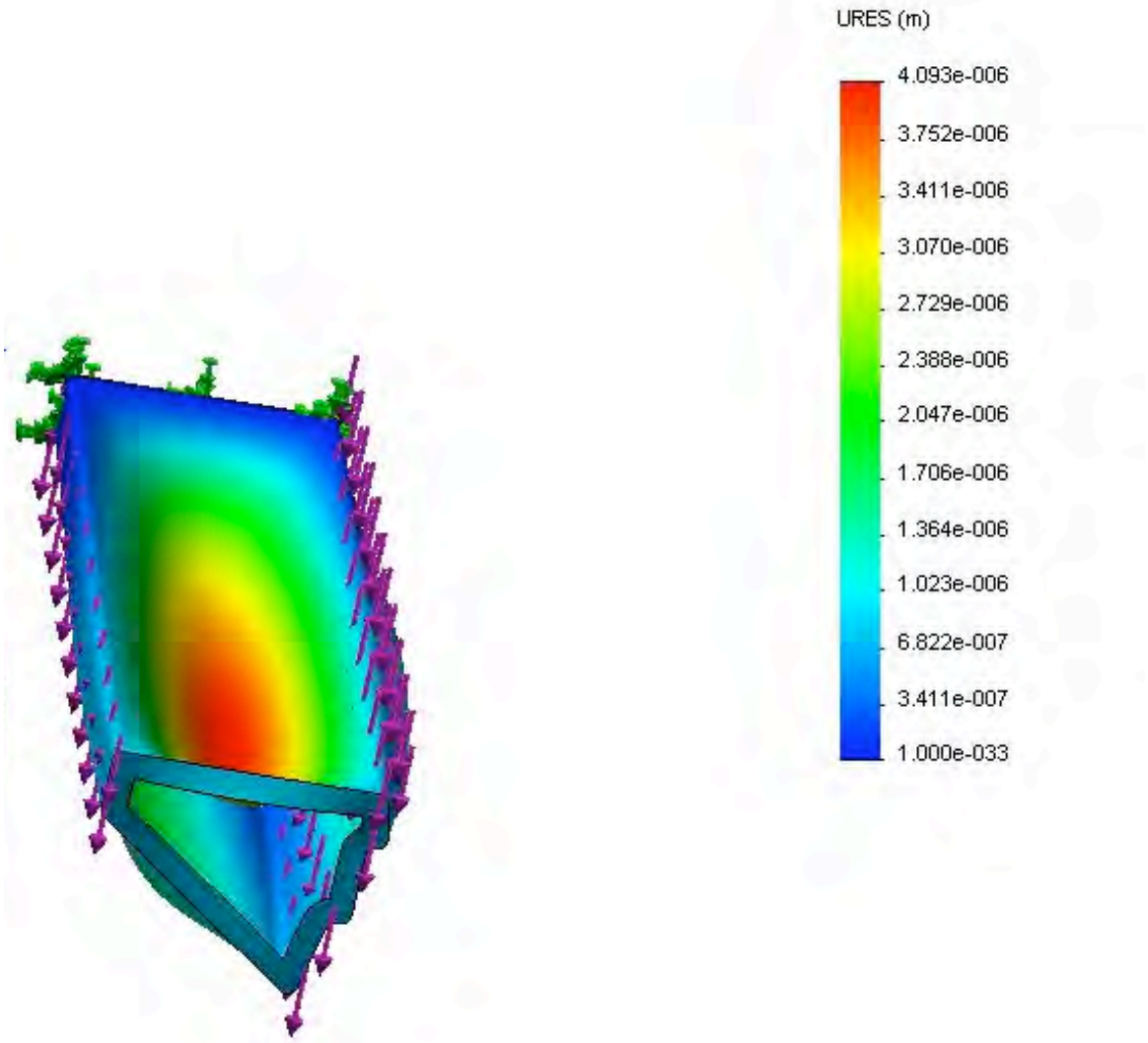


Figure 62 FEA results for gravity deformation of a 120 micron carbon composite support structure carrying 4 detector ladders.

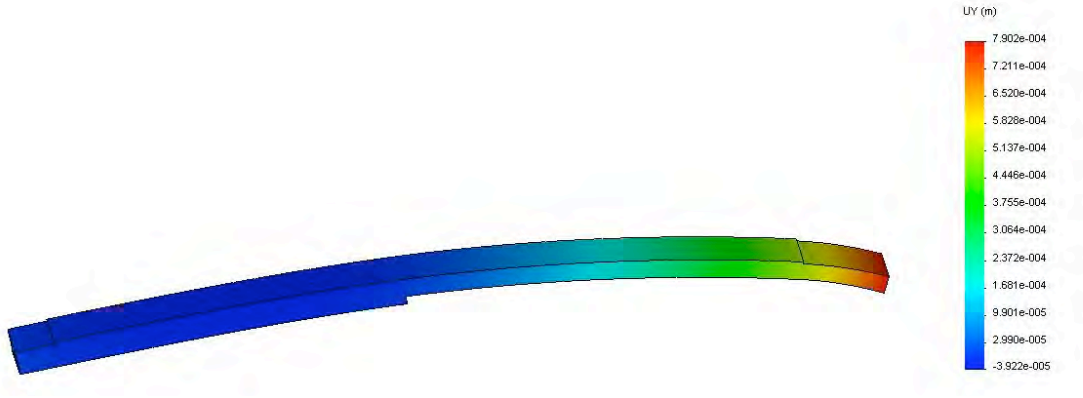


Figure 63 Short section of ladder structure showing problems with excessive thermal bimetal effect bending with using stiff adhesive. The 500 micron displacement resulting from a 20 deg C temperature change is driven by the large CTE of the kapton cable.

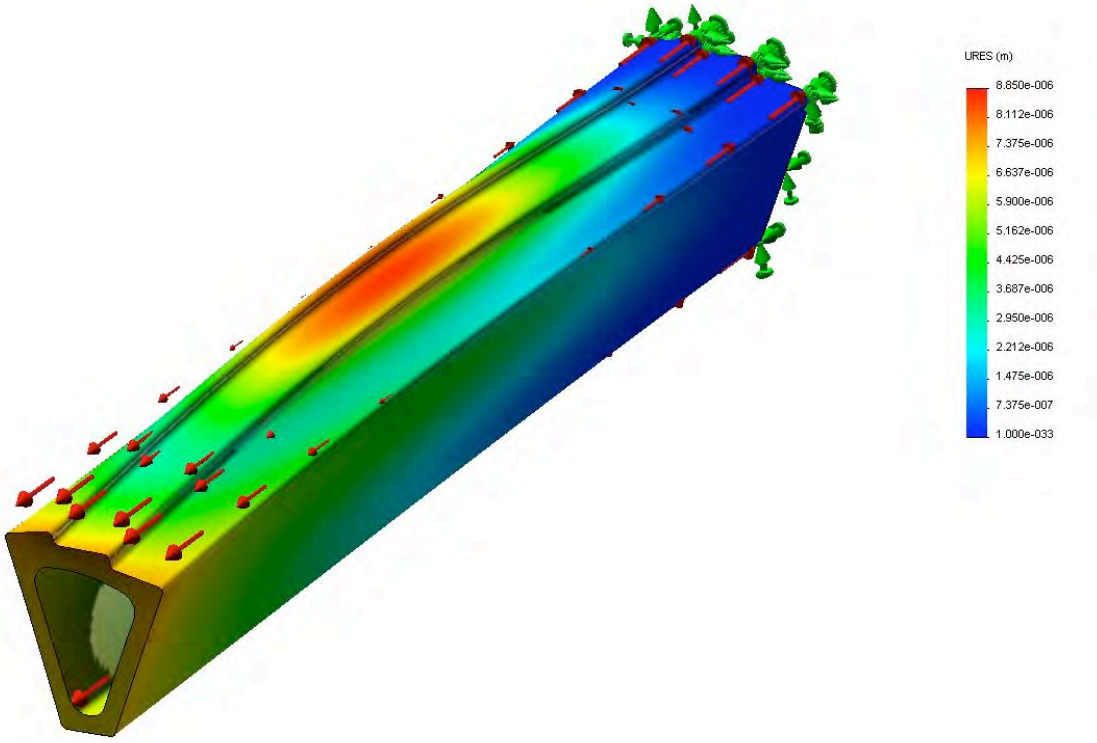


Figure 64 Thermally induced displacement of a sector beam with end reinforcement. The maximum resulting displacement is 9 µm. The beam and end reinforcement is composed of 200 µm carbon composite.

Control of Moisture Expansion Induced Deformation

The carbon composites expand with increased moisture content. There will be a long term reduction in the moisture content from the time of manufacture until completion of

operation in the experiment environment which can potentially lead to unacceptable geometry changes. The ARES Corporation has studied this problem for us and has found a composite layup configuration that meets our 20 micron requirement. This work appears on p. 99 and 102 of their summary report. They recommend a laminate: YSH-50/EX-1515 with a layup: [0, +60, -60]. The FEA analysis gives a maximum displacement of 16 microns. Further analysis and prototyping is required to address this issue. The inclusion of a soft decoupling adhesive may help as it appears to help in the thermal case.

Support strength to handle insertion loads

When the detector is inserted into the final docking position in the center of STAR it engages spring loaded over center latches into the kinematic mounts. The insertion supports have much less stringent stability requirements than the detector ladders since the positioning only has to be good enough to lie inside the kinematic mount engagement window which is ~1 mm, but the support must be able to handle the cocking load of the latches which is on the order of 15 lbs. Displacements must also be limited such that the two half detector cylinders do not collide during the insertion process. A FEA analysis of the supporting hinge structure has been done to check that it is adequate for cocking loads. The results of this analysis, shown in Figure 65, indicate that the design can safely handle the load without undue distortion. The analysis was not done on the latest complete hinge design, but an analysis of one part (see Figure 66) of the latest design shows that it is more than adequate.

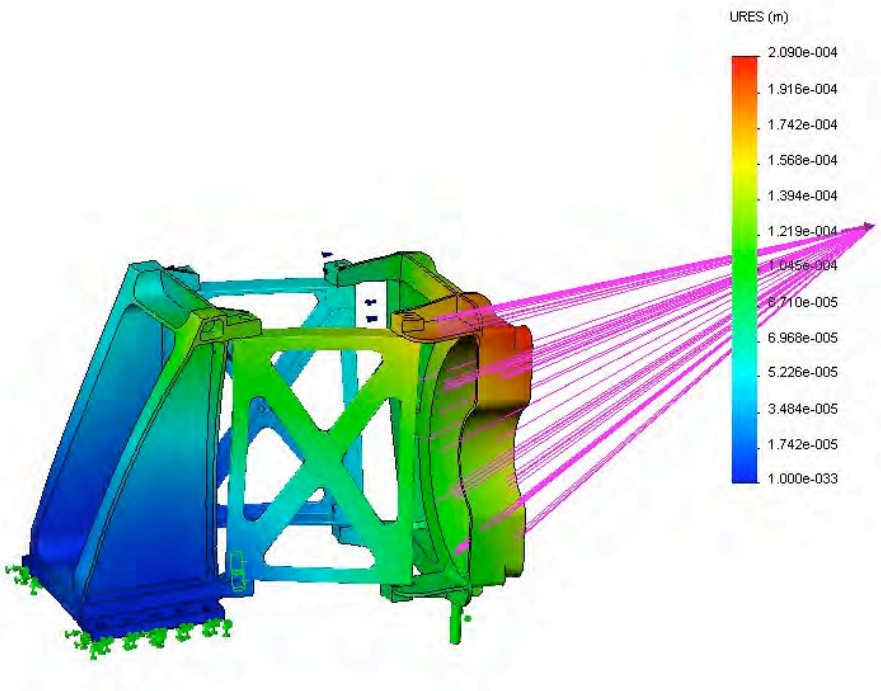


Figure 65 Displacement of an early insertion hinge design under cocking load of the latching mechanism. The displacement in the image is magnified by 140 and the maximum displacement is 210 microns. The pink lines show the position of the remote load as it is carried through the D tube, not shown.

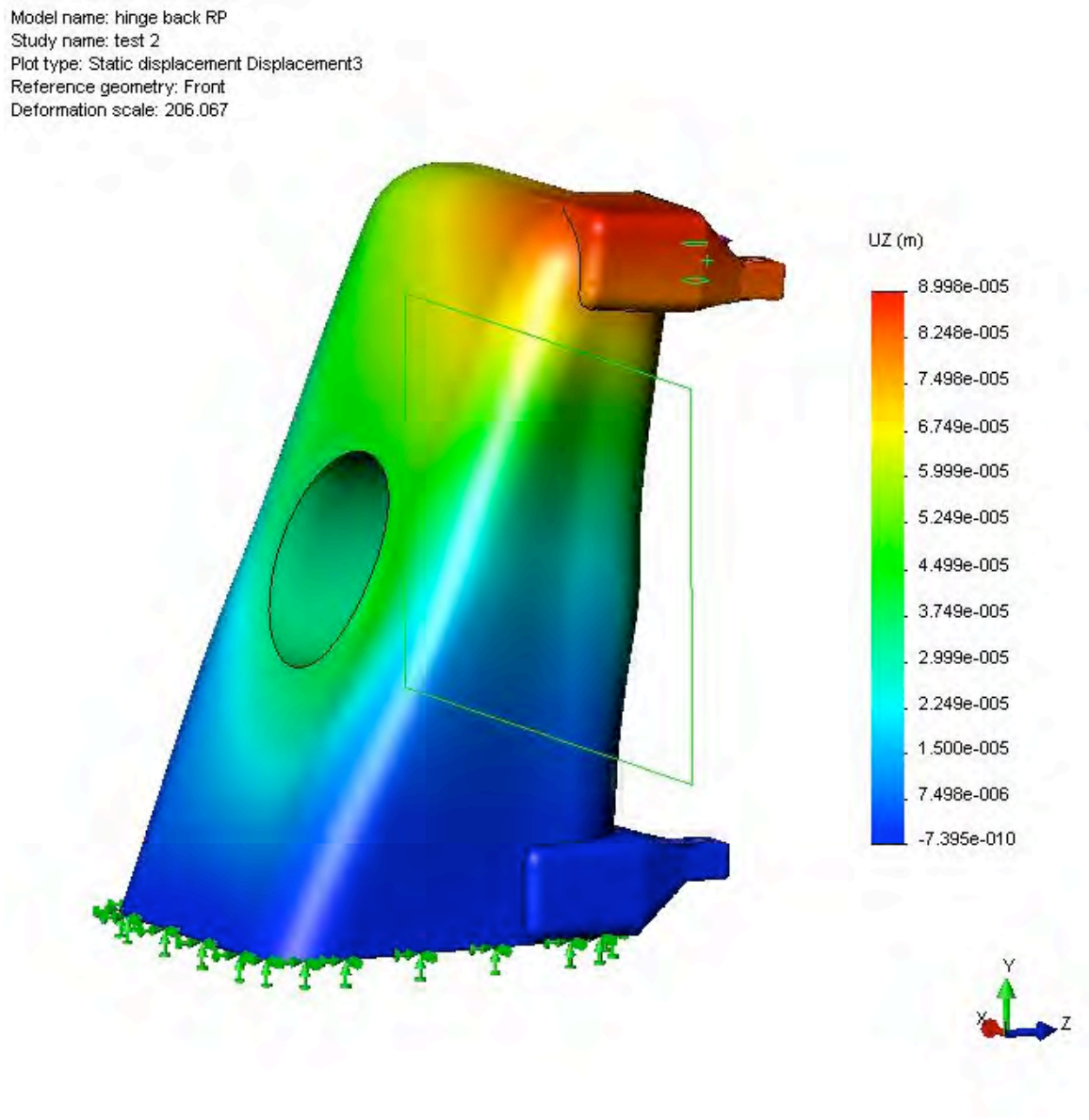


Figure 66 Distortion of support hinge backer under latch cocking load. The flexing in the beam axis direction is 90 microns.

Vibration of STAR central support

In STAR the central inner detectors such as the pixel detector are supported through the OSC and the ISC to TPC end caps. An accelerometer was mounted on the TPC end cap to measure possible vibrations that might couple to the pixel detector and affect position stability. A result from this measurement study (Figure 67) shows the response of a harmonic oscillator as a function of its resonant frequency to vibration if mounted directly on the end cap. This data can be used to set limits on expected vibration of various components and determine whether the performance of the detector is compromised. There are several components of the detector system which each have their own requirements with respect to stability and vibration.

Consider first the vibration of one pixel sector ladder support with respect to the other. This case affects directly the pointing accuracy of multiple tracks to a vertex and therefore the full resolution is required and the vibration should stay below the 9 micron RMS requirement. The fundamental frequency for the sector can be obtained from FEA analysis which gave a 6 micron movement under gravity load. The fundamental

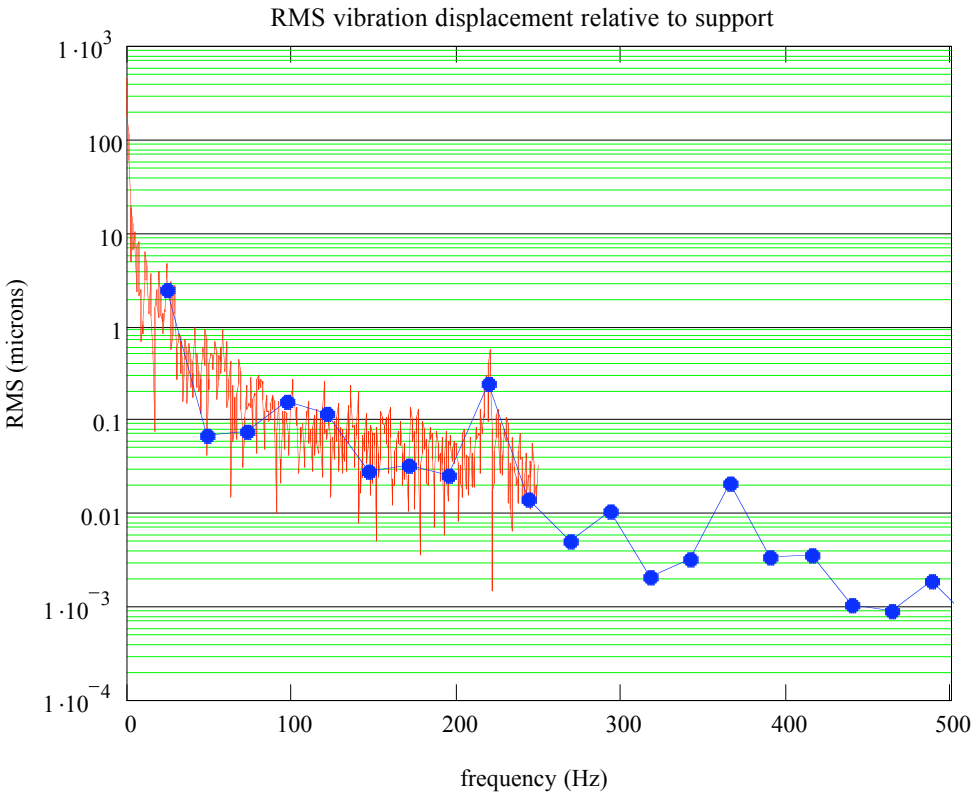


Figure 67 This shows the vibration response of mechanical harmonic oscillator mounted on the TPC end cap as determined with measurements of an accelerometer bolted to the TPC end cap. The two curves represent measurements made using two different methods of recording the data.

frequency is

$$f = \frac{1}{2\cdot\pi}\cdot\sqrt{\frac{g}{d}}$$

or 200 Hz for the 6 micron sag under gravity. From Figure 67 this gives a RMS vibration of .04 microns which is completely negligible compared to our 9 microns requirement. This vibration from this source will actually be significantly less than this because the sector is not directly coupled to the TPC wheel. The less stiff OFC and IFC provide the connection reducing the high frequency coupling.

The next element to consider is the pixel half cylinder as a whole. The stability of this element is most important for track matching from the IST, so the stability of this element should be good enough that it does not compromise the IST pointing resolution, namely it should be less than 100 microns RMS. It is preferable though to be within the pixel limit since there are overlapping pixels between the two half cylinders. The ARES analysis p. 144 gives a fundamental frequency of 110 Hz for the pixel half cylinder when supported on the kinematic mounts. This, according to Figure 67, gives a RMS vibration of 0.2 microns which again is insignificant.

Finally the vibration of the OFC can be checked. The stability of this element only has to be good enough to not compromise the TPC tracking precision which is ~ 1 mm. It is expected that the OFC will be built with a gravity sag of 1 mm or better which was the number for the old support cones that are being replaced by the OFC. The fundamental frequency for this displacement is 16 Hz which according to Figure 67 gives ~ 4 microns RMS vibration. Again, this is not an issue compared to the 1 mm requirement.

7.1.2. Ladder cooling analysis

Air cooling has been chosen for the pixel detector in order to minimize multiple coulomb scattering and a number of studies have been carried out to optimize the air cooling design. Original tests with a heated ladder in a fan driven air stream indicated that ladders with heat loads of 100 mW/cm^2 could be successfully cooled with a moderate air velocity. A study by ARES Corporation, p. 73 found that an airflow velocity of 8 m/s through the sector beam was sufficient to limit the silicon temperature rise above ambient to 13 deg C. To accomplish this however additional cooling fins required under the outer layer of silicon which adds mass and complicates construction.

Bi directional air flow cooling

Since then more extensive, but still preliminary, CDF modeling has been done with air flow over both the inner and outer surfaces of the sector structure. The cooling simulation was run for one sector out of the 10 sectors in the complete pixel cylinder. The air flow path is shown in Figure 39 and Figure 68.

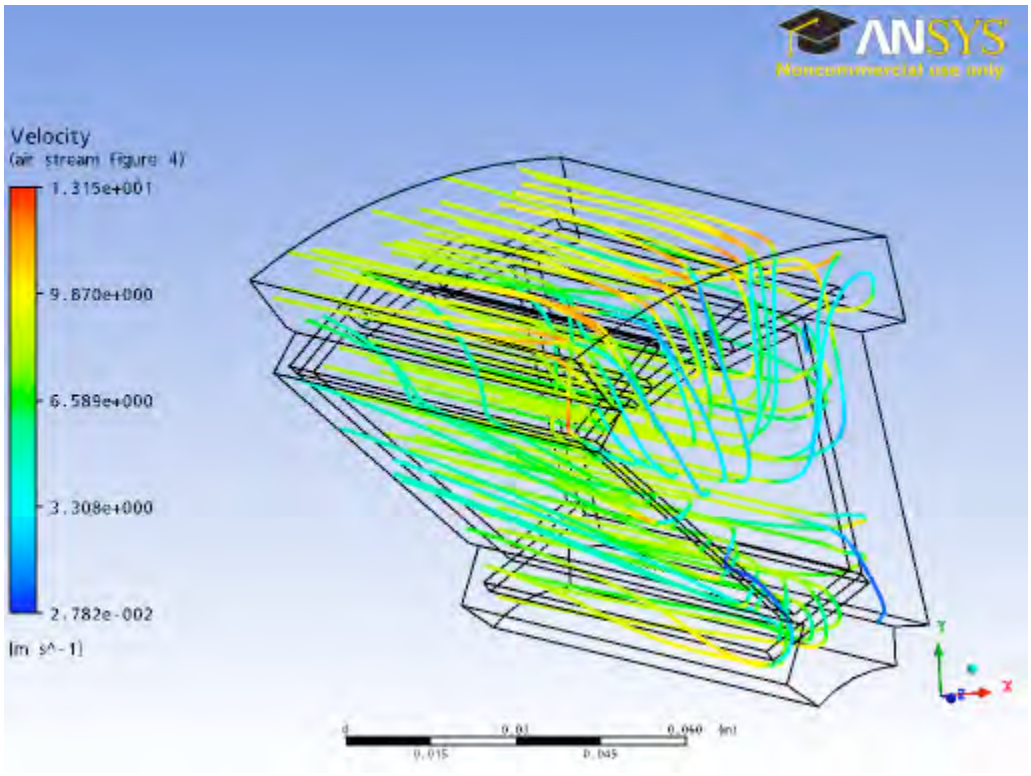


Figure 68 Stream lines showing the cooling air flow. The flow direction is from inside to outside. The color code shows air velocity.

The silicon surface temperature profile is shown in Figure 69.

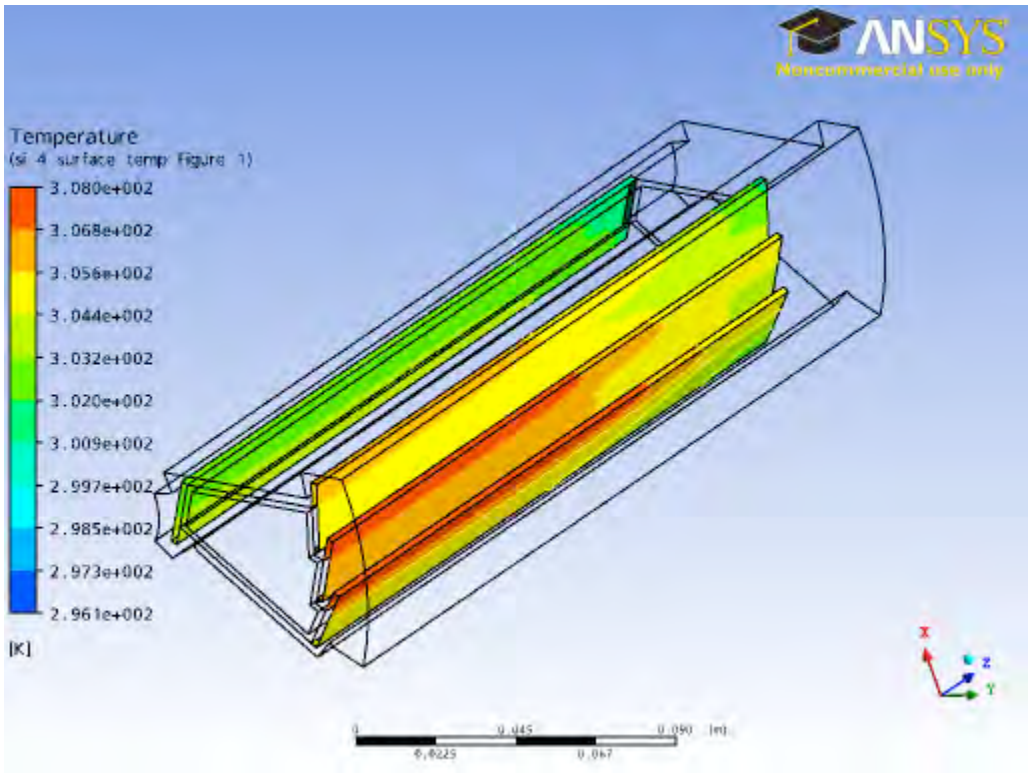


Figure 69 Surface temperature of silicon ladders. The maximum temperature increase above ambient is 12 deg C. The cooling air flows across both the inner and outer surfaces. The air enters from the left on the inside of the support beam, turns around at the right and exits on the left.

In this case an input air velocity of 8 m/s was used. This results in a maximum silicon temperature rise above ambient of 12 deg C which is acceptable. It is interesting to note that the inside ladders next to the beam pipe cool more effectively than the outside ladders. This is because the surface area of the support beam sides provides a significant fraction of the cooling.

The total air flow in this case for the full pixel detector barrel is ~280 CFPM and the temperature rise in the air for the total power of the ladders, 240 W, is 1.5 deg. C. This is a very small rise in the air temperature, so alternatives can be considered with reduced total air flow which would result in a smaller air cooling system.

Alternative air flow design

An alternative design has been investigated with reduced total air flow volume and an increased air velocity at the surface to improve the heat transfer. In this design the high velocity air flow is in the transverse direction local to the ladder surface (see Figure 70). The air flows through narrow slits in the ladder support beam from outside into the sector beam.

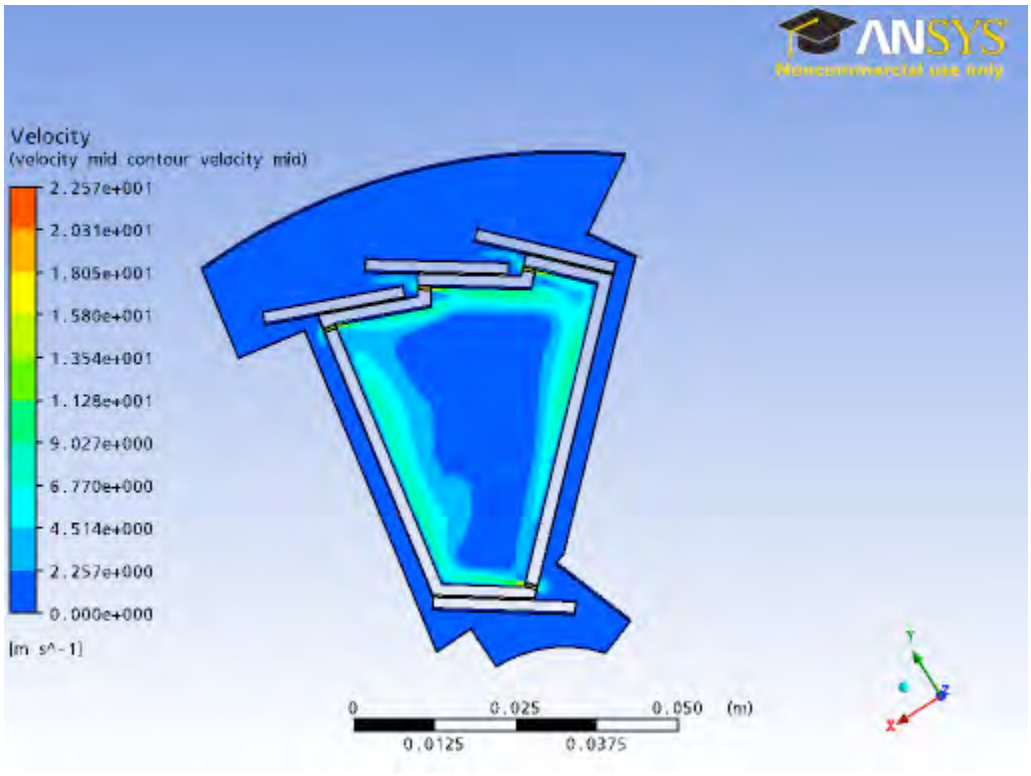


Figure 70 Sector cooling with transverse jets of cooling directed to the inside of the sector beam support structure through thin slots. The air velocity profile is shown in color. The air velocity near the surfaces beneath the ladders is 11 m/s.

The calculated surface temperature as shown in Figure 71 gives a maximum silicon temperature above ambient of 14 deg C. This is not quite as good as the performance with the simpler longitudinal bi directional cooling design with air flow over both inside and outside surface. For this reason future development will focus on the simpler longitudinal flow design.

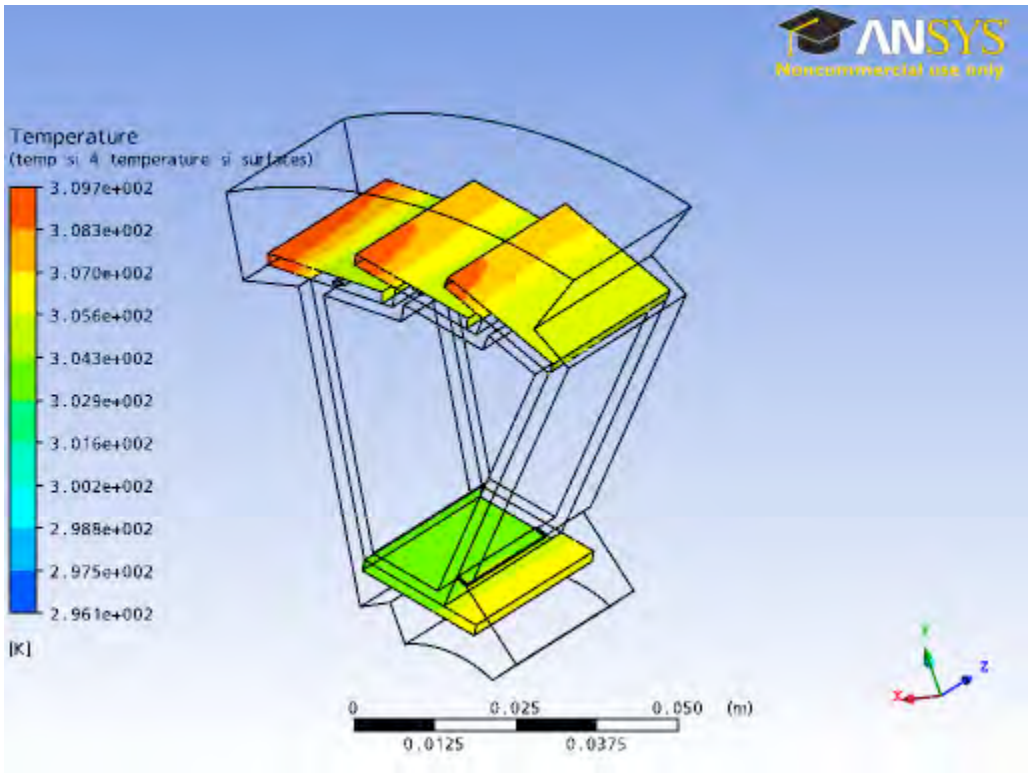


Figure 71 Silicon surface temperature profile for the transverse cooling jet design.

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