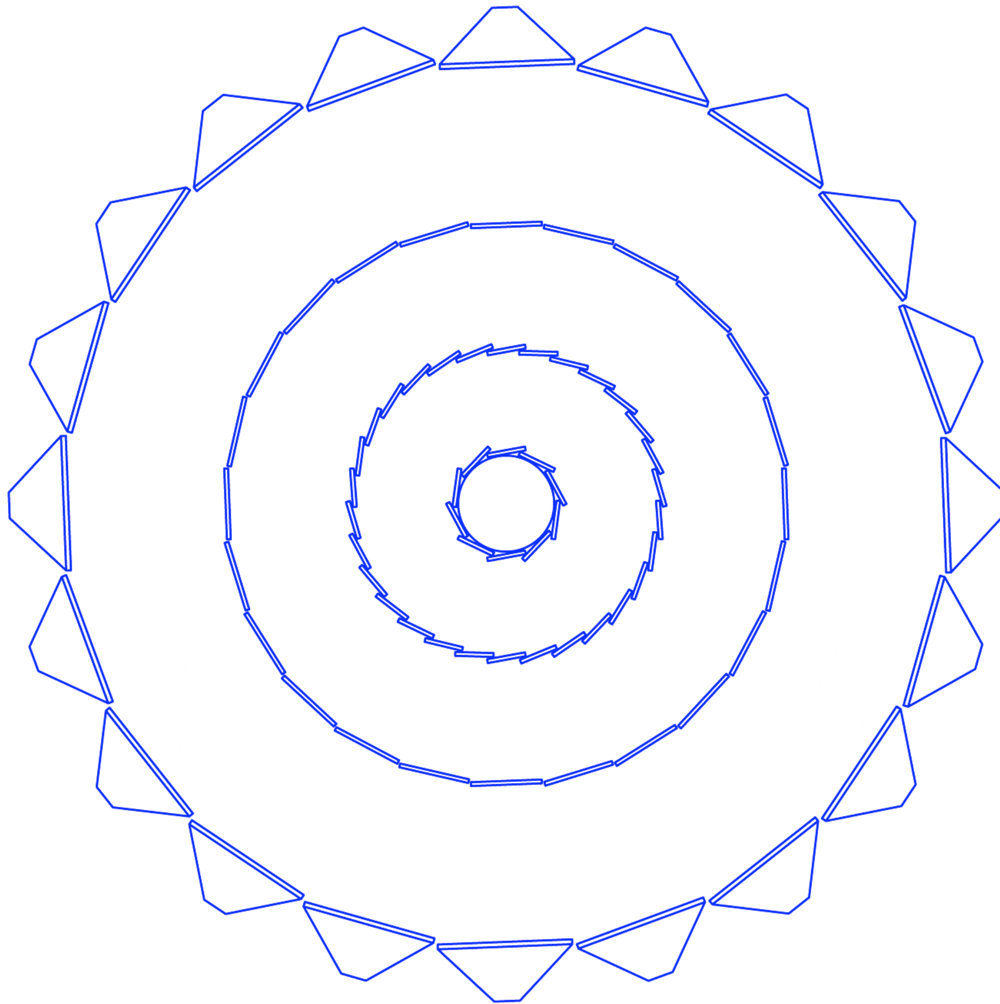
The STAR Heavy Flavor Tracker

Conceptual Design Report



Version: 9

Date: March 17, 2009

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1. Introduction

The Heavy Flavor Tracker (HFT) is a state-of-the-art microvertex detector utilizing active pixel sensors and silicon strip technology. The HFT will significantly extend the physics reach of the STAR experiment for precision measurement of the yields and spectra of particles containing heavy quarks. This will be accomplished through topological identification of D mesons by reconstruction of their displaced decay vertices with a precision of approximately 50 μm in p+p, d+A, and A+A collisions.

The HFT consists of 4 layers of silicon detectors grouped into three sub-systems with different technologies, guaranteeing increasing resolution when tracking from the TPC towards the vertex of the collision. The Silicon Strip Detector (SSD) is an existing detector in double-sided strip technology. It forms the outermost layer of the HFT. The Intermediate Silicon Tracker (IST), consisting of a layer of single-sided strip-pixel detectorss, is located inside the SSD. Two layers of Silicon Pixel Detector (PIXEL) are inside the IST. The PIXEL detectors have the resolution necessary for a precision measurement of the displaced vertex.

The PIXEL detector will use CMOS Active Pixel Sensors (APS), an innovative technology never used before in a collider experiment. The APS sensors are only 50 μm thick with the first layer at a distance of only 2.5 cm from the interaction point. This opens up a new realm of possibilities for physics measurements. In particular, a thin detector (0.28% radiation length per layer) in STAR makes it possible to do the direct topological reconstruction of open charm hadrons down to very low transverse momentum by the identification of the charged daughters of the hadronic decay.

2. Functional Requirements

2.1. General Design Considerations

STAR is a large acceptance experiment with full azimuthal coverage at mid-rapidity in the pseudo-rapidity range $|\eta| < 1$. With the TPC as a central detector and a current read-out speed of about 100 Hz STAR is considered to be a "slow" detector as far as single particle observables are concerned. Even after the DAQ upgrade to 1000 Hz in 2009 the read-out speed will be limiting the single particle capabilities of STAR. The real strength of STAR, good particle identification and full azimuthal coverage, come into play when correlations or multi-particle final states are studied. Good particle identification and full azimuthal coverage have been the bases for the enormous success of the STAR physics program.

It is obvious that when it comes to identifying rare processes, like heavy flavor production with multi-particle final states, full azimuthal coverage will be of utmost importance. Thus, full azimuthal coverage is a prime design requirement for the HFT.

Another important requirement is to keep a very low overall material budget in order to limit the effects of multiple scattering and of conversions. Our goal is to overall reduce the radiation length of the inner tracking and support system compared to the status when the SVT was the STAR inner tracking detector.

The performance requirements listed below are selected so that if those requirements are met by the detector, the detector will be able to achieve the physics requirements. Fulfillment of the performance requirements can be completely determined shortly after the installation of the HFT.

2.2. Pointing Resolution

Heavy flavor hadrons have extremely short life times ($c\tau \sim 50$ μm). Identifying such a short displaced vertex requires extremely good pointing resolution. This is especially important for the identification of low transverse momentum decays where small gains in pointing resolution lead to large gains in detection efficiency. The pointing resolution in $r\varphi$ and in z-direction are shown in Figure 1 as a function of p_T.

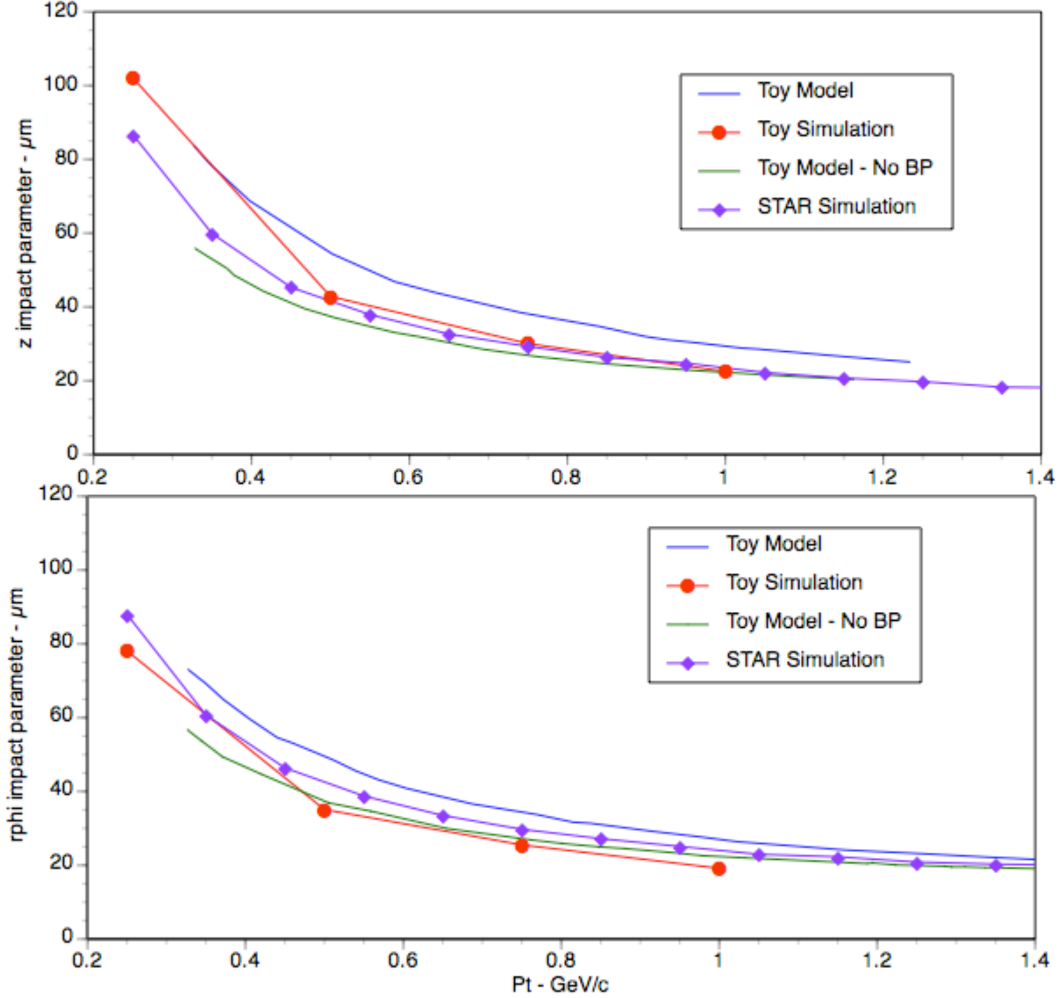


Figure 1: Comparison of three different types of simulations to determine the pointing resolution in rφ and in the z-direction at the vertex. The three methods are the Toy Model, a Toy Simulation, and the full STAR Simulation. Each method has different assumptions and slightly different parameters but overall, the agreement is good. In the figure's legend, BP is short hand for "beam pipe".

We require a pointing resolution of better than 50 μm for kaons of 750 MeV/c. 750 MeV/c is the mean momentum of the decay kaonskanos from D mesons of 1 GeV/c transverse momentum, the peak of the D meson distribution.

The pointing resolution that will be achieved by the HFT can be calculated from the design parameters.

2.3. Multiple Scattering in the Inner Layers

The precision with which we can point to the interaction vertex is determined by the position resolution of the pixel detector layers and by the effects of multiple scattering in the material the particles have to traverse. The beam pipe and the first pixel layer are the two elements that have the most adverse effect on pointing resolution. Therefore, it is

crucial to make those layers as thin as possible and to build them as close as possible to the interaction point.

We have chosen a radius of 2 cm for a new beam pipe. Making this radius even smaller would make the STAR beam pipe the limiting aperture of the RHIC ring. This is not a desirable situation. The central section of the beam pipe will be fabricated from Beryllium. Such a beam pipe can have a minimal wall thickness of 500 μm, equivalent to 0.xx % of a radiation length.

The two pixel layers will be at a radius of 2.5 cm and 8 cm, respectively. The sensors will be thinned down to 50 μm and the ladders will be fabricated in ultra-light carbon fibre technology. The total thickness of the beam pipe and the fist pixel layer will be the equivalent of 0.xx % of a radiation length. With those parameters, the contributions to the pointing resolution from multiple scattering and from detector resolution will be about equal.

The radiation lengths of the two innermost structures, the beam pipe and the first pixel layer, are design parameters.

2.4. Internal Alignment and Stability

The Pixel and the IST positions need to be known and need to be stable over a long time period in order not to have a negativean effect on the pointing resolution. The quality of the data will depend on alignment and long term stability. This is especially important for the Pixel detector that needs to be installed and removed on a short time scale.

The alignment and stability need to be better than 300 μm for the IST and better than 20 μm for the Pixel.

Those parameters can be determined from a survey.

2.5. Pixel Integration Time

Compared to the strip detectors, the Pixel is a slow device with a long integration time. All events that occur during the integration or life time of the Pixel will be recorded. This makes assigning Pixel hits to a particular track in the TPC a difficult pattern recognition problem.

From detailed simulations we have concluded that at RHIC II luminosities the detection and reconstruction efficiency for D-mesons is not appreciably degraded due to multiple events and tracks in the Pixel if the integration time of the detector is smaller than 200 μs.

The Pixel integration time is a design parameter.

2.6. Read-out Speed and Dead Time

In the absence of a good trigger for D-mesons it is imperative for the measurement of rare processes to record as many events as possible and as required by the physics processes. In STAR the speed of the DAQ is the limiting factor for the number of events recorded.

In order not to slow down the STAR DAQ, the HFT read-out speed needs to be compatible with the STAR DAQ speed and the HFT needs to be dead time free.

Read-out speed and dead time are design parameters.

2.7. Detector Hit Efficiency

The hit efficiency of the Pixel and IST detectors is essential for good detection efficiency. In the case of secondary decay reconstruction, the hit inefficiency of each detector layer enters with the power of the number of reconstructed decay particles into the total inefficiency.

In order to keep inefficiency low, we request that each individual detector layer has a hit efficiency of better than 95%.

The hit efficiency of each detector layer can be measured on the bench before installation.

2.8. Life Channels

Dead channels in the Pixel and IST will cause missing hits on tracks and thus lead to inefficiencies in the reconstruction of decay tracks. Therefore, the number of dead channels needs to be as low as possible.

The impact of dead channels on the overall performance will be minimal if more than 97% of all channels are alive at any time.

The number of dead channels can be determined immediately after installation of the detectors.

3. Technical Design

3.1. Overview

The Heavy Flavor Tracker consists of three sub-detectors: the silicon pixel detector (PIXEL), the intermediate silicon tracker (IST), and the silicon strip detector (ssd). These detectors lie inside the radial location of the TPC. The primary purpose of the SSD-IST-PIXEL detector is to provide graded resolution from the TPC into the interaction point and to provide excellent pointing resolution at the interaction point for resolving secondary particles and displaced decay vertices. The TPC will point at the SSD with a resolution of about 1 mm, the SSD will point at the IST with a resolution of about 300 μm, the IST will point at the PIXEL with a resolution of about 200 μm, and the PIXEL detector will point at the vertex with less than 50 μm resolution. A schematic view of the proposed detector layout is shown in Figure 2.

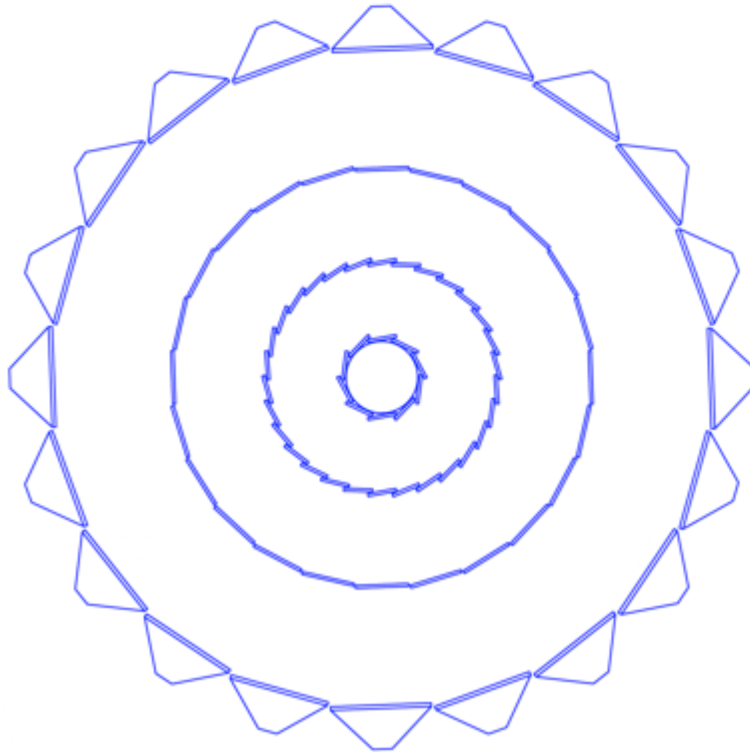


Figure 2: A schematic view of the Si detectors that surround the beam pipe. The SSD is an existing detector and it is the outmost detector shown in the diagram. The IST lies inside the SSD and the PIXEL lies closest to the beam pipe. The beam pipe and its exo-skeleton are also shown.

3.2. Pixel

3.2.1. Introduction

The PIXEL detector is a low mass detector that will be located very close to the beam pipe. It will be built with two layers of silicon pixel detectors: one layer at 2.5 cm average radius and the other at 7.0 cm average radius. The outer layer will have 24 ladders and the inner layer will have 9 ladders; for a total of 33. Each ladder contains a row of 10 monolithic CMOS detector chips and each ladder has an active area of 19.2 cm × 1.92 cm. The CMOS chips contain a 640 × 640 array of 30 μm square pixels and will be thinned down to a thickness of 50 μm to minimize Multiple Coulomb Scattering (MCS) in the detector. The effective thickness of each ladder is 0.28% of a radiation length.

3.2.2. Detector Parameters

The relevant performance parameters for the Pixel detector are shown in Table 1.

Pointing resolution	$(13 \oplus 19\mathrm{GeV}/p{\cdot}c)$ μm
Layers	Layer 1 at 2.5 cm radius Layer 2 at 8 cm radius
Pixel size	18.4 μm × 18.4 μm
Hit resolution	10 μm rms
Position stability	6 μm (20 μm envelope)
Radiation thickness per layer	$X/X0 = 0.28\%$
Number of pixels	436 M
Integration time (affects pileup)	0.2 ms
Radiation tolerance	300 kRad
Rapid installation and replacement to cover rad damage and other detector failure	Installation and reproducible positioning in a shift

Table 1: Performance parameters for the pixel detector.

3.2.3. Sensors and Readout

Development and Deployment Plan

We intend to approach the completion of the Pixel detector for STAR as a two stage development process with the readout system requirements tied to the stages of sensor development effort. The sensor development is taking place at the Institut Pluridisciplinaire Hubert Curien (IPHC) in Strasbourg, France where we are working in collaboration with Marc Winter's group. In the current development path, the first set of prototype sensors to be used at STAR will have digital outputs and a 640 μs integration time. We will use these sensor prototypes to construct a limited prototype detector system for deployment at the STAR detector during the summer of 2010. This prototype system will employ the mechanical design to be used for the final Pixel detector as well as a readout system that is designed to be a prototype for the expected final readout system to be deployed with the final Pixel sensors in a complete detector in the 2012 time frame.

Monolithic Active Pixel Sensor (MAPS) Development at IPHC

The sensor development path for the Pixel detector sensors is tailored to follow the development path of the technology as it was set by the IPHC group. In this path, MAPS sensors with multiplexed serial analog outputs in a rolling shutter configuration are envisioned as the first generation of sensors followed by a more advanced final or ultimate sensor that had a digital output(s). The analog MAPS have been produced and tested and our sensor development path moves to digital binary readout from MAPS with fine grained threshold discrimination, on chip correlated double sampling (CDS) and a fast serial LVDS readout. A diagram showing the current development path and with the attendant evolution of the processing and readout requirements is shown in Figure 3.

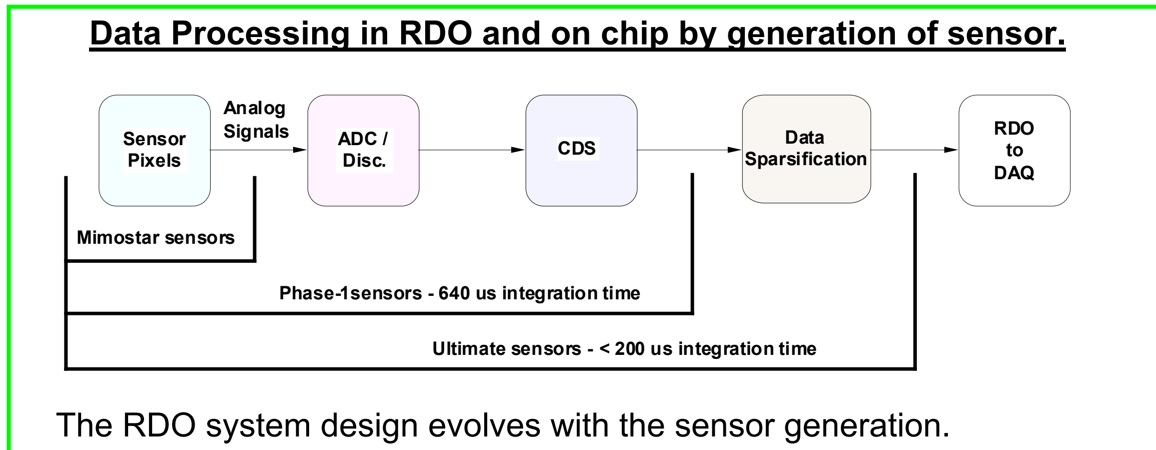


Figure 3: Diagram showing the sensor development path of sensors for the STAR Pixel detector at IPHC in Strasbourg, France. The readout data processing required is shown as a function of sensor generation. The first generation Mimostar sensors are read out via a rolling shutter type analog output. The next generation Phase-1 sensor integrates CDS and a column level discriminator to give a rolling shutter binary readout with a 640 μs integration time. The final generation Ultimate sensor integrates data sparsification and lowers the readout time to < 200 μs.

The Mimostar series sensors are the generation of sensors that have been fabricated and tested. These are 50 MHz multiplexed analog readout sensors with 30μm × 30μm pixels in variously sized arrays depending on generation. This generation has been tested and characterized and, with the exception of some yield issues, appears to be well understood. Testing with these sensors is well described in a NIM paper reference.

The next generation is named "Phase-1". This sensor will be based on the Mimosa-8 and Mimosa-16 sensors and will contain on-chip correlated double sampling and column level discriminators providing digital outputs in a rolling shutter configuration. The Phase-1 will be a full sized 640 × 640 array resulting in a full 2 cm × 2 cm sensor size. In order to achieve a 640 μs integration time, the Phase-1 sensor will be equipped with four LVDS outputs running at 160 MHz. The first delivery of wafers of this sensor design is expected in late 2008.

The final sensor is named "Ultimate". The Ultimate sensor includes all of the attributes of the Phase-1 sensor with the pixel sub-arrays clocked faster to give a <200 μs integration time and the integration of a run length encoding based data sparsification and zero suppression circuit. The pixel size has been reduced to 18.4 μm × 18.4 μm to increase the sensor radiation tolerance in the higher luminosity RHIC II environment. There are two data output lines from the sensor and the data rates are low thanks to the newly included data sparsification circuitry. The first prototypes of this design are expected to be delivered in the 2010 time frame.

Sensor Series Specifications

The specifications of the sensors under development are shown in Table 2.

	Phase -1	Ultimate
Pixel Size	30 μm × 30 μm	18.4 μm × 18.4 μm
Array size	640 × 640	1024 × 1088
Active area	~ 2 × 2 cm	~ 2 × 2 cm
Frame integration time	640 μs	100 – 200 μs
Noise after CDS	10 e-	10 e-
Readout time / sensor	640 μs	100 – 200 μs
Outputs / sensor	4	2
Operating mode	Column parallel readout with all pixels read out serially.	Column parallel readout with integrated serial data sparsification.
Output type	Digital binary pixel based on threshold crossing.	Digital addresses of hit pixels with run length encoding and zero suppression. Frame boundary marker is also included.

Table 2: Specifications of the Phase-1 and Ultimate sensors.

The Phase-1 is a fully functional design prototype for the Ultimate sensor which results in the Phase-1 and Ultimate sensors having very similar physical characteristics. After successful development and production of the Phase-1 sensors, a data sparsification system currently under development at IPHC will be integrated with the Phase-1 design. With the additional enhancement of design changes allowing for faster clocking of the sub-arrays, the resulting sensor is expected to be used in the final Pixel detector. In addition to the specifications listed above, both sensors will have the following additional characteristics;

- Marker for first pixel
- Register based test output pattern JTAG selectable for binary readout troubleshooting.
- JTAG selectable automated testing mode that provides for testing pixels in automatically incremented masked window to allow for testing within the overflow limits of the zero suppression system.
- Independent JTAG settable thresholds
- Radiation tolerant pixel design.
- Minimum of 3 fiducial marks / sensor for optical survey purposes.
- All bonding pads located along 1 side of sensor
- Two bonding pads per I/O of the sensor to facilitate probe testing before sensor mounting.

Architecture for the Phase-1 Sensor System

The requirements for the Phase-1 prototype and final readout systems are very similar. They include;

- Triggered detector system fitting into existing STAR infrastructure and to interface to the existing Trigger and DAQ systems.
- Deliver full frame events to STAR DAQ for event building at approximately the same rate as the TPC (~ 1 KHz for the STAR DAQ1K upgrade).
- Reduce the total data rate of the detector to a manageable level (< TPC rate)

We have designed the prototype data acquisition system to read out the large body of data from the Phase-1 sensors at high speed, to perform data compression, and to deliver the sparsified data to an event building and storage device.

The proposed architecture for the readout of the Phase-1 prototype system is shown in with the physical location and separation of the system blocks shown in Figure 4 and Figure 5.

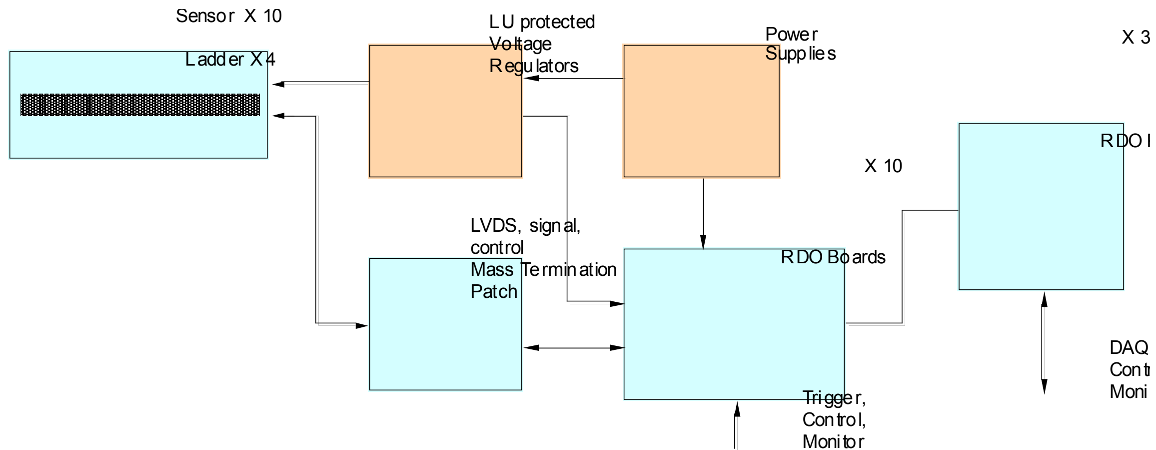


Figure 4: Functional block schematic for the readout for the Phase-1 prototype system. The detector ladders and accompanying readout system have a highly parallel architecture. One system unit of sensor array / readout chain is shown. There are ten parallel sensor array / readout chain units in the full system.

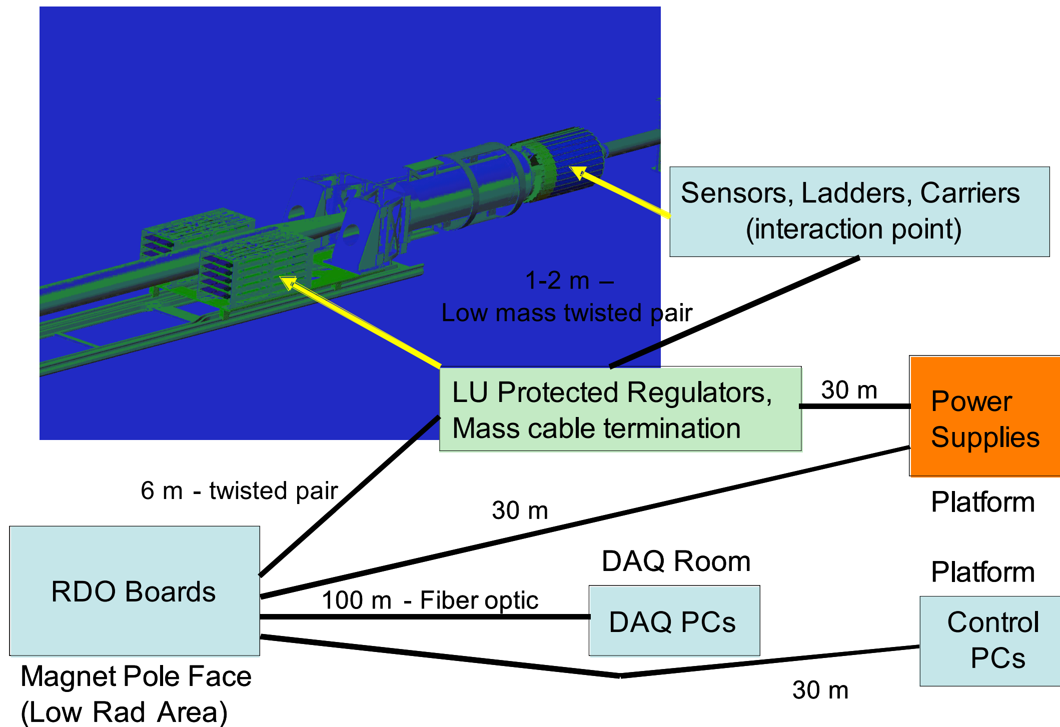


Figure 5: Physical layout of the readout system blocks. This layout will be the same for both the Phase-1 based patch and the final Pixel detector system.

The architecture of the readout system is highly parallel. Each independent readout chain consists of a four ladders mechanical carrier unit with each ladder containing ten Phase-1 sensors. The current plan is to install a patch of Phase-1 sensors consisting of at least two carrier units mounted with the final mechanical positioning structure and positioned with a 120 degree separation. The readout system will be described as if all carriers will be installed since this architecture also extends to the final Pixel system.

The basic flow of a ladder data path starts with the APS sensors. A Pixel ladder contains 10 Phase-1 APS sensors, each with a 640 × 640 pixel array. Each sensor contains four separate digital LVDS outputs. The sensors are clocked continuously at 160 MHz and the digital data containing the pixel threshold crossing information is read out, running serially through all the pixels in the sub-array. This operation is continuous during the operation of the Phase-1 detectors on the Pixel ladder. The LVDS digital data is carried from the four 160 MHz outputs in each sensor in parallel on a low mass flex printed circuit board to discrete LVDS buffers located at the end of the ladder and out of the low mass detector region. This electronics portion of the ladder also contains the buffers and drivers for the clocks and other control signals needed for ladder operation.

Each Phase-1 sensor requires a JTAG connection for register based configuration, power, ground, a 160 MHz readout clock and a synchronization signal to begin the readout. These signals and latch-up protected power as well as the LVDS outputs and synchronization and marker signals from the detectors are carried via low mass twisted pair cables from the discrete electronics at the end of the ladder to a power / mass termination board located approximately 1 meter from the Pixel ladders. There is one readout board per Pixel carrier (40 sensors). A diagram of a ladder is shown in Figure 6.

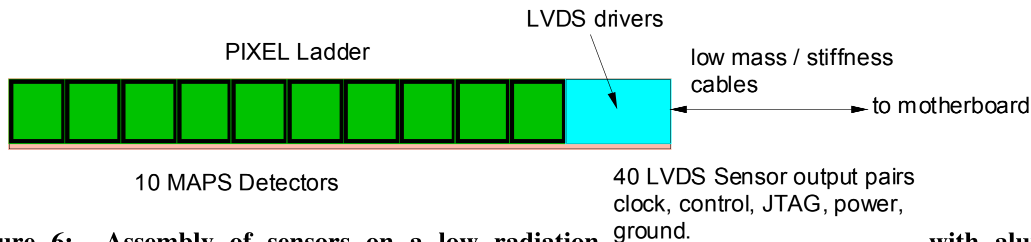


Figure 6: Assembly of sensors on a low radiation length Kapton flex cable with aluminum conductors. The sensors are connected to the cable with bond wires along one edge of the ladder.

The flex cable parameters are shown below;

- 4 layer - 150 micron thickness
- Aluminum Conductors
- Radiation Length ~ 0.1 %
- 40 LVDS pair signal traces
- Clock, JTAG, sync, marker traces.

The connection to the driver end of the ladders will be made with very fine 150 μm diameter twisted pair wire soldered to the cable ends. These wires are also very low stiffness to avoid introducing stresses and distortions into the mechanical structure. The other ends of these fine twisted pair wires will be mass terminated to allow connection to the Power / Mass-termination (PM) board located approximately 1 meter away.

Latch-up protected power is provided to the sensors from the PM boards. Each ladder has independently regulated power with latch up detection circuitry provided by a power daughter card that plugs into the PM board. There are four regulation and latch-up daughter cards per PM board and a total of ten PM boards are needed for the complete detector system readout. A block diagram for the PM board is shown in Figure 7.

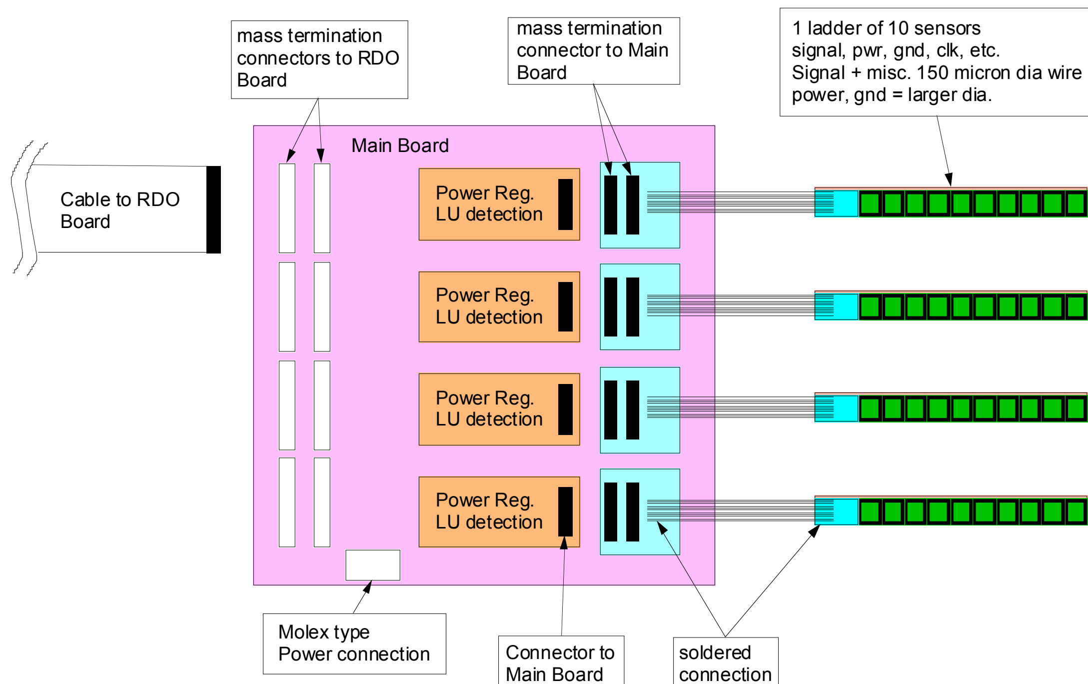


Figure 7: Power and mass-termination board block diagram. The digital signals to and from the sensors are routed through the main board and carried to mass termination connectors for routing to the readout boards. Latch-up protected power regulation is provided to each ladder by a power daughter card mounted to the main board. The main power supplies are located in the STAR racks.

The digital sensor output signals are carried with a 160 MHz clock to from the PM board to the readout boards (RDO) which are mounted either on the magnet iron of the STAR magnet structure or in a movable electronics rack located on the cave floor. Each location is approximately 6 meters away from the MTBs. A diagram describing the attributes of the two PCBs that make up the RDO system can be seen in Figure 8. A functional block diagram of the RDO can be seen in Figure 9.

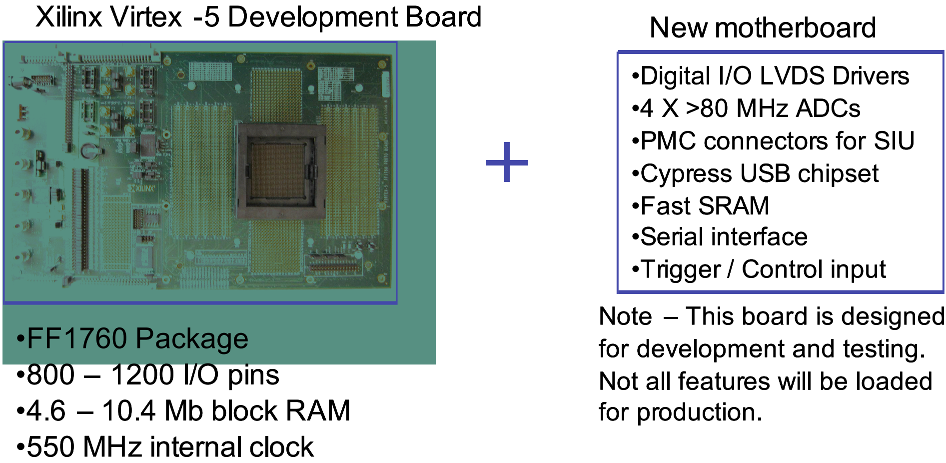


Figure 8: Readout board(s). The readout system consists of two boards per carrier of 40 sensors. A commercial Xilinx Virtex-5 development board is mated to a custom motherboard that provides all of the I/O functions including receiving and buffering the sensor data outputs, receiving the trigger from STAR and sending the built events to a STAR DAQ receiver PC via fiber optic connection.

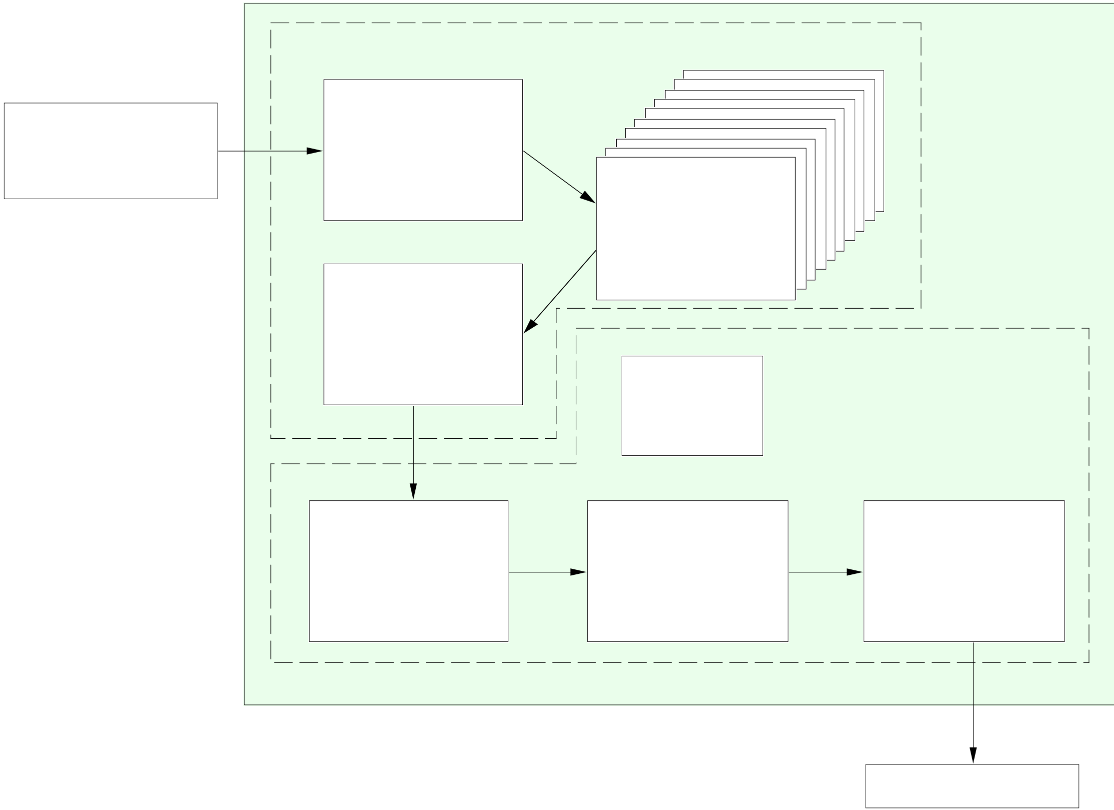


Figure 9: Functional block diagram of the data flow on the RDO boards.

The RDO boards are based on a fast Xilinx Virtex-5 FPGA development board which is mated to a custom motherboard that provides LVDS buffering into the FPGA, the STAR trigger input, PMC connectors for mounting the CERN developed fiber optic Detector Data Link (DDL), SRAM, and various ADCs and I/O to be used in testing. The data processing path is as follows. The sensor output signals are buffered and then fed into the FPGA. In the FPGA the data is resorted to give a raster scan, after which hits registered on pixels are converted to pixel addresses using an address counter. This mechanism of zero suppression, the conversion of hits to addresses in a relatively low multiplicity environment, is the main mechanism for data reduction used in this readout system. The efficiency and accidental rate of a simple threshold on pixel signal is shown in Figure 10.

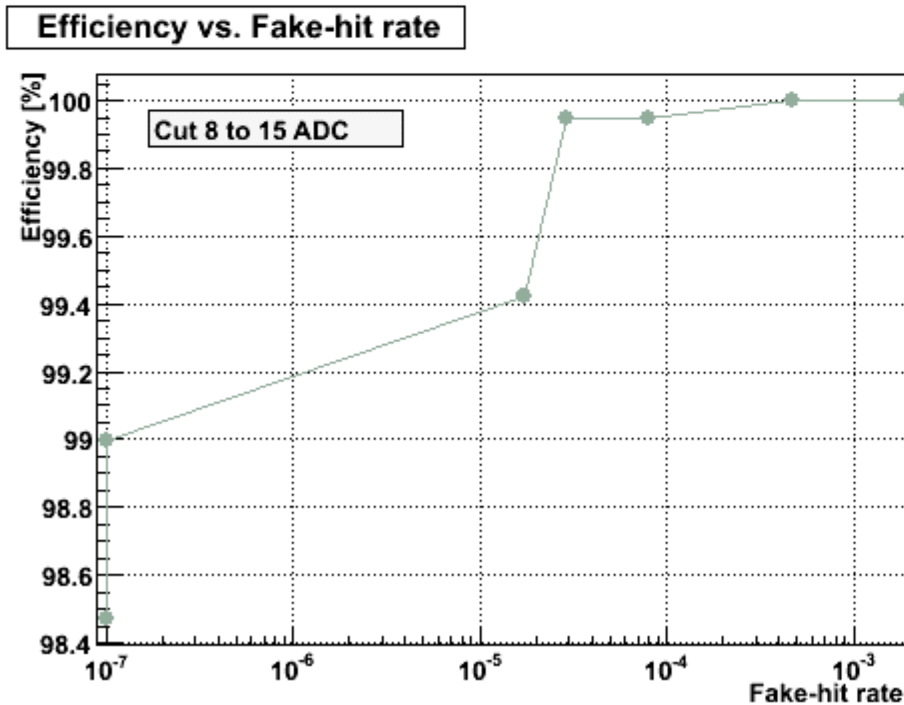


Figure 10: Efficiency and fake hit rate for a simple threshold cut on pixel signal level. This figure is obtained from beam data taken with Mimostar-2 sensors.

When a trigger is received, one of a bank of event buffers is enabled for one frame (409,600 pixels). After the frame has been recorded in the event buffer, the results of that frame are sent to an event builder. The event builder gathers all of the addresses on the RDO from that trigger and builds them into an event which is then passed via fiber optic links to the STAR DAQ receiver PCs. We intend to use the Source Interface Unit (SIU) and Readout Receiver Cards (RORC) developed for ALICE as our optical link hardware to transfer data to and from the STAR DAQ system. These links have been chosen as the primary readout connections for the new STAR TPC FEE. Leveraging existing hardware and expertise in STAR allows for a faster and more reliable design than developing our own custom solution. The complete system consists of a parallel set of carrier (4 ladder /

carrier) readouts consisting of 10 separate chains. A system level functionality block diagram is shown in Figure 11.

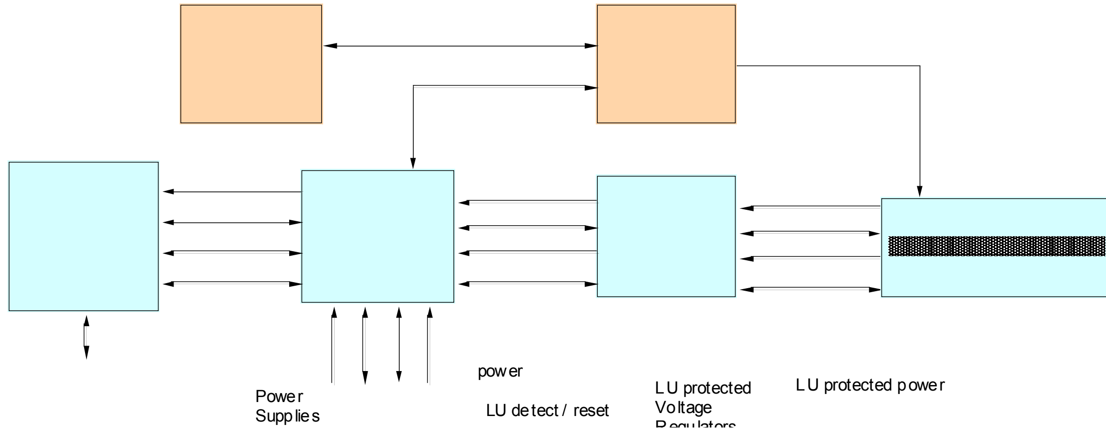


Figure 11: System level functionality diagram of the readout of the Pixel sensors. One of the ten parallel readout chains is shown.

Data Synchronization, Readout and Latency

The readout of the prototype Phase-1 Pixel sensors is continuous and hit-to-address processing is always in operation during the normal running of the detector. The receipt of a trigger initiates the saving of the found hit addresses into an event buffer for 1 frame (409,600 pixels). The Pixel detector as a whole will be triggered via the standard STAR Trigger Clock Distribution (TCD) module. Since 640 μs are required to read out the complete frame of interest, the data will be passed to DAQ for event building ~ 640 μs after the trigger is received. We will provide for multiple buffers that will allow the capture of temporally overlapping complete frames. This will allow us to service multiple triggers within the 640 μs readout time of the sensor. In this system, the hit address data is fanned out to 10 event buffers. A separate event buffer is enabled for the duration of one frame upon the receipt of a trigger from the TCD. Subsequent triggers enable additional event buffer until all of the event buffers are full and the system goes busy. The resulting separate complete frames are then passed to the event builder as they are completed in the event buffers. This multiple stream buffering gives a system that can be triggered at a rate above the expected average rate of the STAR TPC (approximately 1 kHz) after the DAQ1K upgrade. Furthermore, since the addition of buffers is external to the sensors, the capability for the addition of large amounts of fast SRAM will be included in the RDO board design allowing for flexibility in our readout system configuration. This multiple event buffer architecture will result in the duplication of some data in frames that overlap in time, but our data rate is low and the duplication of some data allows for contiguous event building in the STAR DAQ, which greatly eases the offline analysis. In addition, synchronization between the ladders/boards must be maintained. The Pixel will receive triggers and the STAR clock via the standard STAR Trigger and Clock Distribution module (TCD). We will provide functionality to allow the motherboards to be synchronized at startup and any point thereafter.

Triggering Considerations

The primary tracking detector of the STAR experiment is the TPC with the Heavy Flavor Tracker upgrade designed to add high resolution vertex information. The Pixel detector is part of a larger group of detectors that make up the HFT upgrade at STAR. The other tracking detector components of the HFT include the Silicon Strip Detector (SSD) and the Intermediate Silicon Tracker (IST). Since the HFT is a system of detectors, in order to maximize efficiency, the trigger response and dead time characteristics of the each detector in the HFT system should be matched, as much as possible, to the others. As the main detector, the post DAQ-1K TPC sets the effective standard for the other detectors in the system. In the current understanding of the system, the Pixel detector information is only useful in conjunction with the external tracking detectors and thus the Pixel detector will only be triggered when the TPC is triggered.

The triggers in STAR are produced essentially randomly with a 110 ns crossing clock spacing. The behavior of the TPC is to go dead for 50 μs following the receipt of a trigger. This means that the TPC, and by extension the Pixel detector, will receive random triggers spaced by a minimum of 50 μs. An additional constraint is imposed by the fact that the DAQ 1K contains 8 buffers at the front end. This allows for the capability of the TPC to take a quick succession of 8 triggers (separated by 50 μs) but then the TPC will go busy until the data has been transferred and buffers cleared. The time required for this depends on the event size. (Some of these numbers can be found at http://drupal.star.bnl.gov/STAR/daq1000-capabilities others are private communication with the STAR DAQ group (Tonko Ljubicic)). This behavior provides the basis for the assessment of the trigger response characteristics of the detectors in the HFT system. In general, HFT detector readout systems should provide for the acquisition of up to 8 successive triggers separated by 50 μs with some, as yet uncharacterized, clearing time. The goal is to have the HFT detectors "live" whenever the TPC is "live". In appendix 1 we show some analysis of the trigger response characteristics of the Pixel detector.

System Performance for the Phase-1 Prototype Sensor System

The raw binary data rate from each Phase-1 sensor is 80 MB / s. For the 400 sensors that make up the Pixel detector this corresponds to 32GB / s. This raw data rate must clearly be reduced to allow integration into the overall STAR data flow. Zero suppression by saving only addresses of hit pixels is the main mechanism for data volume reduction. The parameters used to calculate the data rates are shown in Table 3.

Item	Number
Bits/address	20
Integration time	640 μs
Luminosity	3×10^{27}
Hits / frame on Inner sensors (r=2.5 cm)	295
Hits / frame on Outer sensors (r=8.0 cm)	29
Phase-1 sensors (Inner ladders)	100
Phase-1 sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5
Average Trigger rate	1 kHz

Table 3: Parameters used to calculate data rates from a Phase-1 based system.

Based on the parameters given above, the average data rate (address only) from the sensors in the prototype Phase-1 detector is 237 kB / event which give an average data rate of 237 MB / s. It is possible to reduce the data rate further using a run length encoding scheme on the addresses as they are passed from the event buffer to the event builder as indicated in Table 3. We are currently investigating this option, though the data rate reduction from this approach is expected to be moderate. The raw data rate reduction from the hit pixel to address conversion is given graphically below as Figure 12.

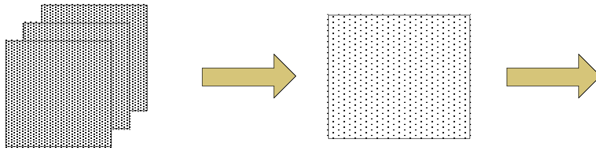


Figure 12: Data rate reduction in the Phase-1 readout system.

Architecture for the Ultimate Sensor System

The most significant difference between the Phase-1 and Ultimate sensors is the integration of zero suppression circuitry on the sensor. The ultimate sensors provide zero suppressed sparsified data with two LVDS output line per sensor. The pixel size for this final production sensor is reduced to 18.4 μm resulting in a larger array. This smaller pixel has a shorter charge collection time making it more radiation tolerant. In addition, the sub-frame arrays are clocked faster to give a <200 μs integration time and a frame

boundary marker is added to the data stream to allow for the demarcation of frame boundaries in the absence of hits in the sensor and to allow for synchronization with the RDO system. The upgrade from the Phase-1 to the Ultimate sensors in the system is expected to involve the fabrication of new sensor ladders using the same mechanical design used in Phase-1 but with the addition of new Ultimate series sensors and a redesign of the kapton readout cable. The Ultimate sensor kapton readout cable will require significantly fewer (20 LVDS pairs instead of 40) traces for readout and the new cable design should have a lower radiation length. The task of reading out the Ultimate series sensors is actually less challenging than the readout of the Phase-1 sensors since the data reduction functionality is included in the sensor. **The readout hardware described above for the Phase-1 readout system remains the same for the Ultimate readout system.** Some reconfiguration of the functionality in the FPGA is required for readout of the Ultimate sensor Pixel detector. A functional block diagram for the RDO boards is shown in Figure 13.

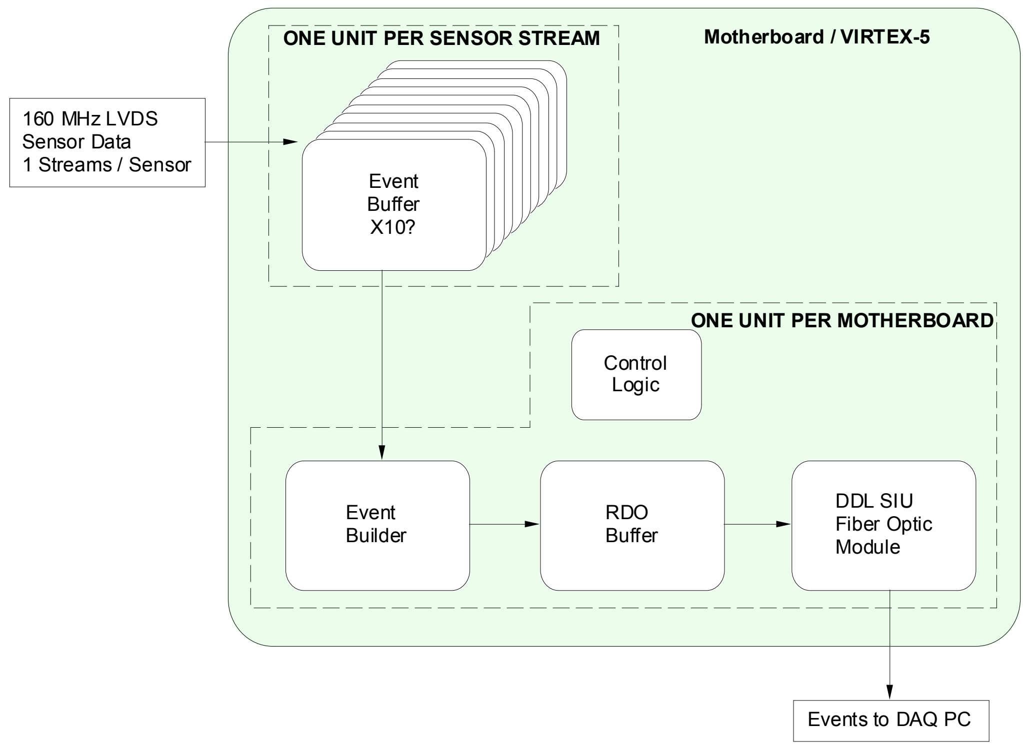


Figure 13: Functional block diagram of the RDO boards for the readout of the Ultimate detector based Pixel detector.

The Ultimate sensor operates in the same rolling shutter readout mode as the PHASE-1 sensor. The address data clocked out of the Ultimate chip has understood latencies that we will use to keep track of triggered frame boundaries and will be able to verify using synchronization markers from the sensors. The first pixel marker from the sensor corresponds to the actual scan of pixels through the sensor. The frame boundary marker delineates frame boundaries in the sparsification system on the sensor. Using this information and knowing the internal latencies in the sensor, we can generate the internal

logic in the FPGA to implement the same multiple buffering technique that was previously described.

System Performance for the Ultimate Sensor System

The parameters used to calculate the data rates for the system are shown in Table 4.

Item	Number
imtegration time	200 μs
Luminosity	8×10^{27}
Hits / frame on Inner sensors (r=2.5 cm)	246
Hits / frame on Outer sensors (r=8.0 cm)	24
Phase-1 sensors (Inner ladders)	100
Phase-1 sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5
Average Trigger rate	1 kHz

Table 4: Parameters used to calculate data rates from a Ultimate sensor based system.

From these parameters, we calculate an average event size of 209 kB giving an address data rate of 209 MB / s from the Ultimate sensor based Pixel detector.

A more detailed analysis of the readout chain including parameters such as the size of buffers and the internal FPGA functions is included as appendix 1.

3.2.4. Sensors and Readout Simulation and Prototyping

Mimostar-2 based telescope test at STAR

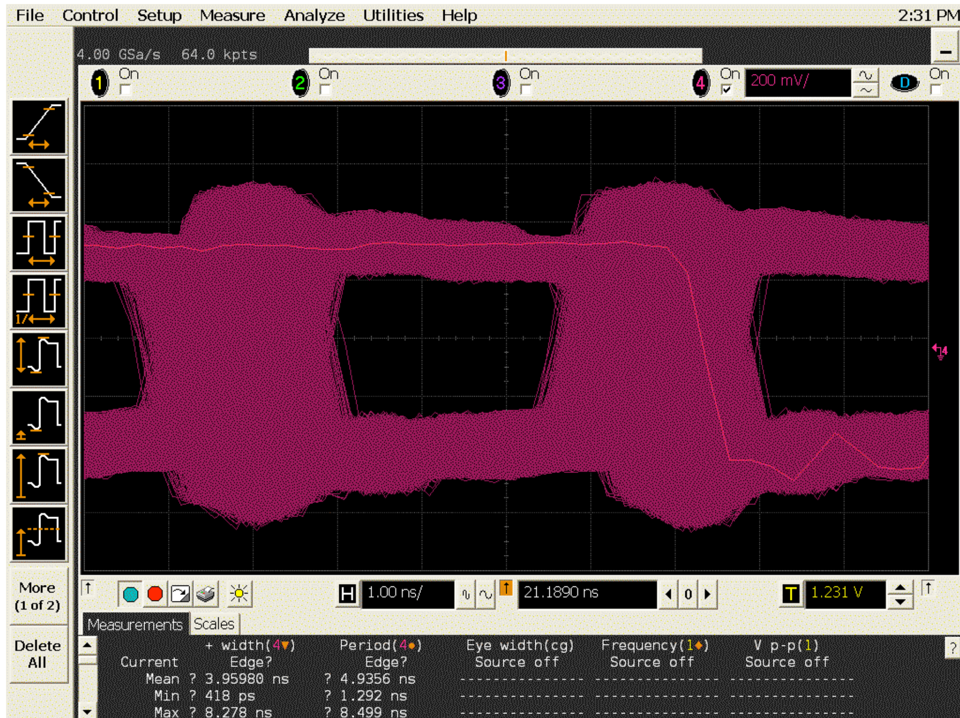
Using a preliminary system design for analog readout, we have taken data with a set of Mimostar-2 sensors at STAR. This system is an early prototype whose performance is evaluated as part of the overall vertex detector development effort. We have successfully implemented a continuous readout 50 MHz data acquisition system with on-the-fly data sparsification that gives near three orders of magnitude data reduction from the raw ADC rates. This readout system has been mated with prototype Mimostar2 sensors and configured as a telescope system to measure the charged particle environment in the STAR environment near the final detector position. This telescope is shown in Figure 14.

Figure 14: Three Mimostar-2 sensors in a telescope configuration used in a beam, test at STAR.

We find that the system works well, gives reasonable efficiency and accidental hit rates, and measures an angular distribution of tracks consistent with imaging the interaction diamond and with imaging beam-gas interaction type background. The prototype readout system integrated well into the existing STAR electronics and trigger infrastructure and functioned successfully as another STAR detector subsystem. This prototype readout system and the results obtained are described in a NIM paper.[1]

LVDS Data Path Readout test

The readout system architecture for the Phase-1 and Ultimate sensors to be used in the Pixel detector for the Heavy Flavor Tracker upgrade at STAR contains a high speed digital data path that is required to read out the sensor hits during the sensor integration time. The RDO sensor data interface path requires that LVDS data move over a total distance of 6 – 8 meters with a speed of 160 MHz for Phase-1 and 125 MHz for Ultimate. 1-2 meters of this distance is over high impedance fine twisted pair wire. Since this design is challenging, though it works on paper, it is prudent to make a prototype set of testing boards and check the performance of our design as a precursor to starting a production design for the final set of readout boards. We have completed making a complete set of test boards for one basic block of the highly parallel RDO system consisting of a functional ladder mockup, mass termination board prototype and a limited functionality RDO motherboard coupled to a Xilinx Virtex-5 Development board. The test was successful with bit error rates of approximately 10-15 for the configurations and clock speeds needed for the detector. A report on this test may be found as Appendix 2.



the FPGA (after all buffers) and triggered on the output data from the FPGA. Full width opening in system is ~ 2.3 ns.

3.2.5. Mechanical Design

Design Overview

The mechanical design has been driven by the following design goals:

- Minimize multiple coulomb scattering, particularly at the inner most layer
- Locate the inner layer as close to the interaction region as possible
- Allow rapid detector replacement
- Provide complete spatial mapping of the pixels from the beginning

The first two goals, multiple coulomb scattering and minimum radius, set the limit on pointing accuracy to the vertex. This defines the efficiency of D and B mesons detection.

The third goal, rapid detector replacement, is motivated by recognition of difficulties encountered in previous experiments with unexpected detector failures. This third goal is also motivated by the need to replace detector that are radiation damaged from operating so close to the beam.

The fourth goal, complete spatial mapping, is important to achieve physics results in a timely fashion. The plan is to know at installation where the pixels are located with respect to each other to within 20 microns and to maintain the positions throughout the operation.

The pixel detector (see Figure 16) consists of two concentric barrels of detector ladders 20 cm long. The inner barrel has a radius of 2.5 cm and the outer barrel has an 8 cm radius. The barrels separate into two halves for assembly and removal. In the installed location both barrel halves are supported with their own 3 point precision kinematic mounts located at one end close to the detector barrel. During installation, support is provided by the hinge structures mounted on a railed carriage. Cooling is provided by air flowing in from one end between the two barrel surfaces and returning in the opposite direction over the outer barrel surface and along the inner barrel surface next to the beam pipe.

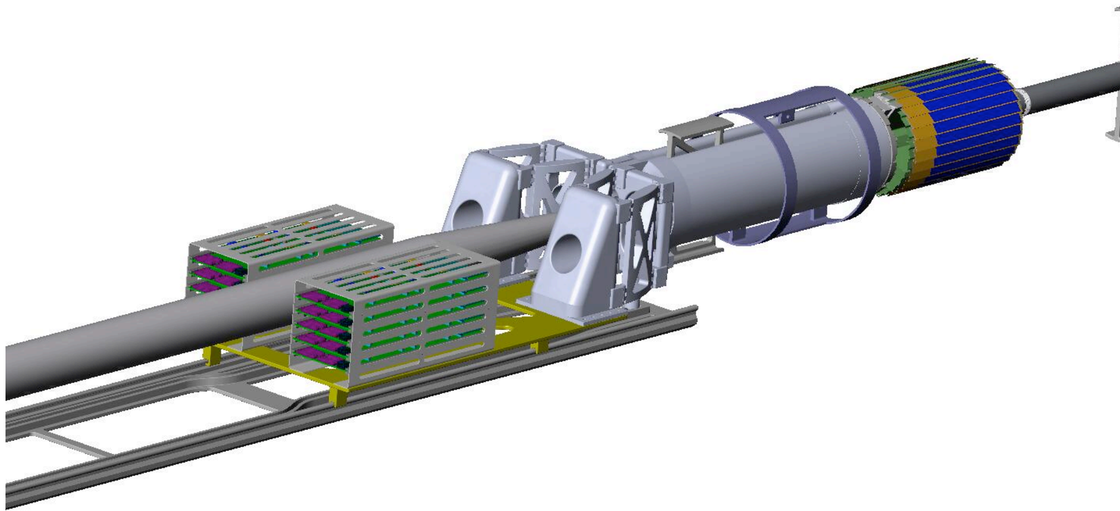


Figure 16: Pixel detector mechanics showing detector barrel, support structures and insertion parts plus interface electronics boards.

The design of the components is presented in the following section. Related structural and cooling analysis is covered in Appendix 2.

Detector ladder design

As previously mentioned (Section 3.2.3) the detector chips are arranged 10 in a row to form a ladder. An exploded view of the mechanical components is shown in Figure 17. The thinned silicon chips are bonded to a flex aluminum Kapton cable which is in turn bonded to a thin carbon composite structure. All electrical connections from the chips to the cable are done with a single row of wire bonds along one edge of the ladder. The carbon composite sheet which is quite thin will only be sufficient for handling and heat conduction. The primary stiffness and support of the ladder is provided by the support beam. This particular ladder structure has not been built yet, but it will utilize

construction methods that we have developed in our previous prototype designs which included gull wing and foam laminate designs. Parts are aligned and held in place with vacuum chuck tooling for bonding. Fifty micron soft, pressure sensitive acrylic adhesive 200MP by 3M is used to make the bonds. A method has been developed which uses a 4 bar pressure chamber to remove bond voids and to stabilize the bond. The low elastic modulus of the adhesive is an important component in the design as it greatly reduces bi metal type deformations stemming from differential expansion caused by thermal changes and humidity changes. This will be discussed in more detail in Appendix 2.

The next step in the ladder development will be to build mechanical prototypes to verify the mechanical design both structurally and thermally.

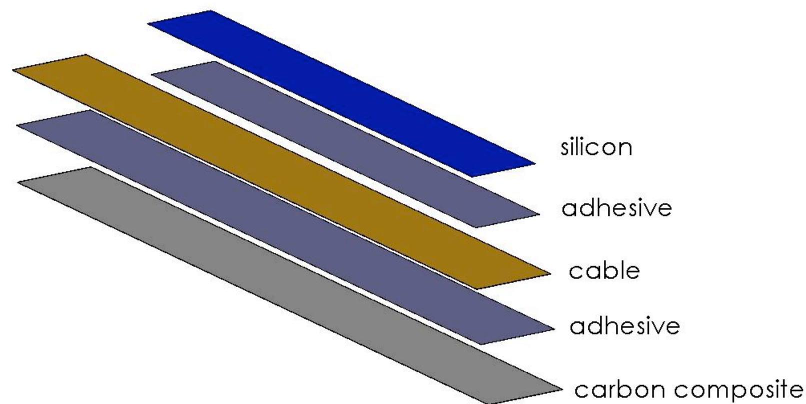


Figure 17: Exploded view of the ladder showing components. The silicon is composed of 10 ~square chips, bit it is shown hear as continuous piece of silicon as it has been modeled for analysis.

Ladder support system

A critical part of the ladder support is the thin carbon composite beam which carries one inner ladder and three outer ladders as shown in Figure 18. This beam which is an adaptation of the ALICE pixel detector design provides a very stiff support while minimizing the radiation length budget. Significant stiffness is required to control deformations from gravity, cooling air forces and differential expansion forces from both thermal and humidity variations. The composite beam carries a single inner ladder and three outer ladders. Ten of these modules form the two barrel layers. The beam in addition to its support function provides a duct for cooling air and adds cooling surface to increase heat transfer from the silicon chips. By making the beam from high strength and high thermal conductivity carbon fiber the wall thickness can be as thin as 200 microns and still satisfy strength and heat transfer requirements. The final thickness however, will probably be limited by fabrication challenges. Forming methods under consideration are a single male mandrel with vacuum bagging or alternatively nested male and female mandrels.

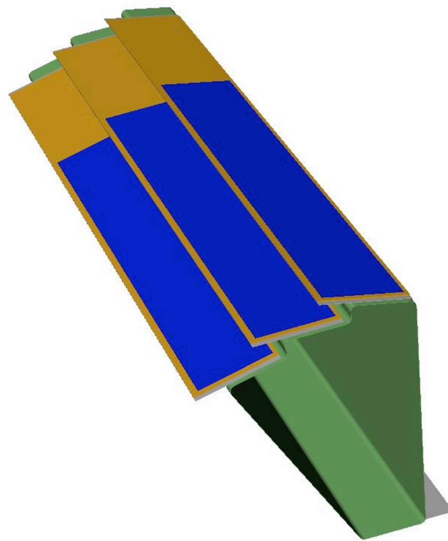


Figure 18: Thin wall carbon support beam (green) carrying a single inner barrel ladder and three outer barrel ladders. The beam in addition to supporting the ladders provides a duct for conducting cooling air and added surface area to improve heat transfer to the cooling air.

The ladders will be glued to the beam using a low strength silicon adhesive as was done in the ATLAS pixel design. This adhesive permits rework replacement of single ladders.

Support of the sectors (beam with ladders) is done in two halves with 5 sector beams per half module (see Figure 19). The sector beams are attached to carbon composite "D tube" with precision dove tail mounts for easy assembly and replacement.

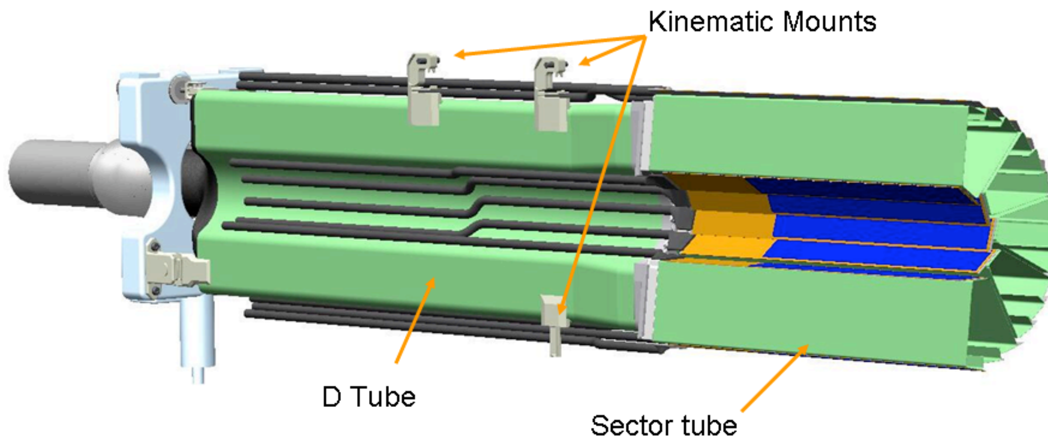


Figure 19: Half module consisting of 5 sector beam modules. The sector beam modules are secured to a carbon composite D tube using a dove tail structure which permits easy replacement of sector modules. Carbon composite parts are shown in green for greater visibility.

The "D tube" supports the 5 sector beams and conducts cooling air to the sectors.

Kinematic support and docking mechanism

When the pixel detector is in its final operating position it is secured at 3 points with precision reproducible kinematic mounts to the Inner Support Cylinder (ISC) as shown in Figure 20.

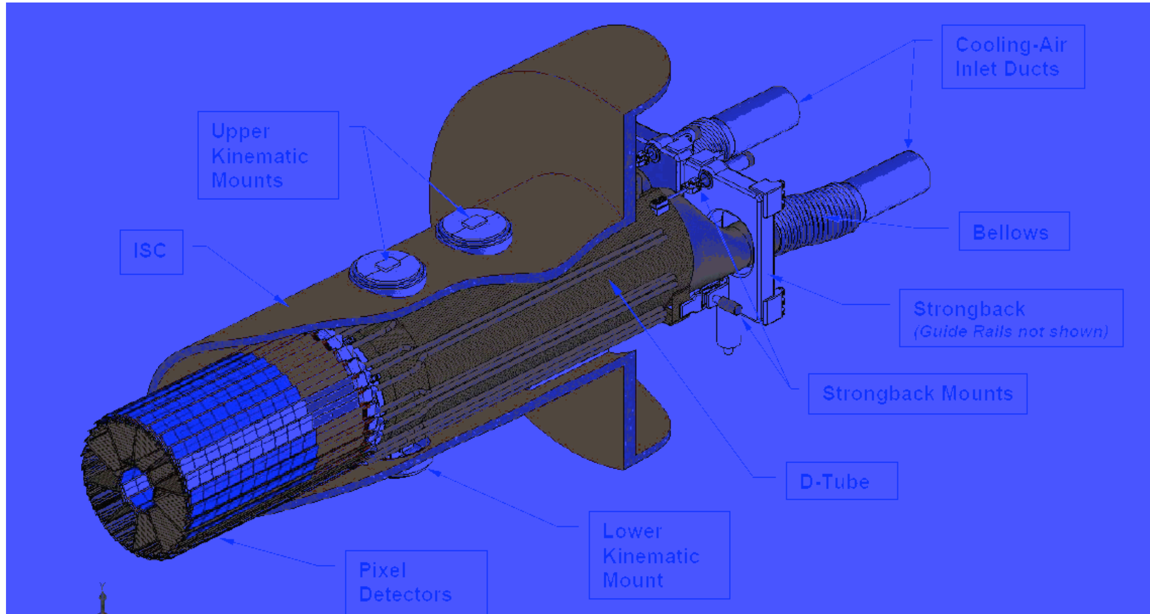


Figure 20: Detector assembly in the installed position supported with three kinematic mounts.

A more detailed view of the kinematic mounts is shown in Figure 21. The mounts provide a 3-2-1 constraint system which should allow repeatable installation to within a few microns.

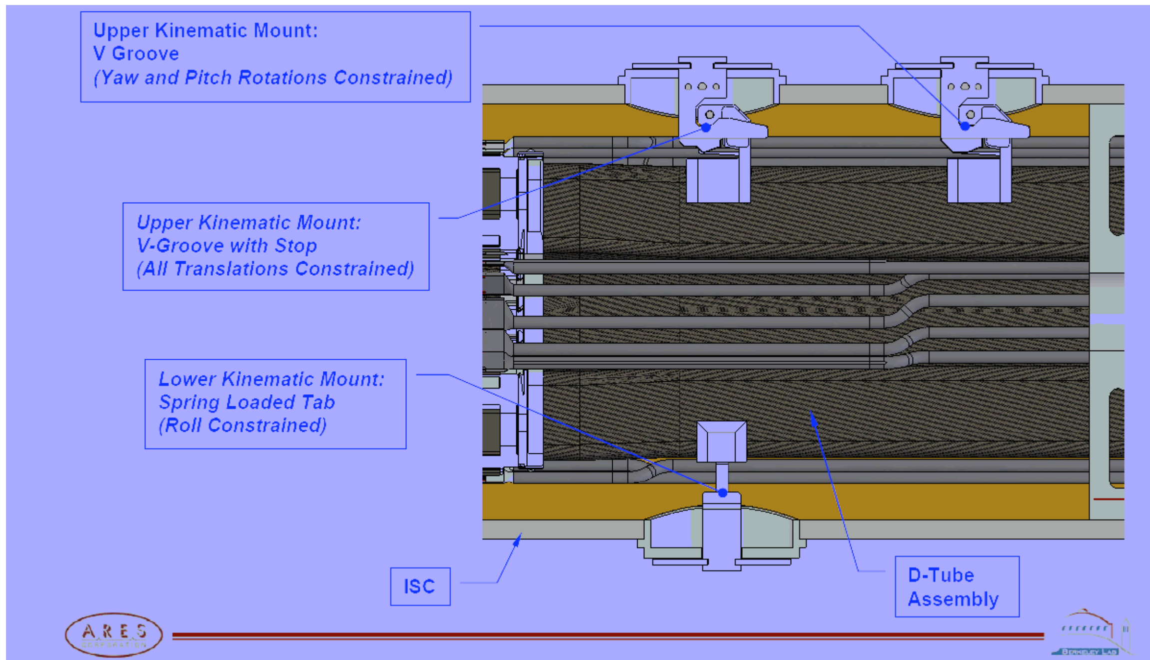


Figure 21: Detailed view of the kinematic docking mounts for the pixel detector. The mounts provide a fully constrained support and operate with a spring loaded over center lock down.

Insertion mechanism and Installation

The mechanics have been design for rapid installation and replacement. Instillation and removal of the pixel detector will be done from outside of the main STAR system with minimum disruption to other detectors systems. This will be done by assembling the two halves of the detector on either side of the beam pipe on rails outside of the STAR magnet iron. The detector carriage will be pushed into the center of STAR along the rails until it docks on the kinematic mounts. As shown in Figure 22 and Figure 23 the hinged support structure is guided by cam followers to track around the large diameter part of the beam pipe and close down at the center into the final operating position. Once the detector is docked in the kinematic mounts the hinged support from the carriage is decoupled allowing the kinematic mounts to carry the light weight detector system with a minimum of external forces affecting the position of the detector barrels. The external loads will be limited to the cables and the air cooling ducts. The cables are loosely bundled twisted pairs with 160 micron conductor plus insulation, so this load should be minimal. The two inch cooling ducts will be the greater load and may require additional design effort to isolate their effect so that the 20 micron position stability for the pixels can be maintained.

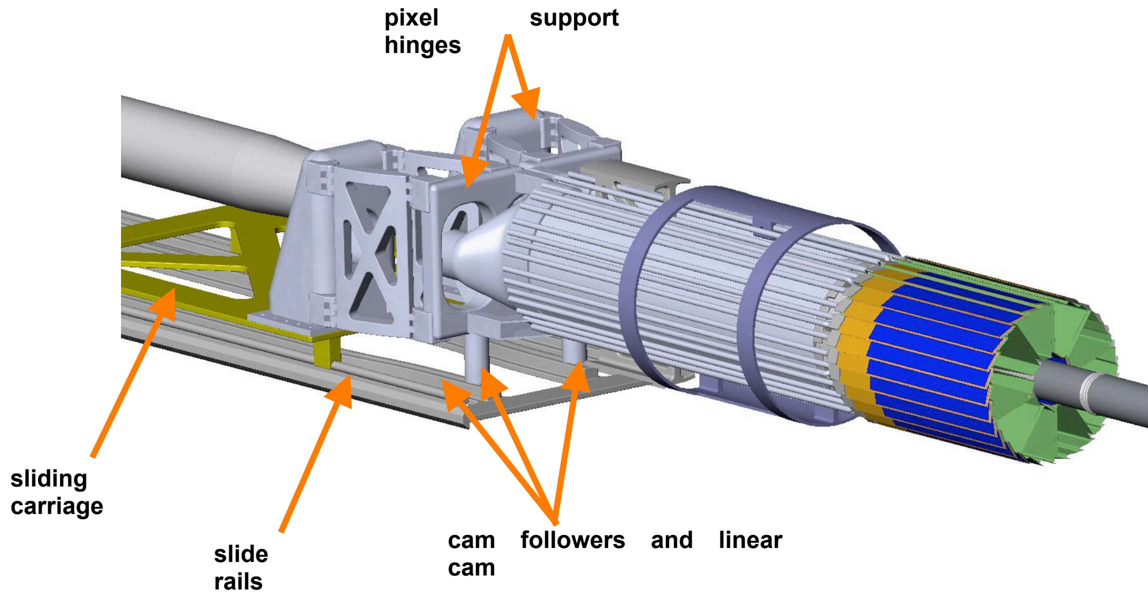


Figure 22: Track and cam guide system for inserting the detector.

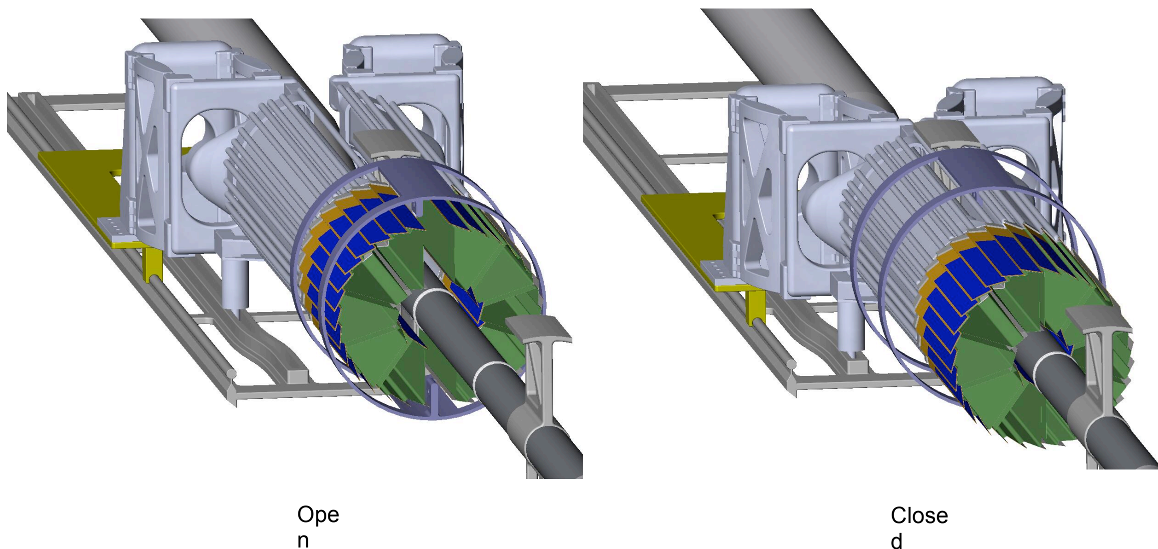


Figure 23: Initially the detector halves have to be sufficiently open to clear the large diameter portion of the beam pipe. It then closes down sufficiently to fit inside the IFC while clearing the beam pipe supports and then finally it closes down to the final position with complete overlapping coverage of the barrels.

Kinematic support

Cooling system

Cooling of the detector ladders with pixel chips and drivers is done with forced air. The pixel chips dissipate a total of 160 watts or 100 mW/cm^2 and an additional 80 watts is

required for the drivers. In addition to the ladder total of 240 watts some fraction of this is required for voltage regulators and latch up electronics that are off the ladder but reside in the air cooled volume. The temperature of operation is still under consideration. An optimum temperature for the detectors is around 0 deg C, but they can be operated at 34 deg C without too much noise degradation. The cooling system design is simplified if we can operate at 24 deg C, slightly above the STAR hall temperature, however if the cooler temperature is required the cooling system will be equipped with thermal isolation and condensation control when the system is shut down. In any case the design will include humidity and temperature control as well as filtration. Cooling studies (see Appendix 2) show that air velocities of 8 m/s are required over the detector surfaces and a total flow rate of 200 cfpm is sufficient to maintain silicon temperatures of less than 12 deg C above the air temperature.

The detector cooling path is shown in Figure 24. Air is pumped in through the support beam. A baffle in the ISC forces the air to return back over the detector surfaces both along the beam pipe and along the ISC.

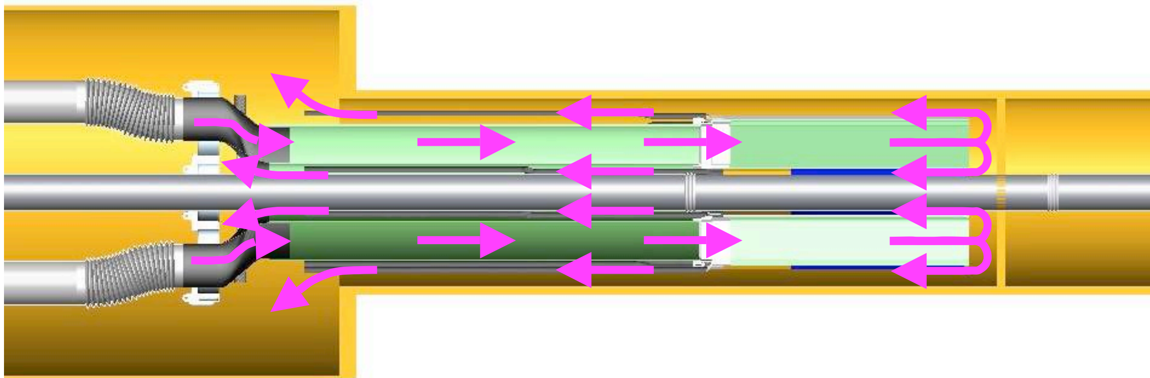


Figure 24: Pixel detector cooling air path. The air flows down the center of the sector modules and returns back over the detector ladders on the sector modules and into the larger ISC volume where it is ducted back to the air cooling unit.

The air chiller system providing the cooling air circulating through the pixel detector has not been completely specified yet, but sizing and ducting have been investigated for a system (see Figure 25) with 400 cfpm capacity (twice currently expected requirement). A commercially available centrifugal pump with a 5 horsepower motor is sufficient for this system. It is expected that the chiller would be located in the wide angle hall within 50 ft of the pixel enclosure and would be connected with 6 inch flexible ducts. An estimate of the required chiller heat capacity is given in Table 5.

Air flow: 400 SCFM

Total pressure drop: 22 inches water

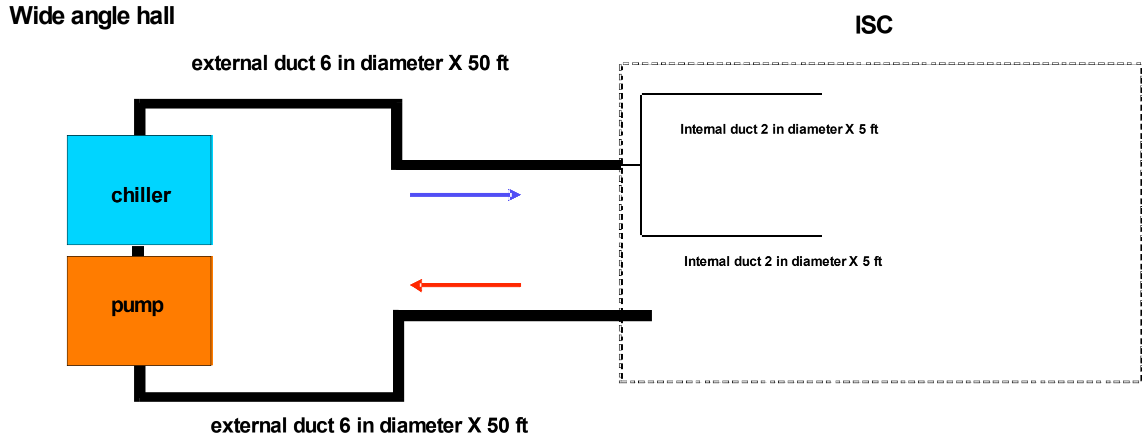


Figure 25: Schematic outline of air cooling system for the pixel detector.

Heat source	Power (watts)
detector silicon	160
on ladder signal drivers	80
voltage regulators in ISC	24
heat influx through ducting and ISC if 35 deg C below ambient	600 - 2000
pumping	1000
Total load on chiller	1900 - 3300

Table 5: Preliminary estimate of heat load on the chiller for the pixel air cooling system.

Cabling and Service system

The required wiring connections are identified in Figure 5. The 2 m fine wire twisted pair (pair diameter .32 mm) bundles leading from the ladders to the interface cards are designed to minimize mass, space and mechanical coupling forces that could disturb the pixel positions. The space envelope required for these bundles is illustrated in Figure 26.

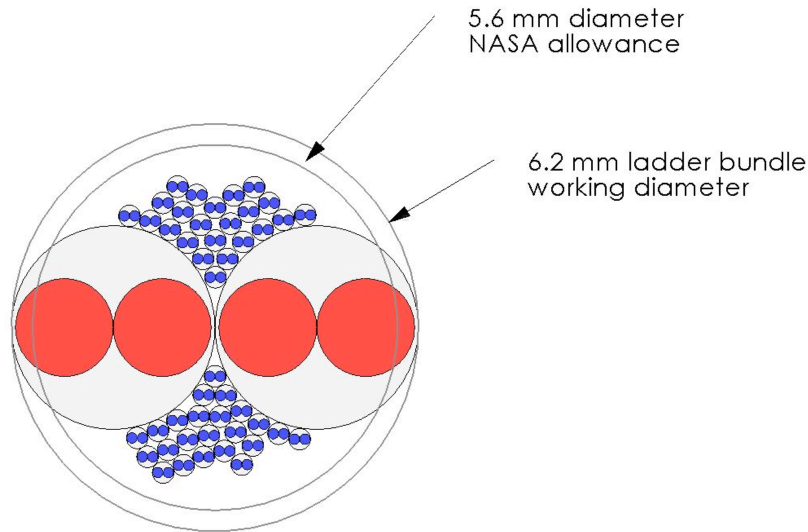


Figure 26: Cable bundle envelope for ladder connections. The blue pairs include 40 signal pairs, clock and trigger lines and JTAG communication. The red conductors are power.

There will be a 2'X2'X3' crate for the readout boards. This must be located outside of the main magnetic field and outside of the highest particle flux region. To achieve the required data transfer rates the LVDS signal cables running between this crate and drivers inside the ISC are limited to 6 meters. To meet these constraints the readout crate will a be located on the floor at the end of the magnet (there is no space on the magnet end ring for mounting the readout box). This will allow operation of the pixel system both with and without the pole tip in place (there is no space on the magnet end ring for mounting the readout box). The crate will be portable on wheels to accommodate end cap access requirements. Compared to the cables running to the detector the power and fiber optic cables from the readout crate to the outside are relatively small and provide little handling burden.Installation

Alignment and spatial mapping

The pixel system is being designed to have full pixel to pixel spatial mapping at installation with a 3D tolerance envelope of 20 microns. This will eliminate the need for spatial calibration with tracking other than determining the 6 parameters defining the pixel detector unit location relative to the outer tracking detectors. Tracking, however, can used with the pixel detector to spatially map the outer detectors if required.

The mapping and alignment will be done by using a vision coordinate machine to determine the detector locations on the fully constructed 20 ladder half modules. A full 3D map of the ladders is necessary since the manufactured ladder flatness will exceed the 20 micron envelope. After mapping the half modules will be installed in STAR without disturbing the relative positions of the pixels.

Addressing this in more detail, a support fixture for the half modules will be used in the vision coordinate machine which has kinematic mounts identical to the kinematic mounts in the ISC for securing the half module. The pixel chips will be manufactured with

reference targets in the top metal layer that can be picked up by the vision coordinate machine and the ladders will be mounted such that there is an unobstructed view. The fixture will be rotated for each ladder measurement. Full 3D measurements of the chips on the ladder are required since the ladder flatness will lie outside of the 20 micron envelope. The fixture will have precision reference targets on each ladder plane so that the ladder points can be tied together into a single coordinate frame. The map of the fixture targets can be measured once with a touch probe measuring machine and thus avoid extreme machining tolerance requirements for the fixture. Precision machining, however, will be required, for the kinematic mounts and their placement tool.

For this approach to work the ladders must hold to their mapped position within 20 microns independent of changes in temperature, humidity and gravity direction.

The detector ladders have 1 mm overlapping active regions with their neighbors, so a check of the mapping accuracy will be done with tracking.

3.2.6. Mechanical Design Simulation and Prototyping

Ladder support Structural analysis

Ladder support prototype development

Ladder cooling analysis

Ladder cooling prototype tests

Insertion prototype tests

Kinematic support tests

3.3. The Intermediate STAR Tracker

3.3.1. Introduction

To reach the full physics capabilities of the HFT, the PIXEL sub-system requires tracks with good pointing resolution at its outer layer and an as good as possible track finding efficiency. TPC tracks alone provide a pointing resolution of around 1000 μm at the outer layer of the PIXEL sub-system which then leads to a single track finding efficiency of about 50%. The SSD layer at a radius of 23 cm improves the pointing resolution to approximately 400μm in the bending direction with an efficiency of about 80%.

The HFT with the SSD alone would provide in principle sufficient pointing resolution and single track finding efficiency. However, there would be no redundancy against failing of (parts) of the SSD. Since the SSD is an aging detector this is considered to be an unacceptable risk to the physics program of the HFT. A relatively simple tracking layer between the SSD and the outer layer of the PIXEL should be able to correct this deficiency.

The Intermediate Silicon Tracker (IST) will provide space points with high accuracy in the bending direction without degrading the single track finding efficiency by more than a few percent due to added material. The IST will make use of silicon pad sensors with strip-like pads located at a radius of 14 cm. Various technical details draw to a large extent from previous experience on the design and operation of silicon tracker systems such as the PHOBOS silicon tracker stations. The construction of the IST will make use of existing equipment and infrastructure from the PHOBOS silicon tracker through the MIT group.

3.3.2. Requirements

Overview

The IST must meet a number of tracking requirements and should also be able to cope with the experimental constraints.

The best figure of merit for the tracking capabilities is the final D0 reconstruction efficiency. However, determining this efficiency involves extensive GEANT simulations and analysis. The choices that are presented here to meet the requirements are based on a much more simplified tracking code which has successfully been checked against the full calculations in a number of major cases. This simplified code was used to determine the optimum radius of the IST barrel and the internal geometry of the silicon pad sensors.

The most important of the experimental constraints are data taking rate capabilities, radiation levels and the material budget. The data rate and radiation levels are constrained by the RHIC environment and have to be taken into account in the sensor and readout chip choice. The material budget connected to the tracking capabilities of the inner tracking system, but has also a large impact on the capabilities of more outward

located detectors and their associated physics programs. To produce a low mass IST with enough mechanical rigidity has led to the choice of state of the art materials.

Tracking tasks

The Intermediate Silicon Tracker has to be located between the outer layer of the PIXEL detector and the SSD. Taking mechanical constraints into account this gives a possible radius range from 12 to 20 cm. This radius has to be optimized for reconstruction efficiency while keeping SSD and IST redundancy in mind.

The IST barrel should cover the full acceptance of the STAR TPC, i.e. 2π coverage for $-1 < \eta < +1$. In addition the IST should also be able to accommodate some of the z-range of the interaction point.

At the highest RHIC energy of 200 GeV for Au+Au collisions the charged particle density at a radius of 12 cm can easily exceed 1 per cm^2. The internal structure of the silicon sensors has to be chosen such that the occupancy does not exceed the few percent level.

Tracking efficiency

The tracking efficiency is defined as the percentage of correct single tracks found by the inner tracking system when presented with events with only one track. This efficiency can be found by a full simulation with GEANT and the STAR tracking analysis. A faster way is to calculate the efficiency with the more simple code described in section XXX. This code calculates the efficiencies for 750 MeV/c kaons which is important because these are the particles that need to be tracked for D0 reconstruction. The whole inner tracking system should have a single track efficiency of better than 80%. If the SSD or the IST is not able to provide a proper space point for the track, because of less than 100% coverage or broken channels, then the efficiency should still be above 70%.

Data taking rate

The IST should be able to operate without significant event pile-up for 200 GeV Au+Au collisions. Therefore, the IST has to be able to resolve interactions from each beam bunch crossing which are occurring every 116 ns. The spin program at RHIC relies on individual beam bunch crossings to set and determine the relative spin orientations in the proton beams. Also here the IST should be able to resolve individual beam bunches.

Radiation environment

Extrapolating the radiation doses received by the RHIC experiments during the past RHIC operations, it is expected that the total radiation dose for the IST barrel will not exceed 30 kRad per year. Both the silicon sensors and the readout chips on the hybrids are required to be fully operational after 10 years of operation.

Low mass and mechanical stability

The mass requirements for the IST are defined by the heavy ion physics requirements in the mid-rapidity region and by the W−boson spin physics program for more forward rapidities. The heavy ion vector meson program, going to di-electrons, was marginal given the mass of the SVT when it was still installed in the mid-rapidity region. Similarly, the upsilon program was marginal with the SVT. The PIXEL plus IST should thus strive to be much thinner than the current azimuthally averaged 4.5% radiation lengths of the SVT. The W−physics spin program was hindered by SVT support structures in the pseudo-rapidity region of $1 < \eta < 2$. Support structures for the inner tracking system should be designed to reduce mass in this region. To make the Multiple Coulomb Scattering comparable to the detector resolution the thickness of the IST layer should be less or equal 1.5% of a radiation length.

3.3.3. Design choices

Barrel radius and layout

The efficiency of the whole inner tracking system is determined by an intricate interplay of the detector layer radii, resolutions and thicknesses. Since these characteristics are mostly fixed for PIXEL and SSD, varying the radius of the IST barrel for a certain internal sensor geometry makes it possible to optimize the radius with respect to the single track efficiency quickly. Figure 27 shows a calculation for a promising internal geometry. Although the dependence is rather weak it is clear that 14 cm will give the best efficiency. Not too surprising is that this is roughly halfway between the outer layer of PIXEL and the SSD.

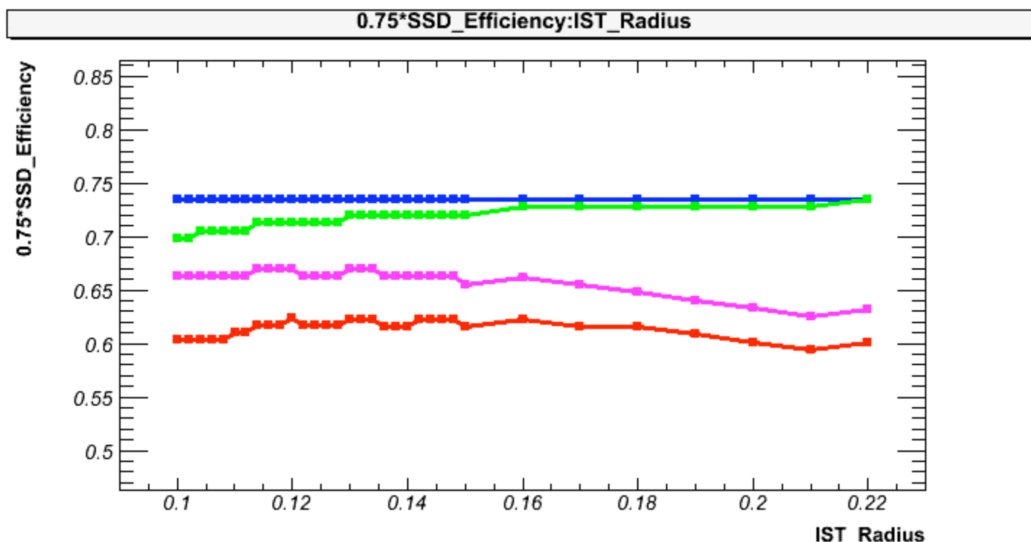


Figure 27: Single track efficiency as function of the IST barrel radius. The assumed internal sensor geometry was 600 μm in r-φ and 6000 μm in z.

The rest of the layout of the layout of the IST barrel is for the most part determined by the size of the sensors and the requirement of 2π coverage for $-1 < \eta < +1$. Figure 2 shows an X-Y cross section of the inner tracking system and Figure 28 a 3D rendering of the IST barrel. For the anticipated sensor layout there will be 24 layers tiled to give 2π coverage. The barrel will be 62 cm long and cover $-1.5 < \eta < +1.5$.

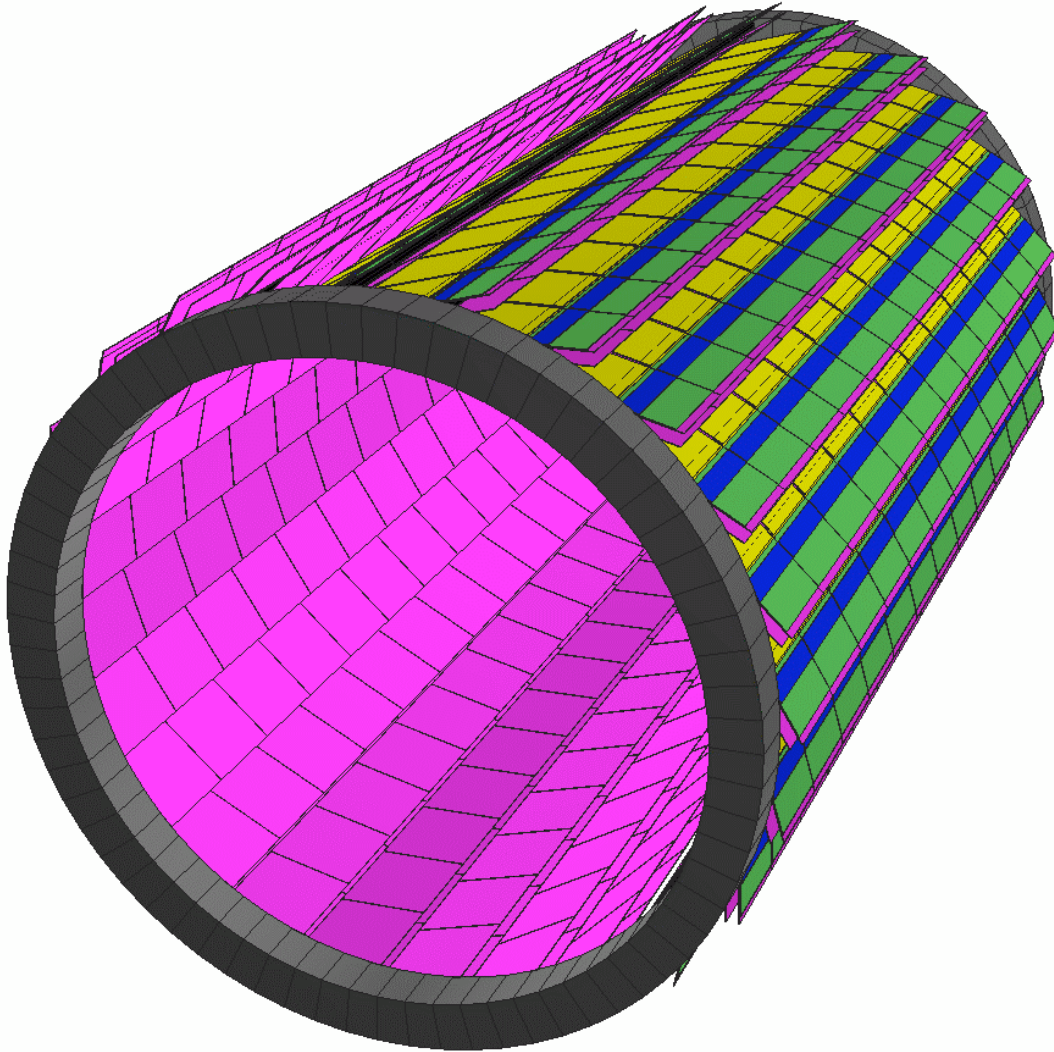


Figure 28: IST barrel layout with 24 ladders of 62 cm long at a radius of 14 cm.

Silicon detectors

The manufacturing techniques for silicon sensors are well established and are mastered by several manufacturers. The preference is to produce single sided devices with p-implants on n-bulk silicon and poly-silicon biased. They are relatively easy to produce with high yields and can also be handled without much difficulty in a standard semi-conductor lab. In contrast, double-sided devices have lower yields (thus more expensive) and need special equipment to handle them.

Central Au+Au collisions at 200 GeV lead to a particle density of about 1 per cm^2 at the IST barrel near mid-rapidity. Using silicon strip sensors would lead to unacceptable occupancies and double hit probabilities.

Silicon pad sensors are much better suited to this environment and proved their suitability in the PHOBOS experiment. Figure 29 shows a study of the single track finding efficiency of the whole HFT as a function of the pad layout of the IST sensors. The better resolution (the size of the pads on the y-axis) is in r-phi, the bending plane. From these studies it was determined that 512 channels arranged in strips of roughly 600μm X 6000μm give an acceptable efficiency of about 83%. Going to more channels could give a slightly better efficiency but would lead to space problems when trying to mount more readout chips on the hybrids. The left plot shows the efficiency when hits from the SSD are not included in the tracking. This could happen because of small gaps in the SSD acceptance or broken channels. This study shows that the single track finding efficiency goes to 73%. This has to be compared to 50% if the IST would not be there and only the TPC would provide tracking to the PIXEL. The IST greatly adds to the redundancy of the inner tracking system.

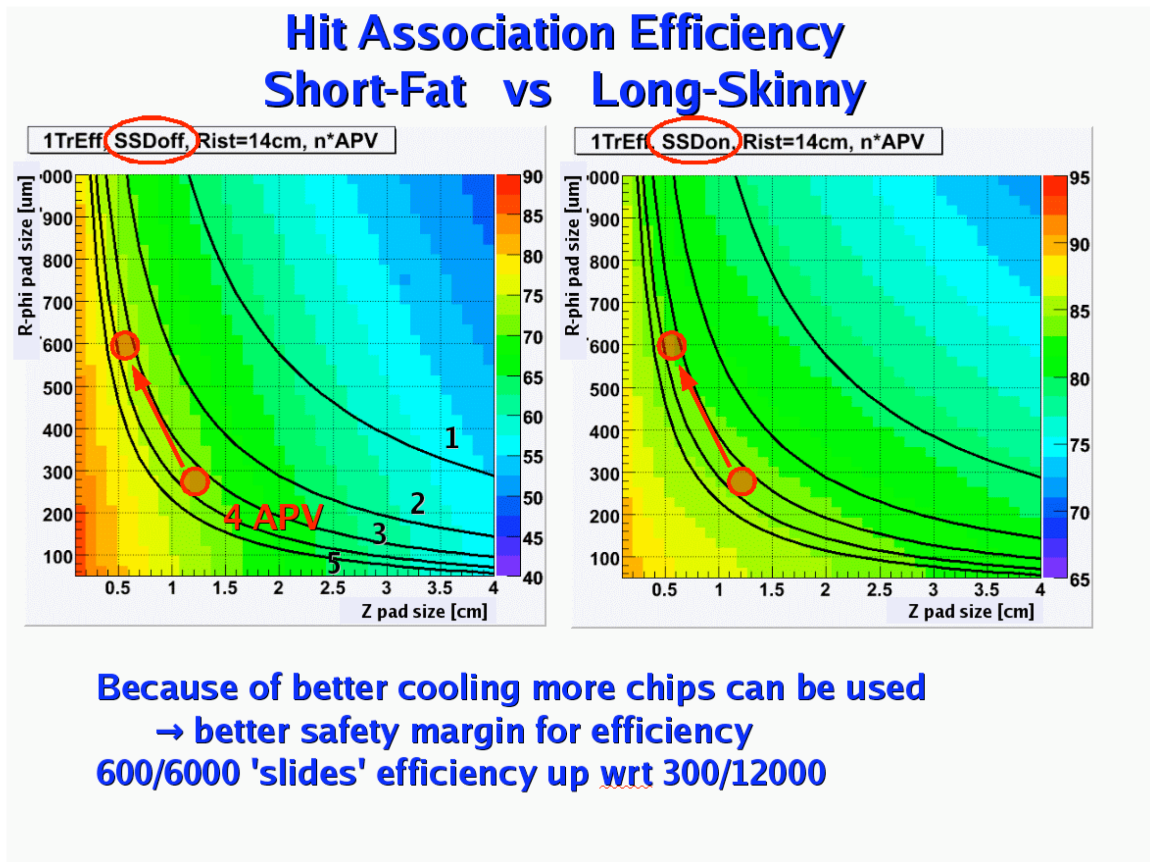


Figure 29: Single track finding efficiency for different r-phi and z pad sizes of the IST. The solid lines show the iso-lines for certain amount of channels (1 = 128ch, 2 = 256ch, 3 = 384ch, 4 = 512ch, 5 = 640ch). The left picture shows the efficiency when no hits from the SSD are included, in the right picture the SSD hits are included in the track. Particles tracked are kaons at 750 MeV/c.

Figure 30 shows the internal layout of the IST silicon pad sensors. The active elements are arranged in such a way that the best resolution is in the bending direction, i.e. r-φ. Along the beam direction the resolution will be ten times larger. The sensors will be roughly 10 cm X 4 cm with 1024 channels. All channels are AC coupled and connected through a second metal layer to bonding pads on one long edge of the sensor. From the manufacturing point of view this design is reasonably standard. Preliminary discussions with Hamamatsu showed that they are able to produce the proposed sensors within the proposed budget.

Hamamatsu is the preferred vendor because of their excellent track record with respect to the quality of their produced sensors. This will greatly reduce the amount of quality control that has to be performed for these sensors. It will be sufficient to fully measure the characteristics of one or two samples per produced batch of about 20 sensors. Moreover, Hamamatsu uses design rules which make their sensors relatively radiation hard. Therefor we foresee no serious performance degradation during the sensor lifetime.

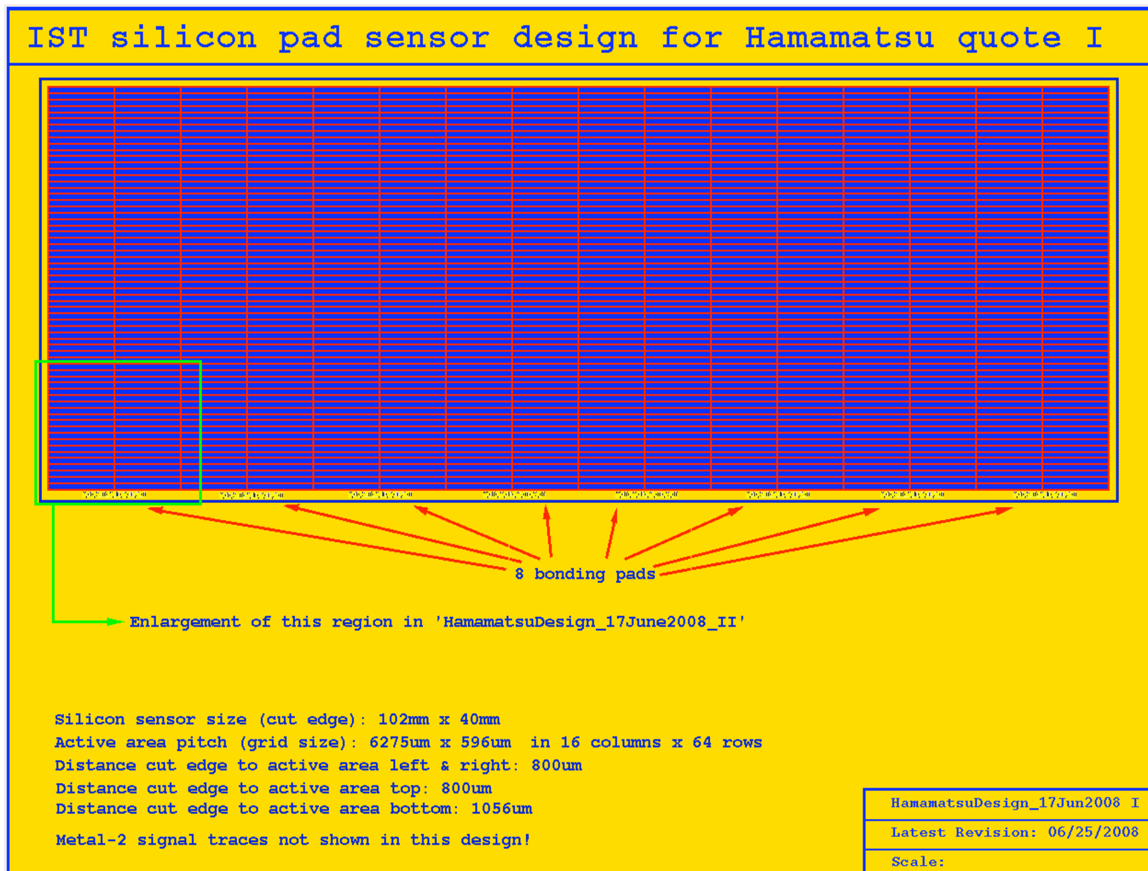


Figure 30: IST silicon pad sensor internal layout.

Read-out chips

About 150,000 channels will be read out in the IST. Readout chips with the necessary requirements for this system are already being used for similar purposes by other experiments. We chose the APV25-S1 readout chip which was designed for the CMS

silicon tracker and of which about 75,000 will be used in CMS. Each channel of the APV25-S1 chip consists of a charge sensitive amplifier whose output signal is sampled at 40 MHz which accounts for the LHC interaction rate. The samples are stored in a 4 μs deep analog pipeline. Following the trigger the data in the pipeline can be processed by an analog circuit, mainly de-convoluting the amplifier response from the actual signal and associating the signal with a certain interaction (or rather beam crossing at LHC). The resulting analog data can then be multiplexed and sent to digitizer boards. Although the analog data leads to higher data volumes at the front-end, it is an enormous advantage that charge sharing between strips and common mode noise can be studied in detail, which greatly improves the understanding and performance of the detector. The Equivalent Noise Charge (ENC) of the APV25-S1 depends on the capacitance of the strips and the de-convolution algorithm used, but, for our purposes, it is better than 2000 electrons. With 300 μm thick silicon sensors this will give a signal-to-noise ratio of better than 11:1 when we take the most probable energy deposition by a minimum ionizing particle (MIP). The nominal power consumption of the APV25-S1 is 2.31 mW/channel, i.e. about 0.3 Watt/chip. The chips are fabricated in the radiation hard deep sub-micron (0.25 μm) process. Figure 31 shows a close-up view of the APV25-S1 chip.

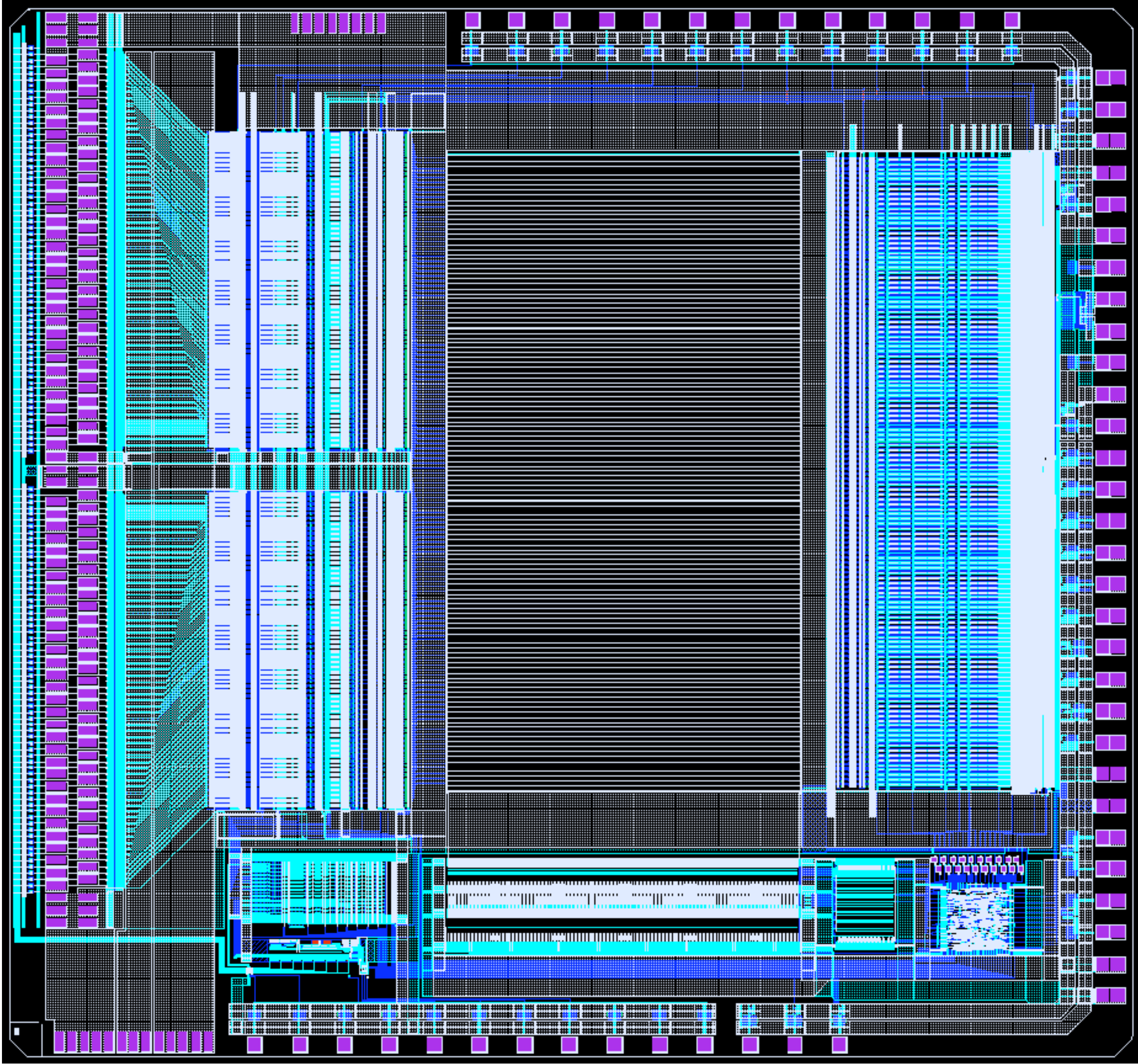


Figure 31: Close-up of the APV25-S1 chip of which the IST will use about 1200.

Hybrids and modules

To keep the material budget low the IST hybrids and modules have to constructed from low mass materials. Figure 32 shows a promising prototype Kapton hybrid design with integrated long Kapton cable. Both hybrid and cable are about 100μm thick. The hybrid will have to be laminated onto a proper substrate material to achieve enough mechanical rigidity. Carbon-Carbon and carbon fiber are being prototyped to study their mechanical and thermal properties. In the final design the flexible cable will be long enough to reach the readout electronics outside the TPC area (~400cm) or to reach a connection to more standard cables outside the active areas which are sensitive to too much material (~100cm). Both lengths pose no production problems. The main concern is the electrical characteristics of the long cable, this is under investigation. The hybrid in Figure 32 has been taken into production.

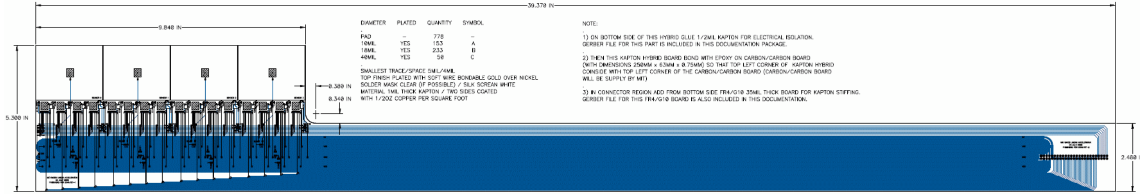


Figure 32: IST hybrid (left) and cable (right) assembly.

The layout of an IST module can be seen in Figure 33. The hybrid carries 2 sensors of the type shown in Figure 30 and 16 readout chips. There will be a gap of 400μm between the sensors. Overlapping the sensors would lead to too many assembly complications. These acceptance gaps will be compensated because of the redundancy between SSD and IST. An interesting feature, and which is not visible in this picture, is that the cable will be folded over to the backside of the ladder on which this module will be mounted. In this way the cables are neatly tucked away and do not obscure visual access to the modules, which is needed for spatial survey purposes and inspection.

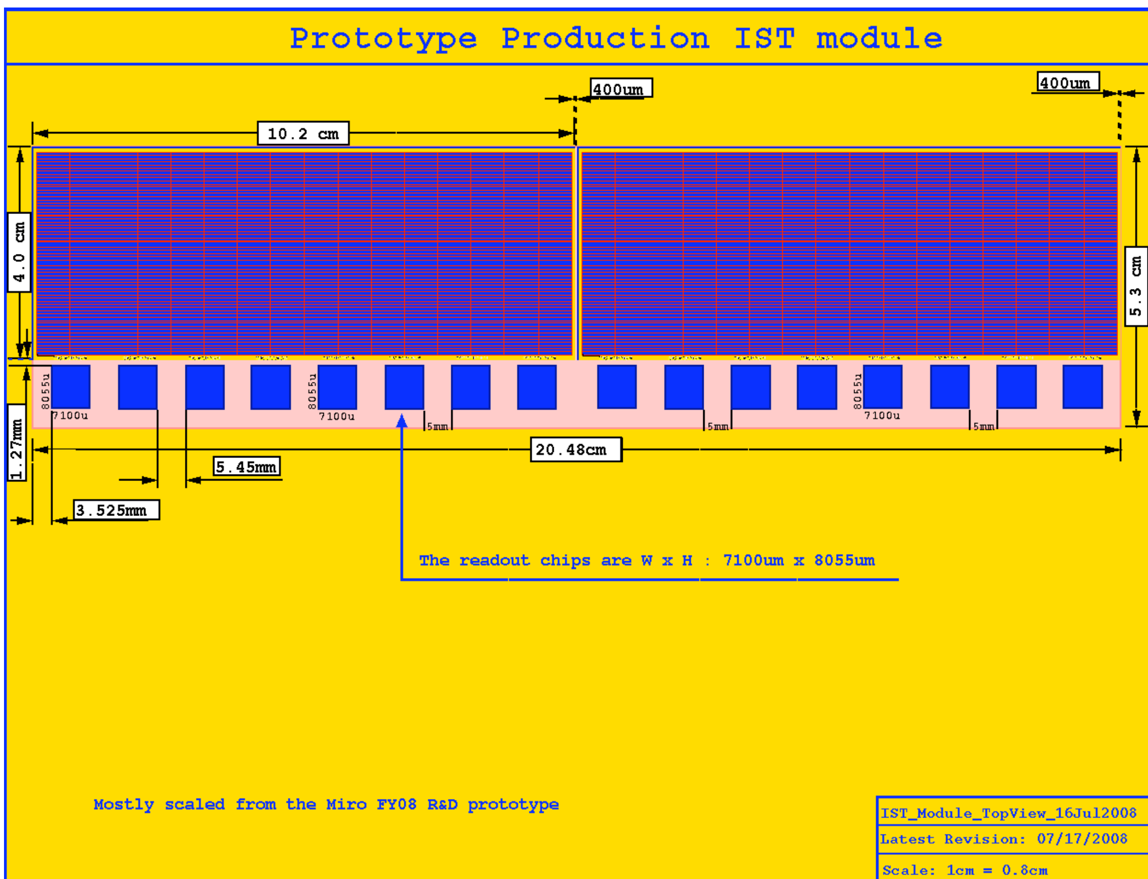


Figure 33: Layout of an IST module.

Mechanical support structure

The IST barrel will consist of 24 ladders which get mounted on a carbon fiber support cylinder. The Inner Support Cylinder (ISC) is described elsewhere in this document and has not been taking into account in the material budget calculations.

Figure 34 shows the ladder structure of the IST with and without the modules mounted. This ladder is a shorter version of the staves which are under development for the ATLAS tracking upgrade. Because they are shorter they are even more rigid than the ATLAS staves and it is expected that their midpoint sag will be less than 100μm when only end supports are used. A prototype ladder is being produced and will be tested.

A more detailed cross section of the ladder and mounted modules can be found in Figure 35. This design shows the 300μm thick silicon sensor, the 300μm thick APV25-S1 readout chip, the 100μm thick kapton hybrid-cable, the 500μm thick Carbon-Carbon substrate and the 5 mm thick carbon fiber ladder with cooling tube. It also shows nicely how the kapton folds over to the backside of the ladder where it is routed out to the readout system. The Carbon-Carbon substrate not only gives mechanical rigidity to the module, but also acts as a heat sink to transport heat from the readout chips to the cooling tube in the ladder.

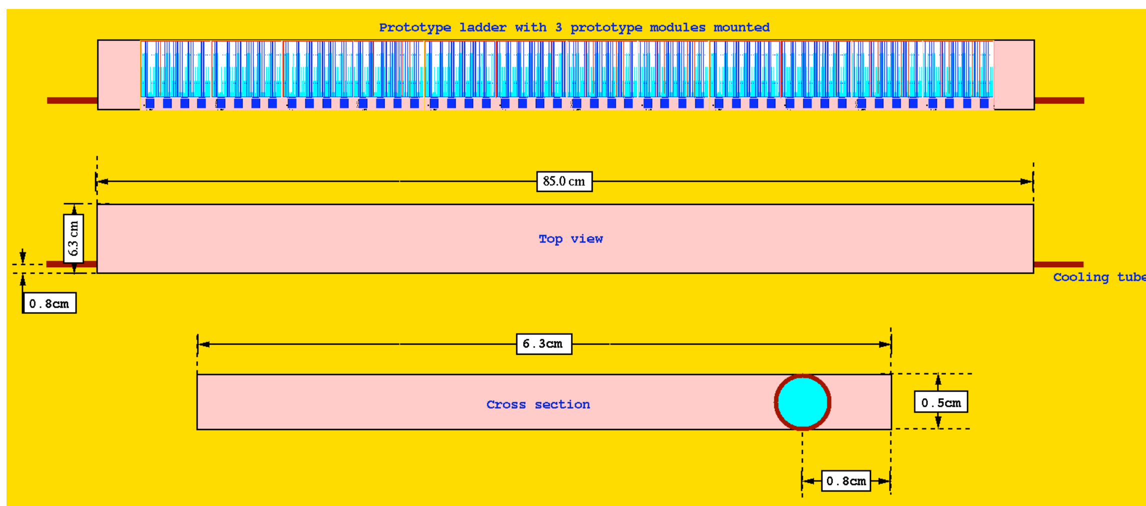


Figure 34: Drawings of the IST ladder. Top picture is with modules attached, middle picture shows the bare ladder and bottom picture shows a cross section of the ladder.

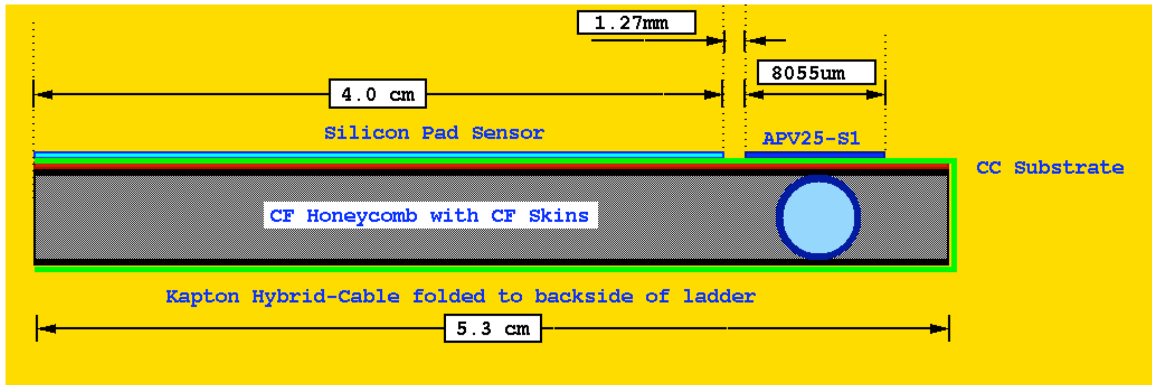


Figure 35: Cross section of the ladder and modules. Especially note the kapton hybrid which gets folded over to the other side.

The options for mounting the ladders on the Inner Support Cylinder are still under investigation. Again it would be benficial to profit from the extensive research that the ATLAS upgrade group has done for the upgrade staves and support. Figure 36 gives an artists impression of one of the more promising designs. Here the ladders would be mounted with clips on the ISC. Because of the shorter length of the IST ladders it is probably sufficient to use endpoint supports only. One end of the ladder would be kept fixed while the other end allows thermal expansion. Most likely there will have to be an clamshell interface on which the ladders are mounted first. This clamshell can then be optically surveyed to determine the sensor positions before it gets mounted on the ISC.

The mechanical support structure will be manufactured with an overall accuracy of 100 μm. Locally, the structure supporting the IST requires an accuracy of less than 100 μm. For instance, the mounting surfaces of the sensor modules will have to be flat to within 50 μm to avoid stress, and possibly breakage, of the sensors.

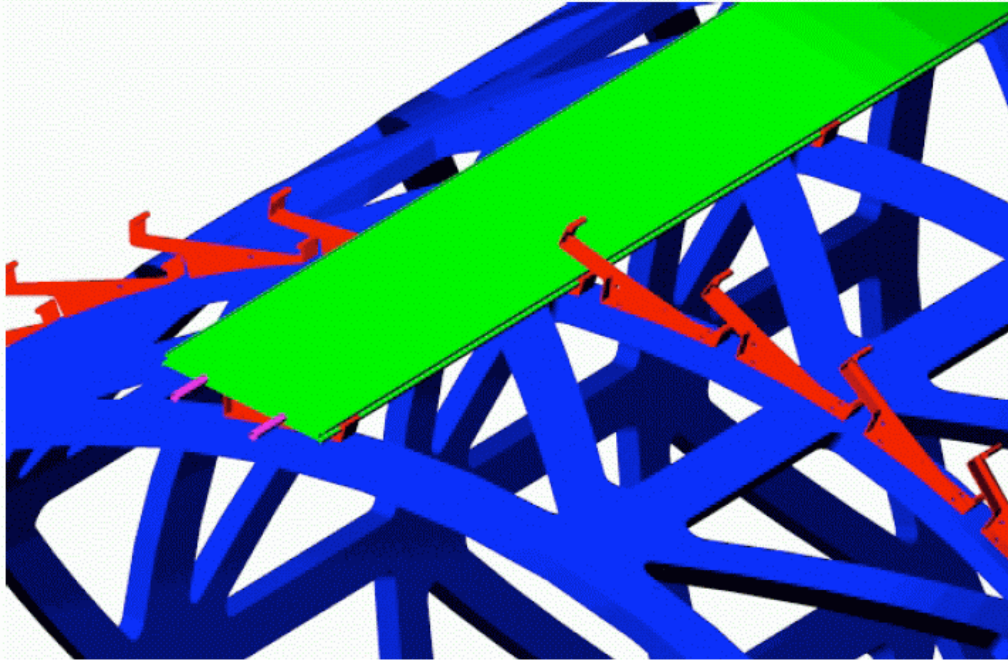


Figure 36: Ladder 'clip' mounting of the IST ladders onto the supporting cylinder (ISC).

Figure 37 gives a realistic estimate of the IST material budget by describing ladder and module designs in a GEANT geometry. These results where obtained by propagating 100,000 geantino events through the IST geometry using GEANT 3.21/08. The material budget at mid rapidity is well below the required 1.5% X_o. However, it should be noted that, because of a lack of a design, the ISC and support clips where not included in these calculation. The asymmetry in the material budget is caused by the kapton readout cables only running in negative rapidity direction.

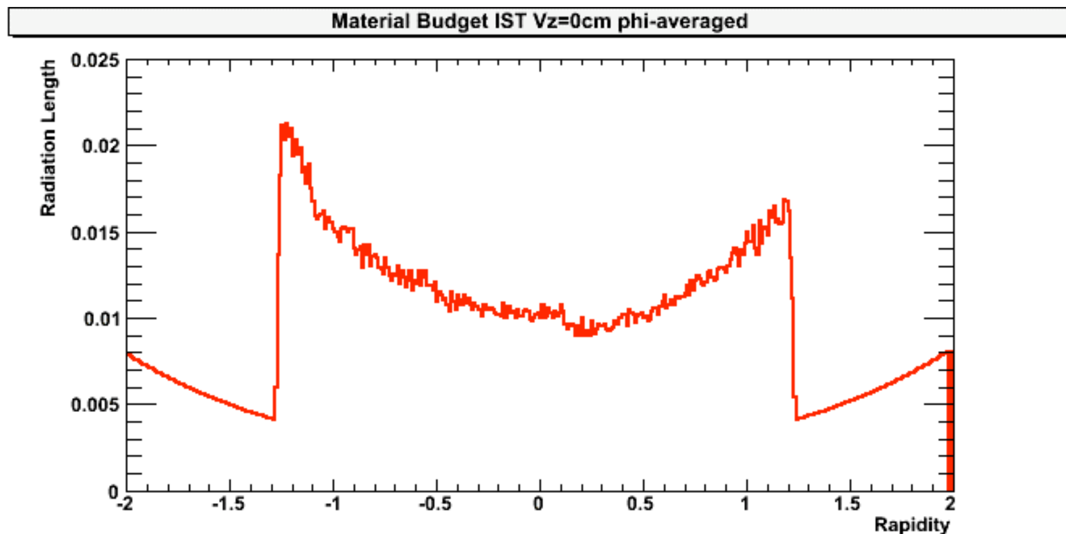


Figure 37: Phi averaged material budget for the IST as a function of rapidity.

Cooling

The only source of dissipation on the ladders are the 48 APV25-S1 readout chips. Athough the nominal power consumption is about 300mW per chip, the final power consumption is depending on the capacitance of the attached sensor channels and the optimal settings of the chip parameters. For safety margin reason a maximum dissipation of 400mW per chip is assumed. This leads to a dissipation of about 20 Watt per ladder, 480 Watt for the whole IST barrel. Trying to cool this with air only was considered too daunting and liquid cooling channels were incorporated in the ladder design. The 20 Watt per ladder leads to about 1.2mW per mm^2 dissipation if the heat would spread out isotropically. The placement of the cooling tube directly under the readout chips and the use of high thermal conductive material like Carbon-Carbon should make the cooling of the ladders manageable with a room temperature water cooling system.

3.3.4. Readout system and Slow Controls

Readout system and DAQ interfacing

Three Wiener readout crates, each containing 9 slots, will house the 8x2 read-out boards (RDO) and 1x2 crate controller boards (RCM). These crates, 6U in size and powered by remote supplies, will be mounted on the electronics platform next to the STAR detector. Just outside the inner TPC area there will be transition boxes translating the thin and fragile Kapton cables to more standard detector cables which connect to the RDO. Each RDO handles three detector cables (48 APV chips), providing an ADC, some data buffering and control of APV chip triggering and readout sequencing. The RDO also operates the I2C slow controls interface to the detector. The RCM interfaces to the STAR trigger and DAQ via the ALICE detector data link (DDL) source interface units (SIU), the standard for all new STAR DAQ-connected developments for the DAQ1000, Time of Flight (TOF), Barrel (BTOW), Forward GEM Tracker (FGT) and Endcap (ETOW) tower level 2 upgrade. The readout system, as designed, will be able to transmit data to L2 following the same plans as for TOF, ETOW, FGT and BTOW. A Linux box will be located in the STAR DAQ room and fitted with the ALICE DDL receiver board and a Myrinet interface to the event builder computer. A schematic detailing these connections is shown in Figure 38.

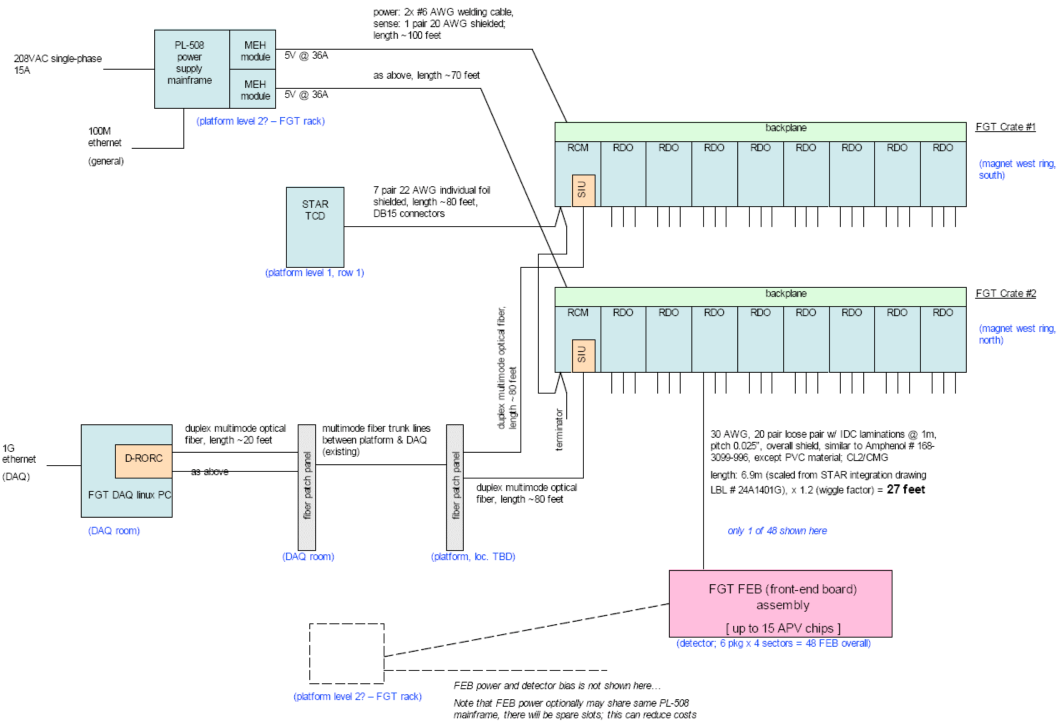


Figure 38: IST DAQ block diagram.

Slow Controls System

The slow controls system will serve as the primary means for controlling and monitoring the working parameters of the IST. These parameters, such as the hybrid temperature, component currents, voltages and gas flow rates, will be interfaced with the standard STAR alarm system. The alarm system logs the parameter history and alerts the shift crew if operating limits are exceeded. The black dashed lines in Figure 39 show the communication flow between the slow controls computer and the hardware being controlled. The red solid lines represent the actual hardware connections which allow this communication. The slow controls for the IST detector and readout crates will be handled exclusively by Ethernet traffic to the IST Linux box, through the ALICE DDL link to the readout crates, and then finally through the RDOs to the APV's via the local I2C link. There will be no other hardware needed for slow controls. All power supplies will be fitted with an Ethernet controls interface.

Although STAR is using EPICS as its standard slow control system there is a slight preference to use LabView instead. LabView provides the user with virtually any instrument driver and a very convenient user interface. LabView runs on both Windows and Linux. It is relatively simple to interface LabView and EPICS. However, at the moment, both options are still open.

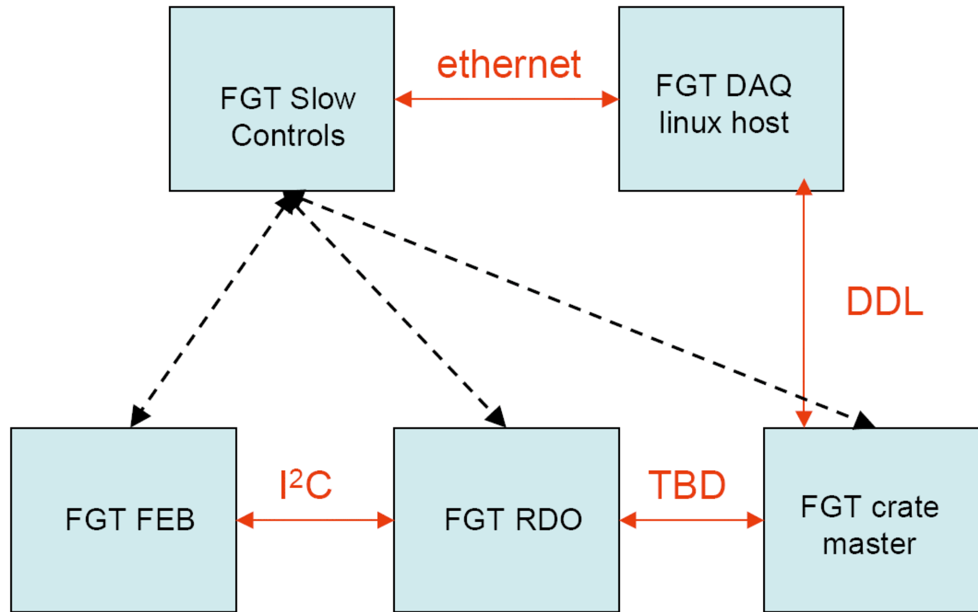


Figure 39: IST slow controls flow diagram.

3.3.5. Spatial survey and alignment

The IST will have to be aligned with respect to the other detector in the inner tracking upgrade, PIXEL and SSD. The final alignment will be done with tracks through an iterative residual method. However, for this method to be successful it is important that the positions of the active elements are known in advance with an accuracy comparable to the resolution of the detectors. For the IST the following 5-step plan has to be followed to achieve this.

The positions of the sensors on the module have to be determined. Internally the structure of the sensors will be well known with an accuracy of about 1-2 μm. This information is obtained through the production mask drawings of the sensors and accessed through alignment marks on the sensors. The modules will be build on an assembly machine under control of an operator checking the process under a microscope. The expected placing accuracy is 5um. After the modules have been assembled they can be surveyed with an optical survey machine at MIT. The accuracy of this machine is about 10 μm in-plane. An out-of-plane contrast measurement leads to an accuracy of 50 to 100μm.

The same methods as for the module while be used for the ladders. Three modules will be glued to one ladder with an accuracy of about 5um. Then the ladder will optically survey with an in-plane accuracy of 10 μm and an out-of-plane accuracy of 50 to 100 μm. After the ladder gets approved it will be shipped to BNL where additional survey can take place. There is a possibility to do this on a coordinate measuring machine and/or by the BNL surveying group using state-of-the-art optical survey equipment.

At BNL the ladders will probably be put together in 2 clamshell cylinders which can be measured on a coordinate measuring machine or by the BNL survey group. After the clamshells have been put together on the ISC to form the IST barrel another survey needs

to take place. Up to this point it should be possible to survey the silicon sensors themselves. The sensors have the highest internal accuracy (1-2 μm) and in the end it is their position which should be known with the best accuracy. However, after the clamshell has been closed visual access to the sensors will become impossible, especially after the ISC gets integrated with the rest of the inner tracking system. It is important to have survey points on the ladders, the clamshell structure and the ISC which are visible to the BNL survey group. These survey points then 'anchor' the IST inside the inner tracking system and finally to the whole STAR detector. It is extremely important that the BNL survey group is involved from the beginning in planning the whole survey process.

Finally, the inner tracking system (PIXEL, IST and SSD) get mounted inside of the STAR TPC. Its location will be determined by the BNL surveyors through optical survey.

All the information which has been gathered in the previous steps will be used to do a least squares fit for the positions of the IST silicon sensors. Since there are only 144 sensors it will be possible to do some hand checking and possible correction of the results. These positions will then go into the STAR tracking geometry and acts as a starting point for software alignment with tracks. This final process can easily take a couple of person months to achieve the desired level of confidence. Therefore, every effort should be made to have a sufficiently rigid construction. Removal of the detector will set a physics analysis back by months and should not be undertaken lightly.

3.4. The Silicon Strip Detector

The STAR Silicon Strip Detector SSD[2] (Figure 40) is a high resolution silicon detector that is mounted inside the inner radius of the STAR TPC at a radius of 23 cm. Its radial location puts it midway between the event vertex and the TPC. Thus, it is ideally suited for the purpose of improving the TPC's pointing and momentum resolution, and extending the physics program of STAR.

It was originally designed to work with the TPC and the STAR Silicon Vertex Tracker (SVT). The SSD will be upgraded so that it will be compatible with and enhance the performance of the HFT. The primary elements of the upgrade include improving the cooling to the detector and upgrading the readout electronics. The original SSD electronics were only intended to meet the performance specifications of the STAR TPC in the early 2000's. Now that the performance of the TPC, and its DAQ system has been raised to 1000 Hz, the SSD requires an upgrade to match these specifications.

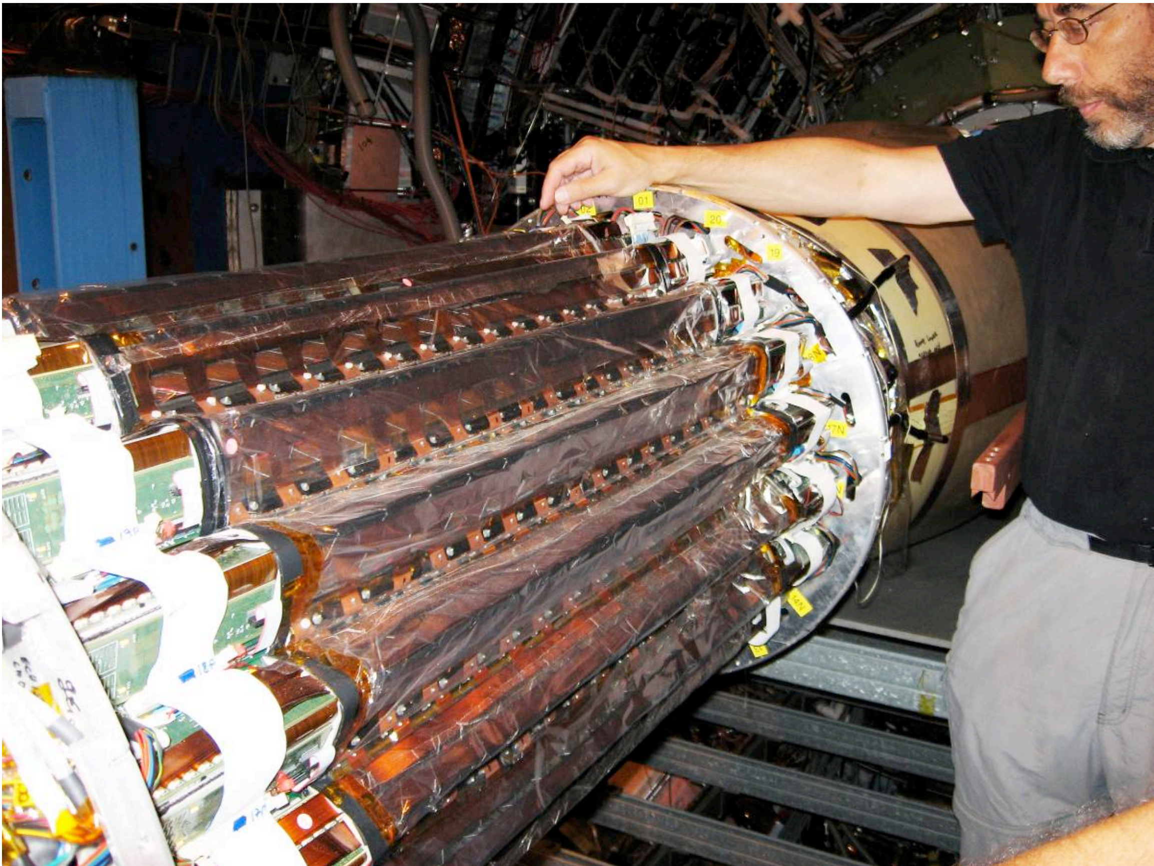


Figure 40: The photo shows the rollout of the Silicon Strip Detector for routine maintenance.

The SSD has the same ϕ and rapidity coverage as the TPC meaning that it offers full 2π azimuthal coverage and extends over a pseudo rapidity range of $|\eta| < 1.2$. Its radial location (Figure 41) puts it midway between the event vertex and the TPC. Thus it is ideally suited for the purpose of improving the TPC's pointing and momentum resolution, and extending the physics program of both detectors.

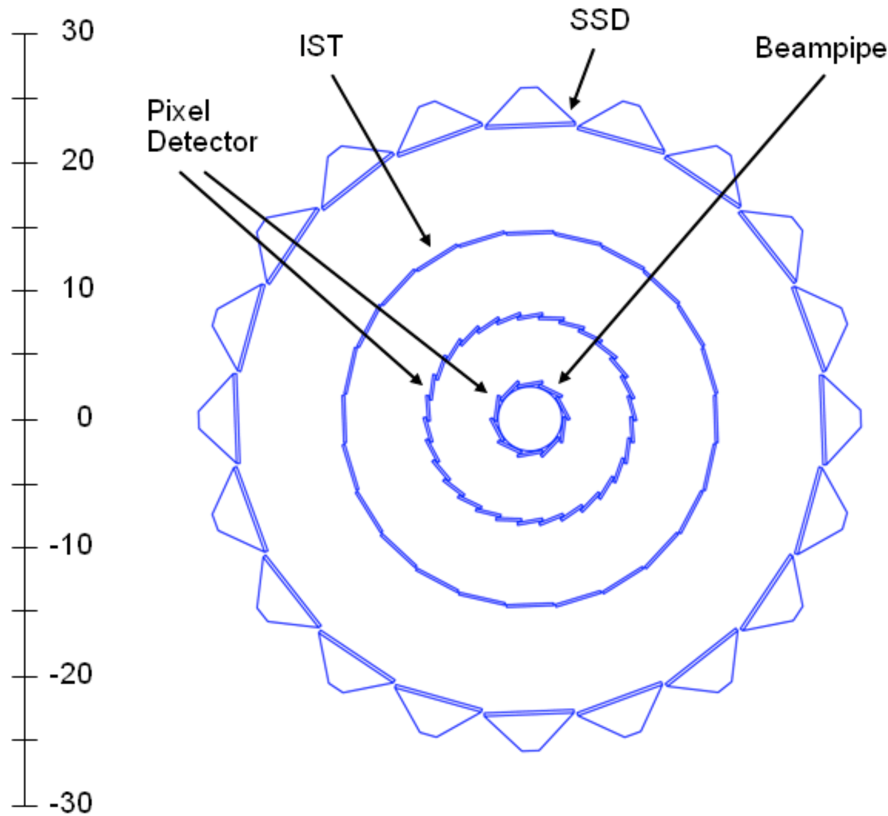


Figure 41: The SSD is shown surrounding the inner silicon tracking layers of the HFT.

The SSD is capable of locating a point on a track with a resolution of 30 μm in the r-ϕ direction and 850 μm in the Z direction[3,4]. This is a considerable improvement over the resolution of the TPC pointing at the SSD (which is greater than 1 mm in both directions) and so it enhances the overall pointing resolution of the combined system at the vertex. The excellent special resolution of the SSD is achieved by using double-sided Si with a layer of strips on each side of the same piece of Si. The strip layers cross and are inclined by 35 mrad with respect to each other and are placed symmetrically with respect to the edge of the wafer. Because of this unique double-sided feature, the SSD is a thin detector and is only ~1% radiation length thick. This ensures that the multiple Coulomb scattering is kept as low as possible for charge particle traversing the detector, but it also means the detector can be used to tag non-photonic electrons while generating a minimum amount of background due to photon conversions.

The SSD enhances the STAR physics program by improving:

- the reconstructable yield of the strange mesons and baryons, especially the K, Λ, Ξ, and Ω,
- the invariant mass resolution for resonances and spectra measurements
- the single-track high p_T resolution by approximately a factor of 2

In addition, the SSD is also an integral part of the proposed Heavy Flavor Tracker (HFT) and it will enhance the efficiency for doing the topological reconstruction of open charm and beauty decays with the HFT. The performance of the SSD is similar to, and nearly redundant with, the performance of the IST. However, this is the only redundancy in the

system and the redundancy is needed in order to ensure efficient track matching with the hits on the pixel layers in a high multiplicity environment.

3.4.1. How the SSD Affects the Performance of the TPC

The excellent special resolution of the SSD, and its ideal location, means that it is suitable to extend and improve STAR tracking from the TPC to the vertex. Figure 42 demonstrates the SSD improves the single track DCA resolution, at the vertex, from a few mm to less than 1 mm in the R-ϕ direction without using a vertex constraint.[5]

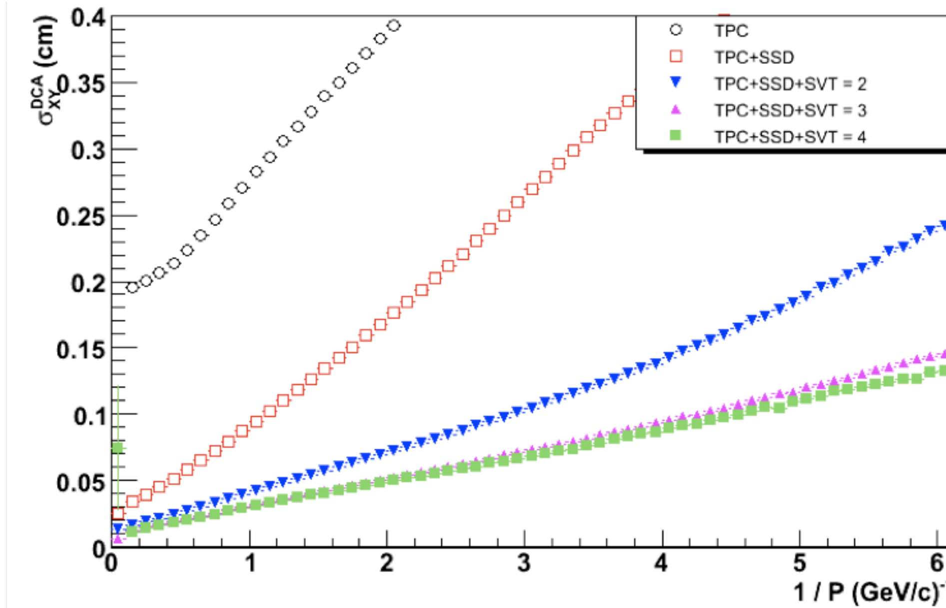


Figure 42: The DCA resolution of the TPC and the SSD versus the inverse momentum of the track. The top line shows the DCA resolution of the TPC, acting alone, for all tracks entering the TPC (i.e. no track cuts) during the high intensity Cu-Cu run at RHIC. The red line demonstrates how the pointing resolution of the TPC can be improved by including the SSD hits on tracks. The results are quoted for 200 GeV minBias Cu-Cu collisions with $|Z_{vertex} < 5$ cm$|$ and $|\eta| < 1$. The remaining lines on eh plot show the performance of the old STAR Silicon Vertex Tracker and are not relevant here.

The improved pointing resolution provided by the SSD will yield important improvements in the reconstructable yield of neutral and charged particles that decay within a few cm of the event vertex; in particular the strange mesons and baryons (K, Λ, Ξ, and Ω). Figure 43 shows a sample of K^0 mesons measured in the Cu-Cu beam with and without the use of the SSD. The improved signal to noise ratio (due to the improved background rejection) for the detection of baryons, mesons and resonances, will be important in our upcoming heavy ion runs and especially in the proposed low energy scan, where the integrated luminosity (and thus statistics to tape) will be limited.

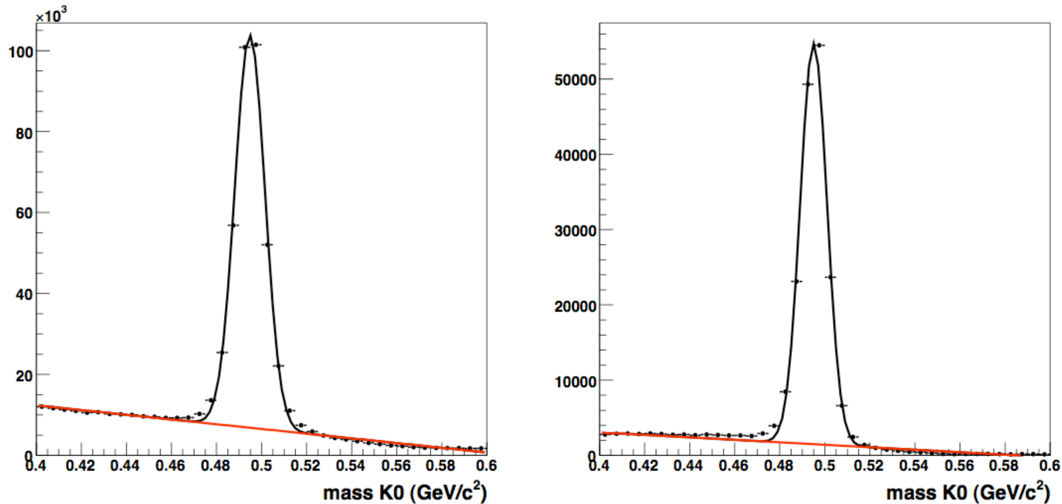


Figure 43: K^0 spectra for the high intensity Cu-Cu run at 200 GeV. The left panel shows the reconstructed K^0s using the TPC alone. The right hand panel the improvement in the signal to noise ratio when the SSD hits are included in the track fitting algorithm.

Figure 44 shows that the SSD improves the momentum resolution of the TPC by a factor of 2 at high p_T without the use of a vertex constraint. As a result, it improves the invariant mass resolution for resonances that decay into multiple charged particles (e.g. $\phi(1020)$, Λ). It is important to point out that the improvement in momentum resolution is achieved on a track-by-track basis and does not require a beamline or vertex constraint to achieve these results.

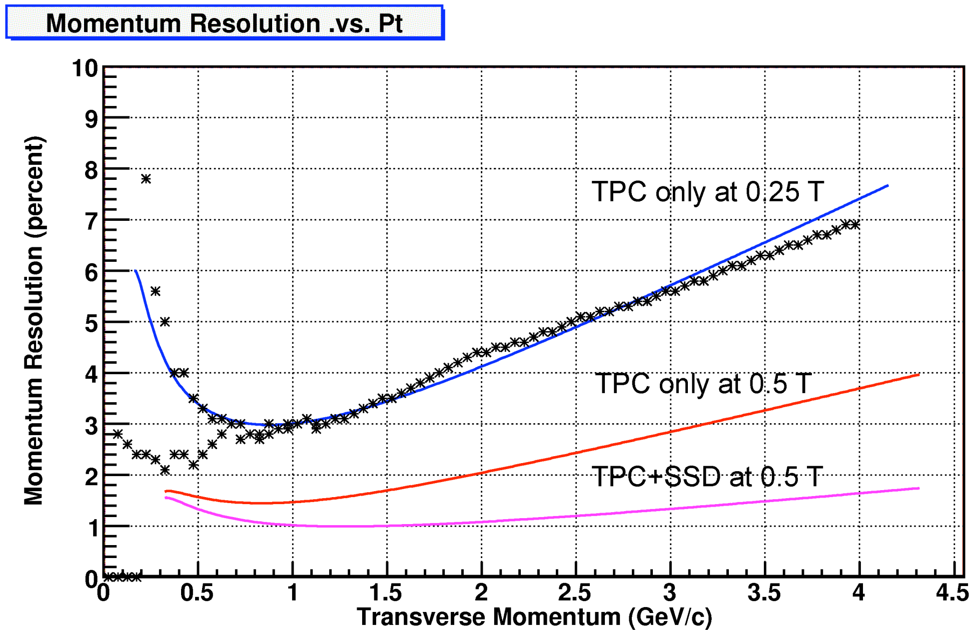


Figure 44: Data compared to simulated momentum resolution of the TPC and SSD detectors in STAR. The data points show a superposition of measured pion and antiproton spectra[6] at a magnetic field of 0.25 T. The blue line (top) is the simulated 0.25 T p_T spectrum for anti protons, while the red (middle) and pink (bottom) lines show the simulated momentum resolution for the TPC and TPC+SSD at 0.5 T, respectively.

The improved momentum resolution will be useful in our future studies of intermediate to high p_T hyperon production. For example (anti-)Λ production whose longitudinal spin transfer is sensitive to the helicity distribution function of strange quarks in the nucleon[7]. Figure 45 shows a Monte Carlo simulation of high p_T Λ spectra that can be observed in polarized p-p collisions at RHIC. There is a cut on the data to ensure that the Λ decays inside the SSD radius. The simulations[8] show that the width of the peak is improved substantially when the SSD is included in the tracking algorithm. It should be noted that an increasing fraction of Λ's decay at radii larger than the SSD radius as the p_T increases. (The two panels in the figure are different simulations and have a different number of events thrown in each simulation. The reader should focus on the width of the peaks as a measure of the improved quality of the tracking.)

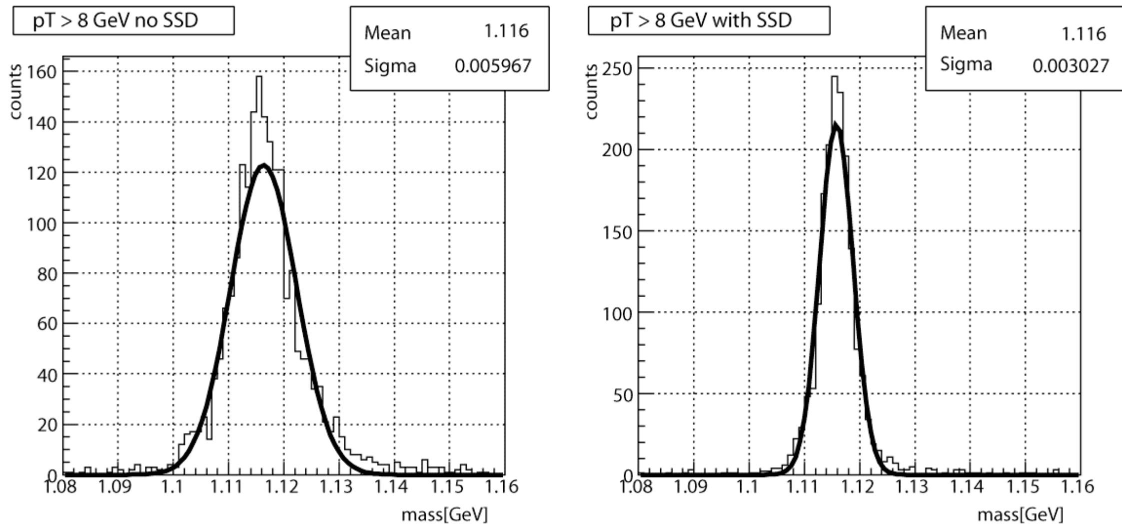


Figure 45: Simulated high p_T Λ spectra using the TPC alone (left panel) or the TPC+SSD (right panel) at 0.5 Tesla. The statistics boxes in each panel document the improved width of the peak when the SSD is included in the tracking algorithm.

The SSD is also a relatively fast detector and so it is only sensitive to tracks for 1.5 μs whereas the TPC is sensitive to tracks crossing its fiducial volume for 36 μs. This is important in p-p collisions where multiple events pile-up in the TPC and these piled up events must be distinguished on an event-by-event and vertex-by-vertex basis. The SSD can help to resolve the ambiguities due to multiple vertices because there is no appreciable pile-up in a fast Si detector, even for p-p collisions at 500 GeV.

Table 6 shows a self consistent simulation of the pointing resolution of the HFT detector sub-system at various points along the path of a kaon as it is tracked from the outside going in towards the event vertex.

Graded Resolution from the Outside - In		Resolution(σ)
TPC pointing at the SSD	(23 cm radius)	~ 1 mm
SSD pointing at IST	(14 cm radius)	~ 400 μm
IST pointing at PIXEL-2	(8 cm radius)	~ 400 μm
PIXEL-2 pointing at PIXEL-1	(2.5 cm radius)	~ 125 μm
PIXEL-1 pointing at the vertex		~ 40 μm

Table 6: A calculation of the pointing resolution of the TPC+SSD+IST+PIXEL detectors at intermediate points along the path of a 750 MeV kaon as it is tracked from the outside – in. Good resolution at the intermediate points is needed to resolve ambiguous hits on the next layer of the tracking system.

A more detailed look at the resolution of the HFT system is described in the HFT proposal[9] and an updated figure from that proposal is shown in Figure 46. The top panel shows the r-ϕ pointing resolution and the bottom panel shows the z pointing resolution at different places in the system. The beam pipe is included in the calculations. Due to the different geometry of the detectors, the r-ϕ and z resolutions are different in different places but, typically, the average pointing resolution improves for each of the layers at smaller radii.

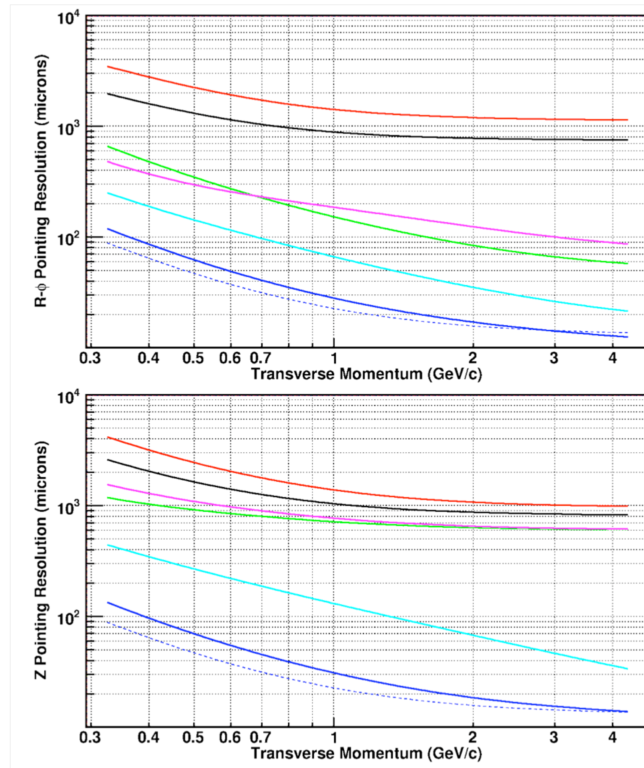


Figure 46: The simulated pointing resolution of the HFT detector system (σ); where the r-ϕ and z pointing resolutions are plotted separately (top and bottom, respectively). The calculations assume a kaon passing through the system. The red line shows the pointing resolution of the TPC onto the vertex. The black line shows the pointing resolution of the TPC onto the SSD. The TPC+SSD pointing at the IST is the green line. The TPC+SSD+IST pointing at PXL2 is magenta, TPC+SSD+IST+PXL2 pointing at PXL1 is cyan, and the full system pointing at the vertex is blue. The blue dashed line is the theoretical limit; it shows the idealized HFT performance without beam pipe or other sources of MCS except in the PXL layers.

The red line (top) in Figure 46 shows the simulated pointing resolution of the TPC (acting alone) at the vertex, while the black line shows the pointing resolution of the TPC onto the SSD. The pointing resolution onto the SSD is better than at the vertex because the SSD is closer to the TPC.

The remainder of Figure 46 is devoted to showing the pointing resolution of the system at each layer of the system. A detailed examination of the figure shows a pattern of improvement in resolution that reflects the detailed design of each detector. For example, the SSD detector has an asymmetric resolution of approximately 30 μm in the r-ϕ direction and 850 μm in the Z direction. The green line in the figures shows the resolution of the TPC+SSD pointing at IST. The r-ϕ and z resolution are also different for the proposed IST detector, as shown by the magenta line, but the figure returns to a simply ordered pattern with the addition of the PIXEL layers because these detectors are symmetric systems with 9 μm resolution in both directions.

The net effect of the increased pointing resolution that is delivered by the SSD is that it increases the efficiency for reconstructing a D^0 meson by at least factor of 2, and probably more when systematic errors are figured into the problem.

In addition, the SSD is also an important element in the alignment and calibration of the TPC because it has different systematic errors than the TPC (e.g. no distortions due to space charge or grid leak). It provides an independent measurement to assure that the TPC is operating at its expected resolution. Thus the theoretical efficiencies described above could not be achieved in practice without the extra benefit of the SSD as a calibration device.

3.4.2. Existing SSD Hardware – Before the Upgrade

The SSD barrel is composed of 20 individual ladders. The ladders are made of carbon fiber and each ladder supports 16 detector modules (see Figure 47). Each of these modules is composed of one double-sided silicon strip detector and two hybrid circuits equipped with analogue readout electronics. On both ends of a ladder, two electronics boards are used to control the detector modules and convert the analogue signal, which is sent to readout boards that are located on the TPC end-wheel.

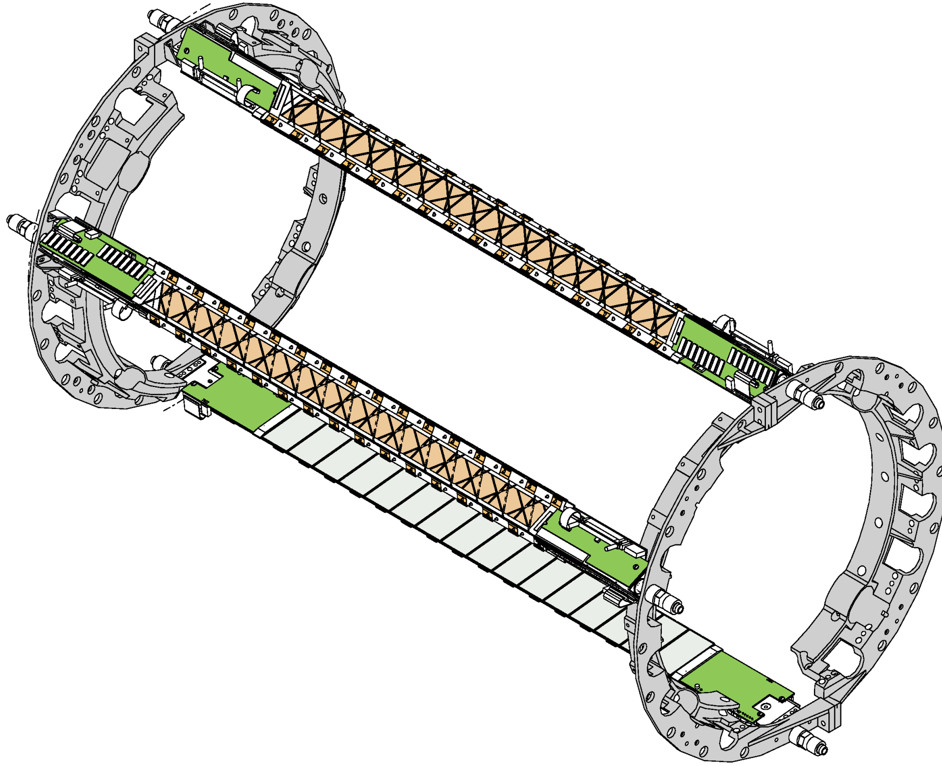


Figure 47: The end-rings for the SSD barrel are shown. The rings split into 4 sectors; the top and bottom sectors support 3 ladders each, while the sectors on each side support 7 ladders each. The complete detector has 20 ladders. In this figure, three ladders are mounted on the barrel at random locations.

One ladder is shown, in detail, in Figure 48. In the existing electronics, two cable busses (one per side of the Si wafers) transport the analog signals along the ladder to a pair of 10 bit ADC boards, which are located on each end. After digitization, the signals are sent to Readout Boards, which are linked to the DAQ system through Giga-link optical fibers.

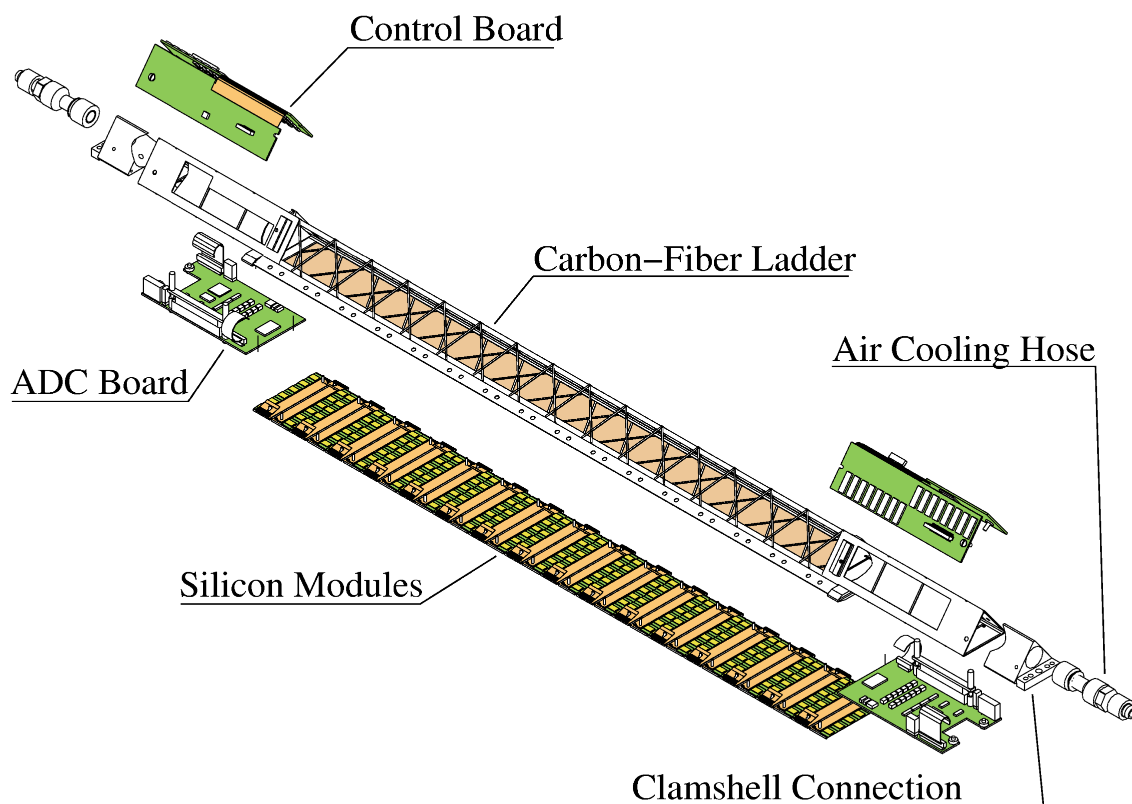


Figure 48: A SSD ladder showing its various components.

A detector module is the basic element of the SSD and it integrates a silicon wafer with its front-end electronics. One detector module is shown in Figure 49. Each module is composed of a silicon detector and two hybrid circuits. A silicon strip detector measures 42 mm by 75 mm and it is doubled sides with 768 strips on each side of the detector. The strips have a pitch of 95 mm, and are crossed with a 35mrad stereo angle between the strips on the P and N side of the silicon.

The two hybrid circuits are built on top of a flexible circuit made of Kapton and copper, which are, in turn, glued to a carbon fiber stiffener. The circuitry includes 6 analogue readout chips (the ALICE 128C), approximately 50 SMD components (resistors and capacitors) and 1 multi-purpose chip (COSTAR) dedicated to temperature measurements and low and high voltage monitoring.

The SSD is remotely controlled using JTAG for the power settings and temperature readings and also to calibrate and tune the front-end electronics. Each ladder dissipates about 20 W of power: 10 W from the Si wafers and 5 W from the electronics on each end of a ladder. The total heat dissipated by the system is 400 W.

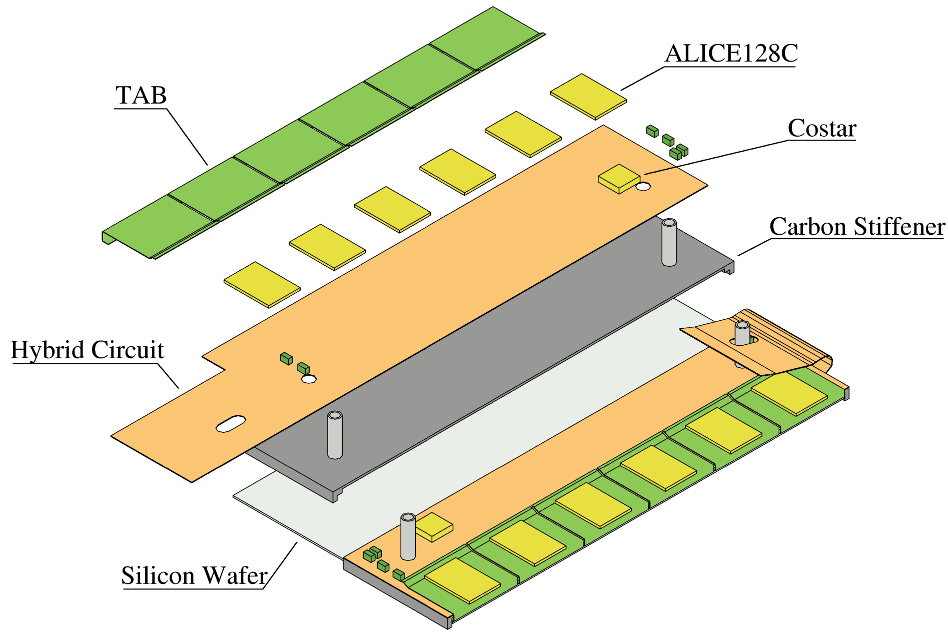


Figure 49: Exploded view of one detector module. It takes 16 modules to fill a ladder.

A schematic view of the electronics readout chain can be seen in Figure 50. The existing SSD electronics is capable of running at 200 Hz and this limit is determined by the availability of ADCs and readout boards. In the existing design, a group of ten ADC boards are daisy chained together to feed one readout board (RDO). Since each of the twenty ladders has two ADCs, a total of four RDO boards are needed to digitize the output of the full detector.

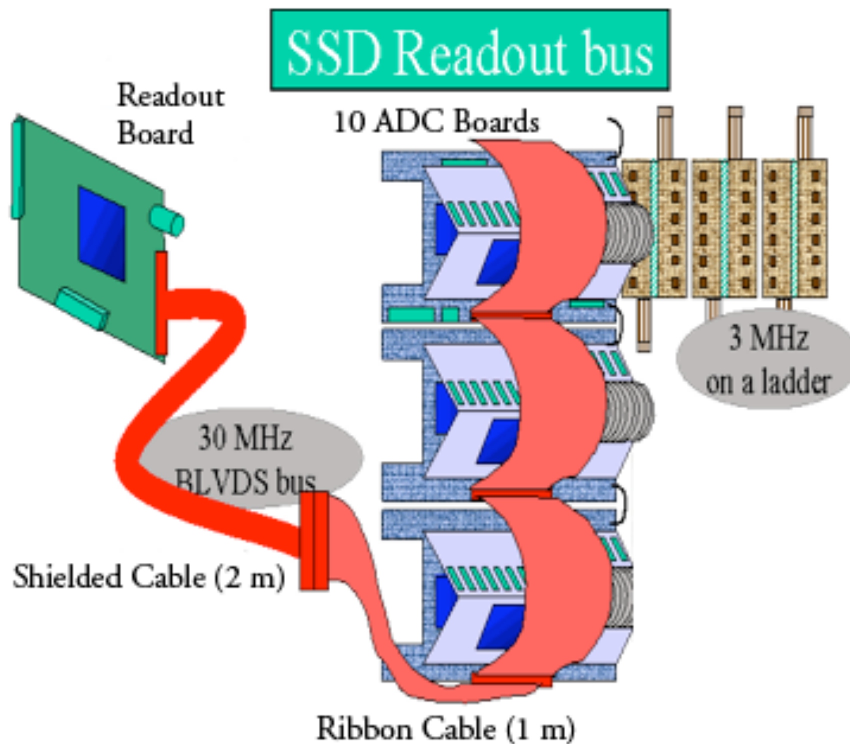


Figure 50: Module layout of the existing electronics (before upgrade).

The existing FEE electronics runs at a 3 MHz clock rate and, because there are 768 strips per wafer and 16 wafers to be read sequentially by a single ADC board, it takes 4.1 ms to read a ladder into the ADC Board. Each RDO runs at 30 MHz and controls ten ADC boards. Therefore it takes a similar time, 4.1 ms, to read out each RDO.

3.4.3. SSD Ladder Status

The SSD detector was used last during Run 7. At the beginning of the run, several ladders were known to be inoperable. Due to hardware issues, two ladders did not provide useful data and were turned off at the beginning of the run. Four other ladders were not stable when they were operated at the nominal HV configuration. They needed to be operated at a lower voltage and therefore were less efficient. During the run, it was determined that there was inadequate cooling to the ladders. Upon inspection after the run, several bent cooling hoses were found and are the probable cause of the ladder's overheating and instabilities. When the SSD is upgraded, the cooling system will be re-designed so that this problem cannot reoccur.

After Run 7, the SSD was removed and returned to Subatech Laboratory in Nantes. There the engineers tested each ladder and made a few repairs. Their final conclusion was that the SSD could be fully operational with an average of efficiency of at least 93%.

Among the 22 ladders (the 20 ladders that compose the SSD and 2 spare ladders), there are 6 perfect ladders; the others have flaws of various kinds. Eleven ladders have a few hybrid circuits that cannot be fully tested with the Subatech test bench. However the data acquired with these hybrid circuits may be completely usable. It was observed during the last data taking at STAR, that most of them produce good data. Nevertheless, due to some cooling failures and to reduce the heat load, a few of the hybrid circuits were turned off.

At this time, it is not possible to give a definitive status of these hybrid circuits. However, a software upgrade is planned to enable testing of these circuits. For a conservative estimate, we assume these hybrid circuits are bad. Using these assumptions, we obtain:

- 7 ladders with one hybrid circuit (out of 32 per ladder) not fully tested,
- 1 ladder with 2 hybrid circuits not fully tested,
- 2 ladders with 3 hybrid circuits not fully tested, and
- 1 ladder with 8 hybrid circuits not fully tested. (This was the first ladder produced so assembly techniques evolved during its assembly.)

In addition, a few inoperable hybrid circuits have been identified in five ladders. During data acquisition, these hybrids circuits had to be bypassed and thus did not provide data.

- One ladder had two partially damaged hybrids. One hybrid circuit had one chip (out of 6) dead. The other chip had 5 out of 6 chips damaged. This results in an effective inactive area of one hybrid.

- One ladder with 1 dead hybrid circuit and 2 not fully tested hybrid circuits. If the 2 not fully tested hybrids are considered as bad, this leads to an electronic coverage of 91% and for data use 81%. It is worthwhile to mention that the two hybrids could provide good data but have not been checked yet.
- Three ladders, known to have frequent HV trip during data taking, have been diagnosed to have some of the modules/hybrid circuits that cause a high leakage current. In that state, the culprit hybrid circuits are disconnected. This means we can use 1 ladder with 2 hybrid circuits off, another ladder can also be used with 4 hybrid circuits turned off, and the last ladder is operational with 2 modules turned off. In addition, some chips are missing (5 in total) and 1 hybrid circuit is not operational.

A repair of some of the ladders is under investigation. Figure 51 shows a thermal image (right) of the hybrid circuit with high leakage current. The leakage current has been identified to come from the hot spot that is at the location of a capacitor. It is possible to replace these capacitors and return the hybrid to a working state. This repair was performed successfully on a test ladder. Plans are underway to make this repair on the working ladders with HV trips.

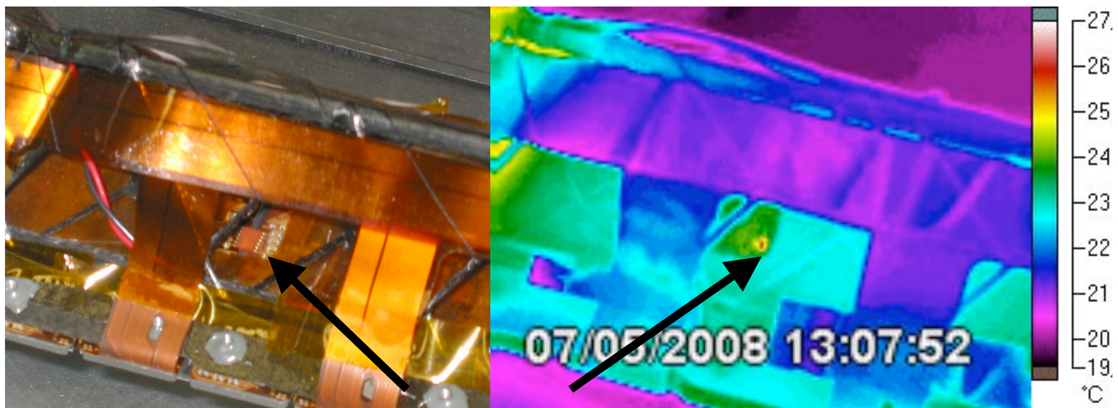


Figure 51: Left: photograph of the hybrid. Right: infrared image of the same hybrid. An arrow points to the capacitor on the left and another shows the hot spot on the right. As the hot spot is at the same position of the capacitor, we conclude that the capacitor is operating at a high current (several 100 μA) and is therefore leaking.

Figure 52 shows a summary of the current status of the best twenty ladders in detail. It assumes that the hybrid circuits that cannot be fully tested are bad. This figure shows the lower limit of the active coverage. The red marker represents the electronic coverage for each ladder. Since the SSD tracking software has been designed to use both the p and n side to determine a particle's position, one single side hybrid failure will result in the whole module being declared unusable. The blue triangle marker in Figure 52 shows the active area taking into account this effect. The average coverage is represented by the blue dotted line. If all the leaking capacitors are removed successfully, the overall coverage would reach 94%. This is represented with the blue solid line.

It is worthwhile to note that only one side of the module can detect a particle when the other hybrid of the module is not operational. This change would degrade the spatial

resolution, but it would increase the spatial coverage to 99%. Studies are needed to determine whether this change to STAR tracking is feasible.

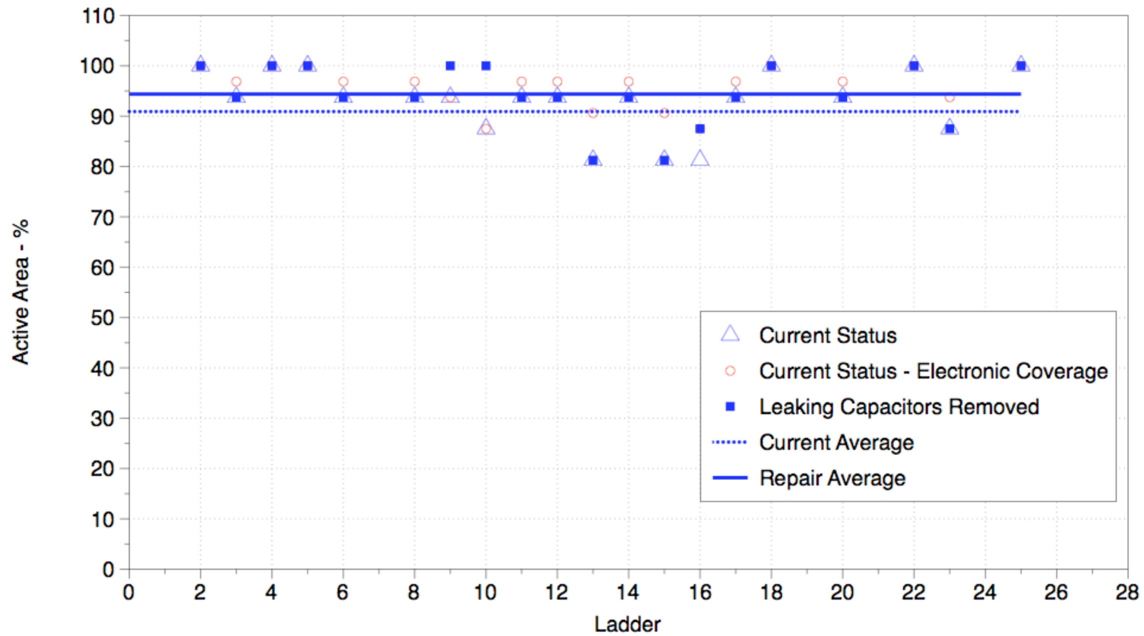


Figure 52: A plot of the percent active area of the SSD at the present and with the proposed removal of the leaking capacitors. The curves are explained in the text.

3.4.4. Plans for repair

In the previous sub-section, there are two kinds of defects in the ladder:

- A capacitor leaking, resulting in a high current of the ladder when biased with a high voltage (around 50 V).
- Several hybrid circuits not responding when programmed via the JTAG bus.

The leaking capacitor has to be removed using a special tool. A soldering head has been designed and fabricated for this purpose (Figure 53). It will be heated up to 250°C to melt the conductive glue, which was used to solder the components to the hybrid.

Figure 53: This soldering head will be used to remove the leaking capacitors on some ladders.

The JTAG chain is a kind of loop with which the data sent to the devices can be readout. During the initialization of the ladder, a test is done to check if the modules are correctly programmed. It consists in reading what was sent to the chips of the modules. If the data does not come back properly, it indicates that the JTAG chain is broken for such diverse items as bad chip, a broken strip, or a broken wire bond. If the chain is broken after the last chip of the module, the test fails, but the chips can be programmed correctly. This problem has happened several times during the construction of the SSD. To be able to cope with that, the software of the test bench at SUBATECH has to be modified. This software upgrade will be done in the near future.

3.4.5. Upgrade of the Electronics

The current speed of the SSD system is too slow to meet the DAQ1000 specifications, so it will be necessary to upgrade the SSD DAQ and RDO system to ensure that it is a viable detector in the future and a good partner for the HFT. The silicon wafers can be reused, but the readout electronics on each end of the ladders must be upgraded. In addition, the cooling system that has been in use for the SSD has proven to be inadequate, and has been removed. A new cooling system will be designed and installed.

Upgrade plans for the SSD electronics

The present SSD readout is limited to slightly more than 200 Hz trigger rate due to a number of factors. The ADCs, which digitize the signals from the modules, are limited in sampling rate, and each ADC is responsible for an entire ladder (16 × 768 samples). The fiber link to the DAQ receiver board is limited to 60 MHz × 20 bit = 1.2 Gb/s and the data are required to be formatted in a somewhat inefficient way in order to be compatible with the existing DAQ TPC receiver boards.

The upgrade addresses these issues as follows:

- A ladder will be digitized by 16 ADCs in parallel.
- TPC receiver cards are not used, removing the backward-compatible formatting constraint.
- The readout board (RDO) will perform zero suppression, reducing the data burden on the fiber link to DAQ.
- Multiple event buffers will exist on the RDO, reducing effective dead time due to the bandwidth limit of the DDL fiber link.

ADC and connection cards

The new electronics architecture reads the ladder modules in parallel. New ADCs, each reading a single module, sampling at 5 Msps, are read out in parallel and brought to the readout card via an optical fiber pair. Figure 54 shows the connection between the ADC boards and the RDOs.

Each readout card accepts the fiber link from five ladders. The readout card is connected to the DAQ SSD PC by a DDL fiber link (160 MB/s) identical to those in use in the TPX. Four readout cards reside in a 6U crate. A readout card is connected to the DAQ SSD PC

by a DDL fiber link (50 MHz × 32 bit = 1.6 Gb/s or 40 MHz × 32 bit = 1.28 Gb/s) identical to those in use in the TPX. Eight readout cards (four for each SSD side) reside in a 6U VME crate; there are, therefore, 8 fibers connecting the readout crates to the DAQ computer. The DDL links, together with their source interface to the SSD RDO (SIU board) and the PCI-X card residing in the SSD DAQ PC (D-RORC board), are readily available for purchase.

The redesigned connection card will deliver the payload from each module to one of the 16 inputs of the ADC card. The ADC card contains 8 Analog Devices AD7356 dual ADC chips. Each chip contains two independent ADCs with 5 MHz sampling rate and a bit-serial output. The serial output produces a 14-bit pulse train, of which only 10 bits are useful in this application. (The remaining bits will disappear in the RDO.) The outputs of the 16 ADCs are sent to the inputs of a parallel-serial converter, along with the slow control output of the FPGA. The parallel signals are clocked in to the serial converter at a 70MHz rate, resulting in a 1.4 Gbps pulse train, which is converted to optical and transmitted to one of the 5 inputs of the RDO board. The optical nature of this connection allows the RDO crate to be relocated outside the STAR magnet, since cable length is no longer a constraint. The cable cross section is also reduced from the twist-and-flat cables used previously.

The optical connection is bidirectional; the second fiber runs at a reduced clock rate since its purpose is to provide slow control information to the FPGA on the ADC card, which manages the analog circuitry on the ladder.

Heat Load

The ADC chips selected for the ladders consume very little power (14 mA @ 2.5 V). Taking into account the remaining components: FPGA, serializer, deserializer, and optical transmitter and receiver, each ladder's end electronics is expected to consume less than 2W. The existing ADC and Connection boards dissipate approximately 5 W per ladder end, with an additional 10W dissipated by the Si modules, hybrid, and costar chip. So the estimated dissipation for a full ladder of new electronics is expected to be 14 W compared with 20 W for the existing system. However, we will not be able to confirm these numbers until we actually build prototype boards and test them.

RDO card

At the RDO card, the 1.0 Gbps bit train is converted by a deserializer to a 20-bit wide data path, which is updated at a 50 MHz rate. Sixteen of the 20 bits produced by the deserializer are delivered to a second bank of 16 1:14 deserializers, resulting in 16 10-bit wide replicas of the original ADC values produced on the ADC card. (The remaining bits are used for the slow control function.) This second bank of deserializers is contained in an array of 5 FPGAs, each one dedicated to the data delivered by the fiber from a single ADC card. These FE-FPGAs perform zero suppression and multi-event buffering on the 16 data streams produced in the last bank of deserializers.

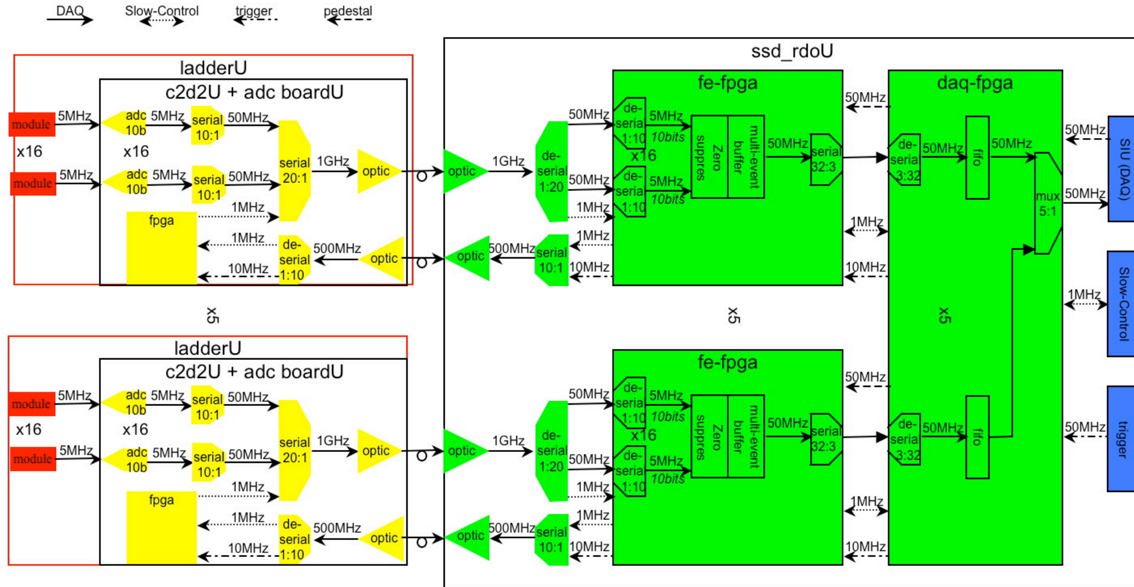


Figure 54: A schematic of the interconnection between the ladder electronics and the RDO card, Each RDO handles 5 ladders. The connection between the ladder electronics and the corresponding RDO card is a dual optical fiber.

The multi-event buffers and zero suppression both provide a means to reduce dead time due to data burden on the DDL optical fiber. Zero suppression provides the additional benefit that it relieves the SSD DAQ PC of the chore of having to find the above-pedestal strips. Delivering the unsuppressed data to the PC can result in a heavy computing and memory-access load on the PC, which may limit the number of DDL fibers which it can host, since the ADC value for each strip has to be extracted from the word in which it has been stored along with 2 other ADC values, pedestal subtracted, and possibly written back to memory. These steps become unnecessary if the data are zero suppressed at the RDO. When done in the FPGA on the RDO, zero suppression can be accomplished in real time.

Zero suppression is carried out in the simplest possible way: the ADC value for each strip is compared with a stored pedestal value corresponding to that strip. If the ADC value exceeds the pedestal, the strip number and ADC value are encoded into a 32-bit word and entered into the multi-event buffer.

The multi-event buffers are provided as a second means of reducing dead time. Simulation has shown that for randomly spaced triggers 4 buffers can keep the dead time to about 7 per cent for a trigger rate of 1 kHz. We expect about 3% of the strips to be hit in a central Au-Au event. If the SSD modules are sufficiently free from hot strips, the zero suppression technique is to be preferred. However, when there are enough hot strips in a module, the event size can become excessive, and the multi-buffering provides a fallback technique.

There is sufficient on-chip RAM storage in the FE-FPGAs to implement buffers for 4 events that have not been zero-suppressed. In zero-suppressed mode, these buffers can be coalesced into a single event buffer large enough to handle largest zero-suppressed event. It is expected that the operator will monitor ladder occupancy. When a ladder is

observed to be producing large zero-suppressed events, the offending module will be masked off.

The ladders are read out by passing a token to the chain of 6 ALICE128 analog multiplexers handling the analog signals corresponding to the 768 strips of a single module. Once this process has started, it must continue until the token reappears, at the end of 768 clock cycles. In the event of an abort arrival, the clock speed will be doubled in order to minimize the time consumed by this process.

Readout Crate Location

The use of optical links between the ladder and readout crates makes the location of the readout crates non-critical. For that reason, it is expected that the crates will be located on the South platform, where space is available.

DAQ resources needed

The 8 SSD readout cards require 8 DDL fiber links to DAQ PCs. Each DDL receiver card (DRORC) handles two fibers; thus, 4 DRORC cards are required to provide the necessary interface. This is best implemented in 2 PCs, each with 2 DRORCs. Each PC will be responsible for one-half of the SSD.

Slow control interface

The existing slow control system is based on software running on a VME-based Power PC running VxWorks. The CPU is obsolete and the VxWorks system is becoming more difficult to maintain.

In the upgraded system the slow control information to and from the ladders travels over the optical fibers to the readout cards The SSD Slow-Control interface consist of two independent JTAG chains: the Slow-Control chain and the FPGA configuration chain. The previous Slow-Control system was connected to the old RDO boards by four cables (2 for each side of the SSD). To minimize the changes in the Slow-Control system software, we will have 2 RDO boards connected to each Slow-Control cable. The transport on optical fiber between RDO and ADC boards is completely transparent to all the components that have to decode and answer to the JTAG orders.

The top-level slow controls software generates the GUI and interprets user commands. The change in architecture necessitates a complete revision of this software, no matter which path the information follows, due to the change in organization of the intra-ladder components.

Trigger interface

Each of the 8 readout cards has its interface to the SSD trigger TCD. The interface will reflect the updated definition of the TCD (still in progress), if this definition is finalized in time. The functionality of the trigger interface remains unchanged from the present system except that it will use both the 10 MHz and the 50 MHz clocks instead of creating the 50 MHz onboard.

3.4.6. Cooling System – Requirements, Status and Upgrade

The evacuation of heat produced by the electronics in the SSD is critical in order to establish stable behavior with the sensors and the associated electronics.

The SSD is an assembly of 20 carbon fiber ladders. Each ladder is equipped with 16 double-sided silicon micro-strips detectors (320 modules in the whole) and each strip is connected to its own charge amplifier channel. This means nearly 4000 "A128C" integrated circuits. These latter are made of 128-channels charge amplifiers with low noise and low power consumption. At each ladder end, there are 2 electronic boards (one "ADC Board" and one "Connection Board") used for analogue to digital conversion of the signal and for wire connections to send signals to the data acquisition system.

Power consumption

The power consumption of the different components of the SSD layer can be separated into two independent parts: The first part is due to the Front End Electronics (Alice 128C) chips, and the second part to the ADC and Connection Boards. Table 7 shows an initial estimate, and the final measurement, of the power used by the FEE.

FEE POWER	Number of elements	Predicted Power	**Measured Power**
Alice 128	12 per module	44 mW	
COSTAR	2 per module	44 mW	
Detection Module	16 per ladder	616 mW	
TOTAL FEE		**9.8 W**	**10W**

Table 7: Estimated and measured power used by the FEE in the existing SSD electronics.

Table 8 presents estimates for the new electronics and results of measurements for the existing electronics for power consumption of the ADC and of the Connection Boards.

Electronics Boards	**Number of elements**	**Predicted power (old)**	**Predicted power (new)**	**Measured power (old)**
ADC Board	2/Ladder	2.0 W/card	1.0 W/card	
Connection Board	2/Ladder	3.0 W/card	1.0 W/card	
Total from Boards		**10 W**	**4 W**	**10 W**

Table 8: Estimated and measured power for the ADC and Connection Boards.

Table 9 summarizes the power consumed by the FEE electronics and the electronics boards on both ends of each ladder.

	Old	**New**
Total FEE	10 W	10 W
Total Electronic Boards	10 W	4 W
Total per ladder	**20 W**	**14 W**

Table 9: Estimated power consumption for a ladder

Given the low power dissipation per unit area in the detection surface (~20 mW/cm^2), a cooling system using air was developed and designed for the SSD. For the two ends of a ladder (ADC + Control Boards) the problem is different: the density of released energy per unit area is 4 times bigger than for the FEE. Fortunately, this zone is not in direct view of the silicon modules.

The air path in the ladders

Each ladder is cooled by air circulating throughout the carbon fiber structure and, in effect, the ladder functions as an air pipe. So each ladder is wrapped in a thin Mylar film to guide the air. The electronic boards are installed on the ladder ends with the components pointing inwards and 'seeing' the inside of the triangular section. Deflectors inserted inside the ladder help guide the air to the warmest components.

The flow of air is driven by an external vacuum system so that air is pulled through the ladders and the heated air is removed from the central part of the STAR detector. The input air comes from IFC, which contains the free volume between the SSD and the TPC. The warm air is then evacuated to the outside of STAR through a flexible hose of approximately 10-mm diameter.

The 10 mm diameter flexible hoses were the probable cause of the cooling failures seen in Runs 6 and 7. After re-installing two ladders of the SSD during the shutdown following Run 5, the SSD was re-inserted into STAR. However, sufficient care was not taken with the hoses during installation and several of them were bent out of shape and kinked. The kinked hoses interrupted the airflow to perhaps 10 of the 20 ladders and probably affected all of the ladders to one degree or another. The exact analysis is hard to determine because the kinked hoses are hidden from view during the operation of the detector, however we had problems with the cooling system in both of the following runs.

We found direct evidence (see Figure 55) in several cases that this was problem during the disassembly of the SSD in the shutdown period following Run 7. We believe that hard plumbing the cooling lines to the SSD ladders and replacing the vacuum system with a more reliable and simpler system can overcome these problems.

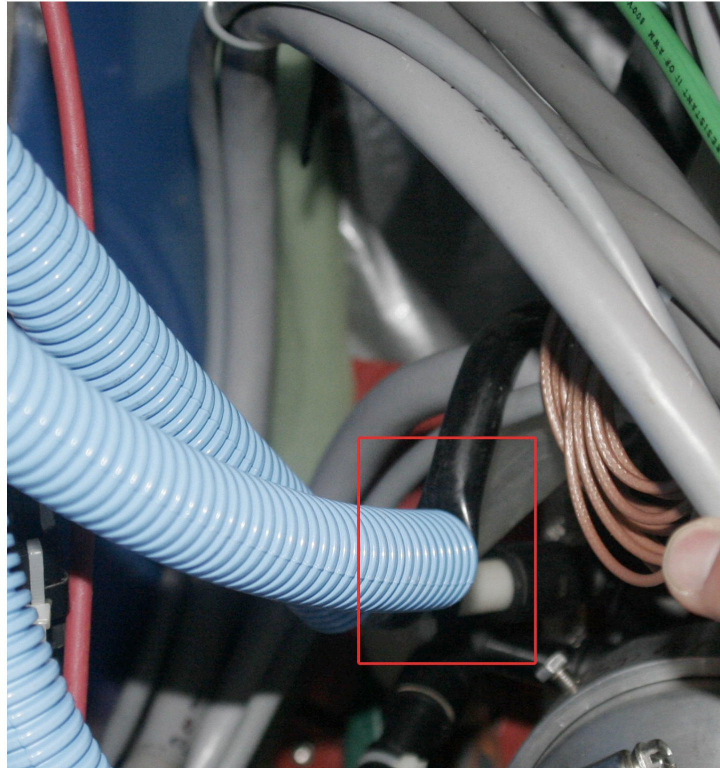


Figure 55: The red box highlights a kinked cooling hose that was discovered during the removal and disassembly of the SSD in August 2007. Ideally, the blue corrugated hose should have protected the black vacuum line … but did not in this case. The existing hoses will be replaced with larger and stiffer hoses or alternatively several lines can be replaced with a hard-covered plenum.

Requirements and Functionality Tests

The Si detectors and the ADC boards will become unstable when they get too hot. For example, during RHIC Runs 6 and 7, the SSD ladders routinely shutdown when they reached a temperature between 45°C and 50°C. The exact temperature that the modules shutdown depended on the location and ladder number, but the primary reason for the shutdown was that the noise on the chip increased as it got hotter. As the noise went up, the HV had to be raised to get a bigger signal. Increasing the HV caused higher leakage currents and eventually the leakage current went above the limit of the HV power supply and the system tripped off. So experience has shown that the SSD electronics should be maintained at 35°C to 40°C; pushing above 40°C is very dangerous.

The SSD design team at Nantes has done a series of thermal tests on a ladder to see how it will perform under various conditions. Table 10 shows the temperature inside the ladder at a few critical points when the cooling system is off. The maximum temperature measured was 46.5°C. These tests were done at an ambient temperature of 19°C whereas the average temperature inside the IFC of the TPC during Runs 6 and 7 was 24°C. Thus, you would expect a global shift of 5°C in the actual STAR Environment.

	SIDE P (°C)	SIDE N (°C)
ADC	42.8	46.5
Control Board FPGA	34.8	36.5
Connection Board	45.2	45.4

Table 10: Mean electronics temperatures measured on the test ladders with cooling off. The ambient air temperature was 19°C.

Therefore, we believe that the chip failures that were observed in Runs 6 and 7 are fully consistent with a cooling system that was not working because the environment for the SSD inside STAR allowed the chips to float up to the critical 45°C to 50°C region.

On a happier note, the cooling system performs quite well when it is turned on and the flow of air is not impeded. Table 11 show the temperature distribution at the critical points with the cooling 'on'. Once again, it is worth noting that these temperatures were recorded using input air at 19°C. In the actual STAR environment, the input air is drawn from the IFC and the air in this region typically has a temperature of 24°C. It would be highly desirable to lower the IFC air temperature to 20°C to 22°C in order to provide a small safety margin for the SSD and the other silicon detectors.

	SIDE P (°C)	SIDE N (°C)
ADC	33.1	33.2
Control Board FPGA	33.7	30.7
Connection Board	27.6	24.5

Table 11: Mean electronics temperatures measured on the test ladder with cooling on. The ambient air temperature and input air temperature was 19°C.

Additional temperature measurements were performed at various points along the ladder and these results are shown in Table 12. Between modules 8 and 11 (in the middle of the ladder), the temperature goes above 37°C even when the cooling system is on.

Module	Si Temperature (°C)	COSTAR Temperature (°C)
3P	27.8	35.3
5P	32.9	32.5
8P	30.9	37
11P	30.2	37.5
14P	28.7	34.9
16P	25.1	32.3

Table 12: Mean Temperatures measured at various points along the test ladder with the cooling system turned on. The column on the left identifies the wafer number (1-16).

Temperature as a function of time is shown in Figure 56. The input air was 19°C, the air speed along the ladder was ~0.5 m/s, the airflow was 1 liter/s, and the pressure drop across the ladder (assuming no input impedance) was 12 mbar. The air temperature at the output end was 29°C.

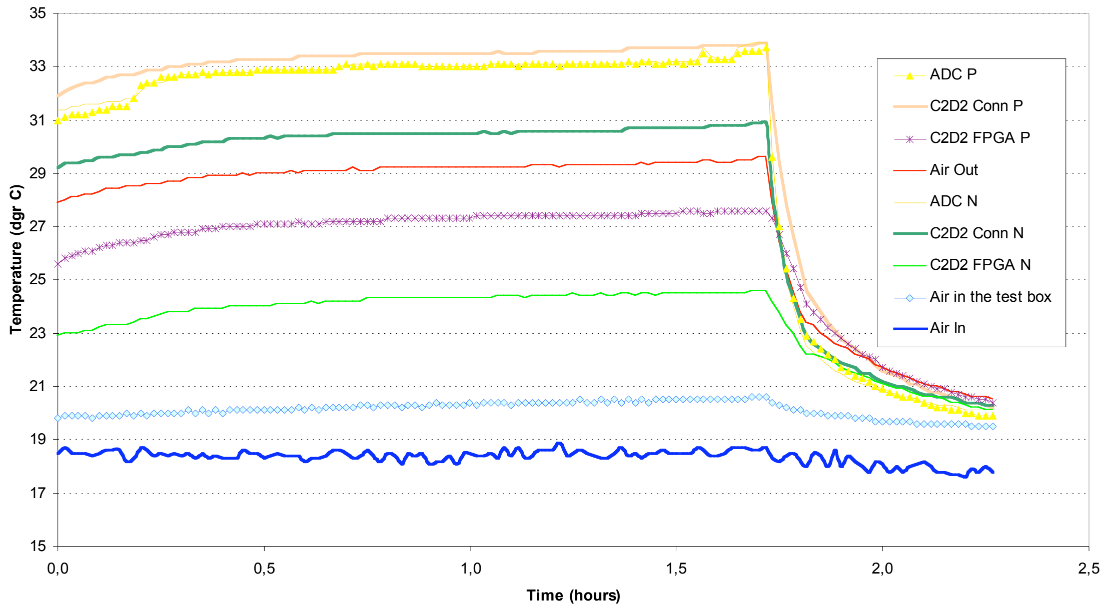


Figure 56: Example of ADC and Control Board temperature evolution during 2 hours of running. The electrical power was switched off after 1.8 hour while the cooling remained on. The input air was held at a constant 19°C while the output air averaged 29 °C.

Cooling System Summary and Upgrade Plans

A vacuum driven cooling system can maintain the temperature on the SSD ladders to between 32°C and 37°C if the input air temperature is kept below 20°C. The silicon detector temperatures are held below 31°C under these conditions and the wafer leakage currents are reasonable. The leakage currents increase with the wafer temperature but this has a minor impact in terms of electronic noise if we stay out of the danger zone above 40 °C.

However, these tests were made with the incoming air held at 19°C while in STAR the IFC air temperature is around 24°C. This means that we should expect a global temperature shift of the same order for these tests results and this is consistent with our observations in Runs 6 and 7. It is highly desirable to lower the IFC temperature to 20°C to 22°C in order to provide a large margin of safety for the Si detectors.

As was already mentioned, the air hoses from the vacuum source to the SSD need to be upgraded so that they are robust and reliable under all conditions. We will engineer a new system that uses hard-covered hoses or alternatively a hard covered plenum to deliver the air to the SSD.

The source of vacuum also needs an upgrade because the existing Vortex system is complex, prone to failure, and expensive. It consumes 76 kW of power.

A cheaper and more reliable system is available. The wood working industry needs high volume vacuum sources to clear wood chips from around saws and lathes. Thus, there is a commercial line of vacuum supplies that provide vacuum with the flow and pressures

that we need. These vacuum supplies can be purchased, off the shelf, and run on 120 VAC or 240 VAC. Typical examples are shown in Figure 57 and Table 13.

Figure 57: A typical vacuum system from *Dust Collection and Vacuum Systems, Inc.*

Specifications	RP-212-EL	RP-426-QL	RP-546-QL
Input Voltage	230 VAC 1	230/460 VAC 3	230/460 VAC 3
Power Consumption	1.2 kW	2.6 kW	4.6 kW
Maximum Airflow	100 CFM	150 CFM	225 CFM
Max Static Pressure	110 in. H_20	105 in. H_20	130 in. H_20
Tank Capacity	15 Gal	12 Gal	30 Gal

Table 13: A typical vacuum system from *Dust Collection and Vacuum Systems, Inc.*

A three-phase system is highly desirable because a 3-phase motor does not require brushes and so is capable of continuous operation over a very long period of time. We will mount the vacuum system on the North Platform (dirty power side) and provide vacuum to the SSD via non-conducting plastic pipes. The precise details on how to route the pipe, and divide the airflow so that it reaches each ladder are still to be determined.

3.4.7. Alignment Mounts on the Cone

The SSD is attached to the existing cone by four mechanical pieces at each end of the barrel (Figure 58 and Figure 59). Those parts allow a geometrical adjustment to position the SSD concentrically with the IST and PIXEL. These pieces are equipped with screws (Figure 60) to adjust the SSD. The new cone will be designed to use these existing fixtures.

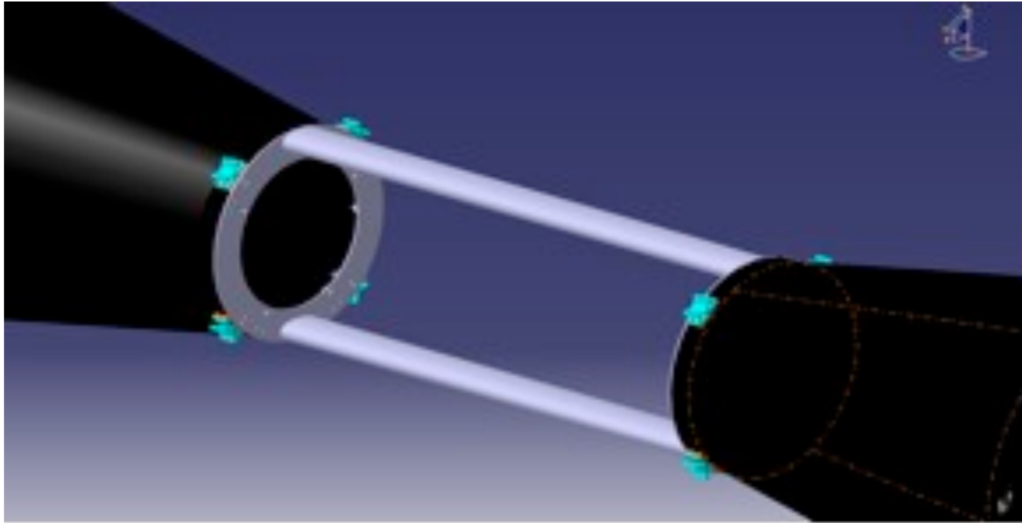


Figure 58: Detail of central area of cone with attachment and geometrical tuning parts of the SSD. This picture shows the design of the existing STAR cone.

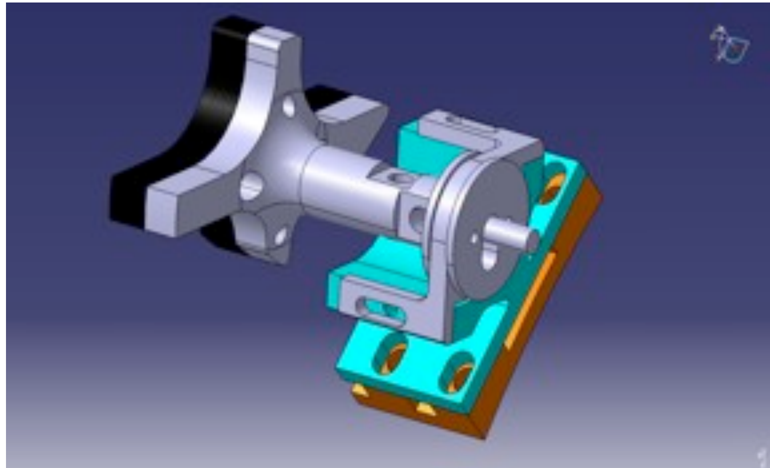


Figure 59: Detail of the interface between SSD and cone (the orange part is glued to the cone).

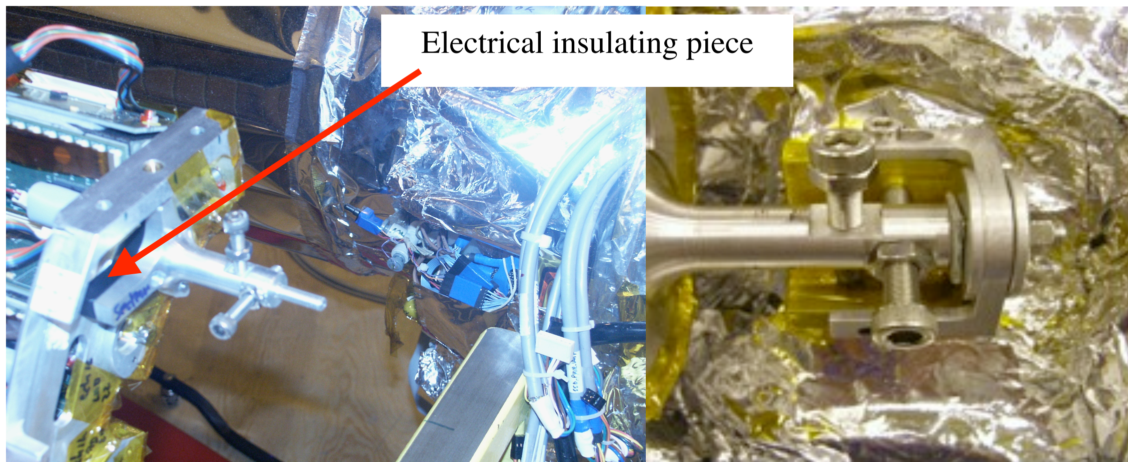


Figure 60: The left panel shows the SSD mount before it is mounted on the cone. The right panel shows the SSD mount after it is attached to the cone. The black electrical insulator that isolates the SSD from the rest of the system is shown under the tip of the arrow.

3.4.8. Cable paths

Figure 61 shows the cable paths from the SSD to the DAQ Room. We plan to use the existing power cables except on the cone where the path length is expected to be longer. There needs to be breakout on the end of each side of the cone so that detector can be moved inside the Assembly Hall without removing the connections to the ladders. Sufficient space must be allocated on the cone ends for the breakout boxes.

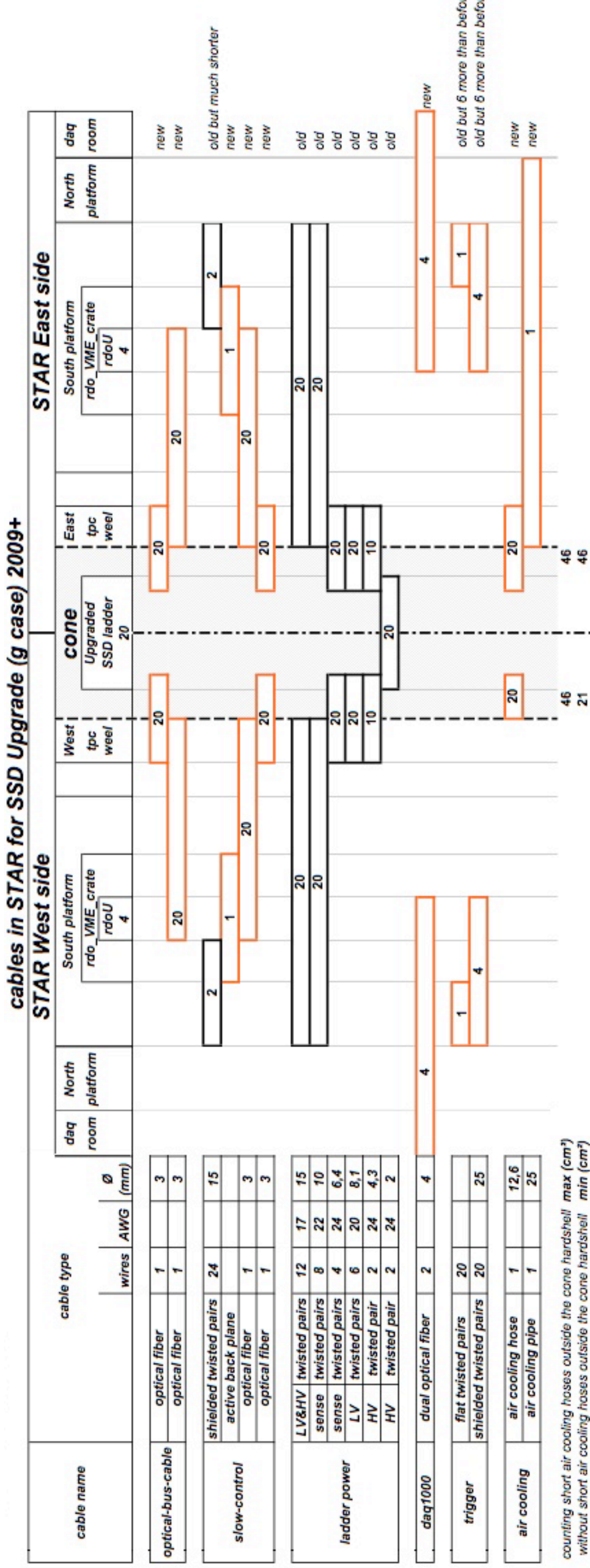


Figure 61: Cabling paths for the SSD.

3.4.9. Cable Paths on the Cone

While there is space available for the cables on the STAR platform and the path to the DAQ room, there is limited area on the STAR cone. The FGT will be installed on the West cone and there are only limited access ports for passing cables. Therefore, we make a preliminary estimate of the space needed. This calculation uses the existing power cables and size for the cooling tubes and adds in the expected cable bundle from DAQ and Slow Control.

The SSD is readout separately on each side of STAR. Each ladder is a separate detector. Therefore there will be 20 cables of each type on both the East and West Cone. As each ladder requires only one HV bias cable, alternate ladders are fed from both the east and west side. An estimate of the size of the cables is given in Table 14. The power cables are the same size as the original design.

System	Cable Type	#	Diameter mm	Area Rectangular cm^2	Total Area Rectangular cm^2
DAQ and Slow Control	Optical Fiber (dual)	20	3.0	0.1	1.8
Ladder power	Sense (4x AWG 24)	20	6.4	0.4	8.1
	LV (6x AWG 18)	20	8.1	0.7	13.2
	HV Bias (2x AWG 24)	10	4.3	0.2	1.9
Air Cooling	Air cooling to end of cone	20	12.7	1.6	32.3
Contingency		0.15			8.6
				Total cm^2	65.8

Table 14: SSD Cable parameters. The area for the cable size is calculated assuming it is square.

In the current design of the SSD mount, the space for cable removal was around 10 cm. As that design had cables and air tubes spread all around the cone, it was relatively easy to work on the detector. This feature must be achieved in the new design. Now that the FGT wants to be situated as close as possible to the center of the interaction region, careful attention must be paid to the cone design so that there is adequate space for the installation and removal of the SSD cables and cooling tubes when the FGT is installed. Sufficient space on the cone must be allocated for these cables.

3.4.10. Rack space

The SSD currently occupies one rack on the South Platform. This rack contains a VME crate, two CAEN power supply crates, and two distributions boxes for the HV and power

cables. This space will be maintained for the present CAEN supply or a replacement. The power supplies provides, +2 V, -2 V, and +5 V to the ladder.

The use of optical links between the ladder and readout crates makes the location of the readout crates non-critical. For that reason, it is expected that the crates will be located on the South platform, where space is available. Therefore sufficient space will be needed for this item.

It will be necessary for the STAR Slow Control system to communicate with the RDO board. Thus an interface will be necessary. At this time a design has not been made. Therefore, we will need space in either the existing SSD slow control VME crate or a nearby one if a different VxWorks operating system is needed.

3.4.11. Staging Plan

There are three stages in the construction of the SSD. In FY09, we will build a prototype. We will build one test setup with several modules. Then we will readout a full ladder. The ladder will them be shipped to BNL and tested in the DAQ Room with the full STAR Trigger. To accomplish this, we will need to have a complete STAR system (DAQ1000, trigger and slow control) at SUBATECH. With the decommissioning of the old STAR TPC DAQ system, there are spare VME crates and processors. With an addition of building a cable, which has been already been designed by the STAR TOF upgrade group, we will have the hardware to create a trigger that can generate arbitrary command sequences. What is most important is that we have Slow Controls involved during this stage.

In FY10 we will build one test section (3 ladders), check it, and then ship it to STAR to be used as part of inside of STAR in a Physics run. After the run, the section will be shipped back to SUBATECH, where the final electronics will be built and installed. In FY11, the full detector will be sent back to BNL and will be installed in STAR.

3.4.12. Resources

Summary

Subatech will handle the upgraded electronics design up to the schematic level. At BNL, the schematics will be used to generate board layouts for the various components, and the boards will be fabricated and assembled under BNL responsibility. This will require an engineer and technician for 3 months.

Subatech will provide a prototype of all firmware for programmable parts. All upgrades and revisions will then become the responsibility of BNL.

The design and implementation of the cooling system will be the responsibility of a BNL mechanical engineer.

Resources needed in Nantes

The upgrade to the SSD readout requires the participation of Christophe Renard (SUBATECH electronic engineer), Stéphane Bouvier (SUBATECH project engineer), Gerard Guilloux (SUBATECH mechanical engineer), and Louis-Marie Rigalleau (SUBATECH electronics technician). Most of the design for the upgrade to the readout system will be carried out at SUBATECH, with participation during the production phase by a BNL engineer, who will continue to maintain the system after it is installed.

Resources needed from BNL

For the readout upgrade, a digital electronics engineer will be required at BNL to participate in the design, layout, and debugging of the upgraded electronics. It is essential that this person takes ownership of the new electronics, learn to diagnose problems, and repair the affected boards. (5/8 FTE integrated over the time of this project.) In addition, an electronic technician (BNL) will be required to lay out the new boards and be responsible for their fabrication. Following completion of the upgrade, a continuing engineering effort (0.1 FTE) will be required. It is assumed that this will be contributed by BNL.

Cooling system replacement

The cooling system needs to be designed and implemented. A BNL mechanical designer is required for this effort. Estimated cost for the cooling system: $12K, in FY09, plus the engineering cost and associated travel ($5K). The new system must be ready for installation in the summer of 2010.

Slow controls upgrade

Slow Controls needs to be redesigned and implemented using a Linux PC as a platform. Implementation of the Slow Controls upgraded software will be done on PCs, with Ethernet linking the various nodes in the system. This hardware will cost $15K and travel for the SC person to Nantes for integration will cost $5K. A partial implementation must be ready for integration at Nantes in mid 2009. The final system must be deployed in summer of 2009.

Shipping and travel to/from Nantes

Shipping of the detector ladders from Nantes for the detailed test and installation is included.

Replace CAEN HV/LV power supplies

The existing power supplies caused some down time in Run 7. There are no spare crates for quick swaps, and the manufacturer no longer offers them for sale. We propose to replace them with more modern models, at a cost of $20K. This change will require a modification of the Slow Controls. To minimize this effort, we plan on selecting a model

that uses an Ethernet interface. We are also exploring the possibility of obtaining these supplies from a decommissioned detector.

Contingency

The cost of the readout upgrade is dominated by manpower and related costs. Hardware represents a small piece of the total. Contingency for the custom hardware is calculated at 30%. Additional travel for U.S. personnel should be planned for, as well. We estimate the travel contingency at three additional foreign trips.

Cost offsets due to BNL contributions

The US engineering effort is expected to be contributed by BNL and will effectively reduce the costs in the table (shown below) by approximately $400K. See below.

Cost offsets due to SUBATECH contributions

All engineering and technical effort to be provided by SUBATECH is assumed to be contributed labor and will not be charged to the project. Due to the differences in the US and French accounting systems, these costs are not included in the table, below. We assume that the Subatech numbers include contingency.

3.4.13. Cost Summary

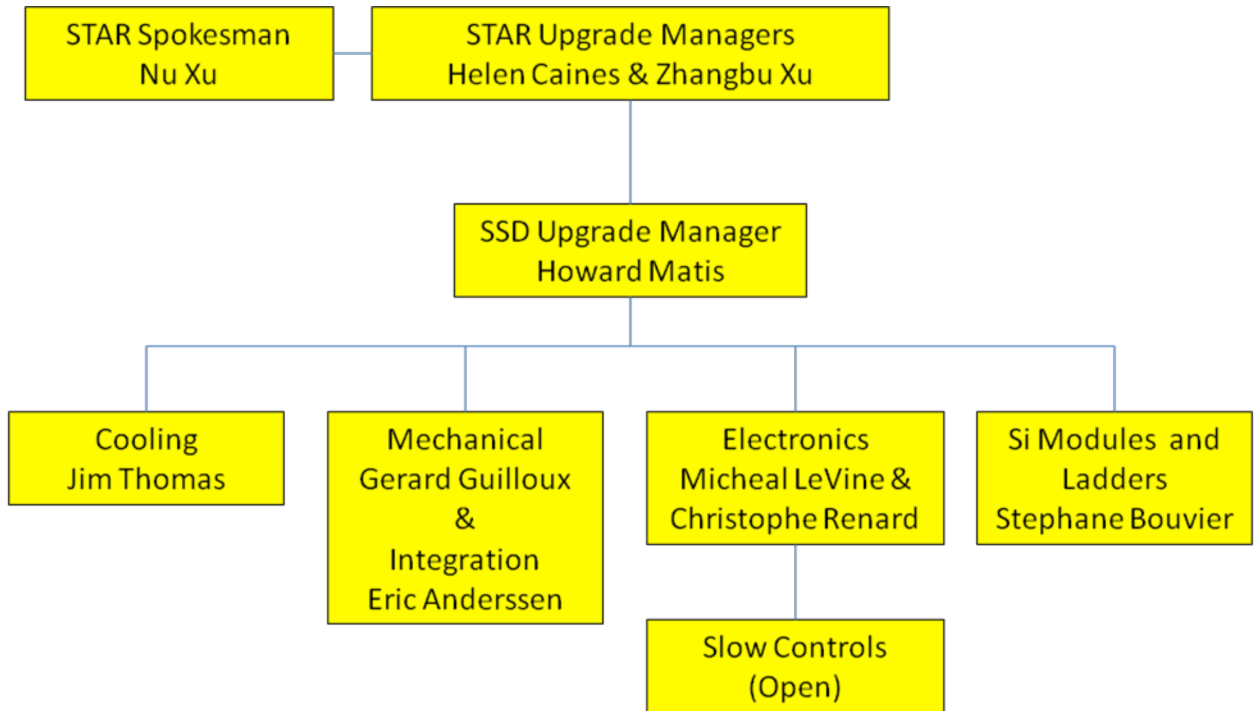
FY09		**Hard Expenses ($K)**	**Salary ($K)**
Slow controls integration with new electronics	STAR	5	0
FPGA development tools/evaluation boards	STAR	6	0
Upgrade coordination meeting	STAR	5	0
Hardware–partial readout implementation	STAR	34.9	0
¼ FTE BNL electronics engineer	BNL	0	70
¼ FTE BNL electronics technician	BNL	0	45
Slow controls hardware	STAR	15	0
Hardware–bench test prototype readout system	STAR	3.4	0
Replace power supplies	STAR	20	0
New cooling system hardware	STAR	12	0
Cooling system engineering	BNL	0	52.5
Travel	STAR	21	0
Shipping electronics to Nantes	STAR	1	0
Shipping detector to BNL	STAR	3	0
Upgrade installation & test	STAR	8.6	0

SSD connection to STAR & test	STAR	2.9	0
Burden (50%)		*68.9*	
Contingency (30%)		*62.0*	*50.3*
Total FY09		**$268.7 K**	**$217.8 K**

FY10		**Hard Expenses (K$)**	**Salary ($K)**
Hardware–full readout implementation	STAR	103.9	0
¼ FTE BNL electronics engineer	BNL	0	70
¼ FTE BNL electronics technician	BNL	0	45
Travel	STAR	30.4	0
Burden (50%)		*67.2*	
Contingency (30%)		*60.6*	*34.5*
Escalation (3%)		*7.9*	*4.5*
Total FY10		**$270.0 K**	**$154.0 K**

FY11		**Hard Expenses ($K)**	**Salary ($K)**
1/8 FTE BNL electronics engineer	BNL	0	35.0
Travel	STAR	15	0
Burden (50%)		*7.5*	
Contingency (30%)		*6.75*	*10.5*
Escalation (6%)		*1.75*	*2.73*
Total FY11		**$31.0 K**	**$48.2 K**

3.4.14. Management Structure



3.5. Integration into STAR

3.5.1. Cone and Support Structure

Overview

West-East Cone

ICS

OCS

Assembly procedure

Assembly area requirements

3.5.2. Beam Pipe

Mechanical

Bakeout Considerations

Support

3.5.3. Services

Summary of Air, Water and Power

Space requirements on Magnet and Platform

3.5.4. Controls

3.5.5. Data Acquisition

3.5.6. SSD

3.6. Software

This section contains the description of the software elements required for the successful processing and analysis of the acquired raw HFT data. Since the HFT is an upgrade detector of the STAR experiment, its software needs modules to be incorporated into the existing software and computing environment of the experiment. After a brief discussion of STAR's software environment, we list and describe the online, offline and simulation modules and tools that are required to be developed for the HFT. We will finish with a discussion of resources and institutional software responsibilities and commitments.

3.6.1. STAR's Software Environment

The STAR software environment comprises of a set of tools (development, simulation, production and analysis environment), mainly in the form of plug-in software modules in a ROOT – based backbone interface. At the same time it provides the data model and the coding standards and the data model for new module development and integration in the top-level shell scripts. Each detector sub-system is responsible for the development of all modules necessary for its successful operation. New, major pieces of code need to be reviewed and approved before insertion in the main repository. This work is coordinated with the rest of the experiment through a designated software representative from the group. At the same time there is a software infrastructure group based at Brookhaven National Lab (aka BNL-core), that maintains and manages critical pieces of code (tracking, calibrations, databases) and also provides help with the integration of new software in the system.

Online Environment

The online software primarily ensures the data integrity during data acquisition via appropriate detector monitoring and sample event reconstruction. Beyond these basic but important tasks, and as computer processing capabilities improve dramatically, more and more formerly offline tasks move to the online environment. One such task is the hit finding in the STAR TPC. Discussion has started on the possibility for online (pre-) tracking in the TPC. This is of particular interest to this group since we plan for on chip Pixel clustering and hit finding for the Pixel detector.

Offline Environment

The offline environment consists of the event reconstruction software packages. This starts with the raw data as input and through proper calibrations it proceeds with detector cluster/hit finding, integrated tracking, event vertex finding and event information writing on DSTs.

3.6.2. Online Software

The online software serves as a tool to monitor detector performance. It is also used to perform online calibrations where possible. Online software is detector specific and is described in Section 3.2 for the Pixel, in Section 3.3 for the IST, and in Section 3.4 for the SSD.

3.6.3. Offline Software

Hit Reconstruction

The Cluster/Hit finder is the first piece of code applied to the pedestal subtracted raw information from the IST and PIXEL detectors.

In the IST detector this will be a standard search for all fired strip-lets, i.e. all strips with a pedestal subtracted ADC value above a cut/threshold value (typically a value two to three times the strip noise-RMS level. Groups of adjacent strips that are fired will be clustered and further analyzed by a peak finding program for one or more possible hits. Every such 'hit' is then first going to be assigned a set of local/wafer coordinates based on the strip's position on the wafer. This will be followed by a local-to-global transformation to STAR global coordinate system (detector hit information needs to be saved in global coordinates), which is usually done via a series of partial transformations (wafer to ladder, ladder to shell, shell to detector, detector to STAR). This is common practice in silicon strip detectors and the MIT group, which will build the detector, has extensive experience in this area.

In the PIXEL detector the first steps (Cluster/Hit finding) are incorporated on the chip's logic, i.e. done online during data acquisition, as discussed in Section 4.2. The local to global transformation process is identical to the IST even though the partial transformations will be different in order to incorporate the specific geometry and the specific hardware-implemented alignment features of the PIXEL detector (see discussion on Alignment below and in Section 4.2).

Tracking

The current STAR reconstruction environment provides a Kalman-filter based integrated tracker. This tool is in principle ready to accommodate and integrate the IST and PIXEL hits, with their proper error/weights, in its environment. In reality work and close collaboration with the BNL-core group will be required to tune the tracker's parameters and optimize its performance. For example it has to properly handle the high precision information coming from the PIXEL layers. Also, there is a need to develop methods to deal with the path ambiguities in the SSD and IST (effective strip 'hits' with relatively large errors in the long strip direction), as well as dealing with the ghosting in the PIXEL detector due to out of time events in a high luminosity environment. Dealing with the latter two problems of tracking/ghosting will require studies that use a several-passes tracking approach and/or knowledge of the triggered event vertex obtained from a first-

pass (or quick) vertex finder. This is a critical item which will finally determine the physics performance of the system and therefore needs special attention and effort.

Event Vertex Reconstruction

Currently STAR deploys two different event vertex finders during event reconstruction, one for heavy ion and one for proton-proton collisions. Each of them is specifically tuned to perform best in these completely different environments (high multiplicity w/out pile up in heavy ions and low multiplicity with high pile-up in p-p). In a typical heavy ion collision the TPC has to cope with events of relatively large multiplicity and virtually pile-up free whereas in p-p one needs to extract the primary vertex from a few primary tracks surrounded by a thousand of out of time (pile-up) tracks. As a direct consequence of this fact STAR uses a Minuit-based event vertex fitter (with a seed finder) in heavy ion collisions. For p-p the vertex fitting procedure is based on a chi-square minimization method but, most importantly, the information from fast detectors is used to select (tag) the tracks that belong to the triggered event. Only these tagged tracks participate in the event vertex-fitting step.

In the RHIC-II era's increased luminosity there is going to be pile-up in the TPC but most importantly in the two PIXEL layers of HFT due to the relatively large integration time of the detector (see Section 4.2 and also *Pileup* discussion below). This will be the case in both p-p and heavy ion collisions. The SSD and IST are assumed to be pile-up free even for the highest rate p-p collisions. The presence of these two (as well as the other) fast detectors will require a new, revised version of the vertex finder that will combine the best features of both current finders. At this point we do not anticipate the need for any new functionality, just the need for tuning and QA-ing the new/combined finder.

We should note here that the mid-term plans of the reconstruction/infrastructure group include the deployment of a Kalman filter-type vertex finder, which at the same time will do the primary track fitting. In high multiplicity events (>30 tracks or so) one can perform without loss the vertex finding/fitting and primary track fitting (i.e. fitting global tracks with the vertex as an extra point on track for tracks with DCA within a cut value, e.g. currently 3cm, from the vertex. This will be revised in the HFT era due to much higher precision in pointing.) in two separate steps. In low multiplicities it is generally better if one performs a simultaneous fit of primary tracks and event vertex. This is worth exploring. Let us remember that the larger fraction of the secondary/decay vertices we are trying to resolve are in the range of 10-100 microns and any improvement in determining the event vertex (the most important single reference point in the event) is indispensable.

Secondary/Decay Vertex Reconstruction

The reconstruction of short-lived particles in a collider environment is an extremely challenging task. The key measurements of HFT involve the reconstruction of D- and B-mesons with typical $c\tau$ in the range of 120 – 500 microns, and Λ_C with a $c\tau$ of 60 microns. The lack of a Lorentz boost typically results in mean decay distances of about half the $c\tau$, for decays at midrapidity of a properly p_T weighted sample. For example, the anticipated mean p_T for D_0 mesons in Au+Au collisions at RHIC is about 1 GeV/c. This is a conservative estimate taking into account expected high p_T suppression effects. The

$\beta\gamma$ factor for a midrapidity D_0 is 0.54 and thus its mean decay distance ($c\tau$ of 120 microns) is about 65 microns. For a 1 GeV/c Λ_C baryon this will be about 30 microns. This environment demands the highest level of sophistication in the methods used to reconstruct the decay/secondary vertices.

Up to now, the STAR secondary vertex reconstruction code had to deal with decay vertices of strange particles, typically in the few centimeters range. For those distances, simple geometrical reconstruction models coupled to crude, fixed value cuts were sufficient. Only a recent effort to reconstruct D-mesons with the SVT, the first generation silicon vertex detector in STAR, started deploying decay vertex fitting techniques using the full error information of a track, on a track-by-track and vertex-by-vertex basis (sometimes also called μ-Vertexing). Cuts like the decay length are not fixed values but rather a number of standard deviations of the fitted value. This way the cuts are less biased especially the one, like DCA, which have strong momentum dependencies. This work, currently still under development, will be the basis of the modules deployed on the HFT data. These important software modules are to be developed, as they are a key piece of the new software.

Databases – Calibration and Alignment

The accurate monitoring and recording of the state and the position of the detector inside the STAR apparatus is of outmost importance as it directly impacts its performance. Calibration is the online and offline task of monitoring the state of the detector. The online part (often referred to a slow controls) gathers information of the detector in-situ, usually during running periods. Such information might be temperature or position of elements, pedestal files etc. This information is stored in a Database with a timestamp. The slow controls for the SSD, IST and PIXEL detectors are discussed in Sections 4.4, 4.3 and 4.2 respectively. The offline part of the calibration includes also software methods used to check e.g. the position of the detector elements using tracking information. The results of these procedures are stored as updated values in specific bank in the Database and are used in the massive offline physics production reconstruction passes.

The task of Alignment is a very demanding one especially for the PIXEL detector where one would like to perform/know the positioning of the detector elements with offsets and tolerances to within a few microns.

The alignment of the SSD and IST is not a challenging task provided good survey data has been collected of the detector's elements beforehand. The in-situ alignment will be done with software techniques (global and/or local alignment) and there is previous experience on this in the collaboration. All it is required is to bring the SSD (IST) hits within the TPC (TPC+SSD) track projection errors to the detector layer, typically around 100 microns or so. Global alignment techniques usually yield results accurate to about 10 microns using a set of only a few hundred thousand tracks. Rotations are also typically kept to a fraction of milli-radian.

In the PIXEL detector this task is more difficult and the designers of the detector decided early on to incorporate 'hardware' techniques in order to minimize element displacement in-situ. The pixels are designed with a 20 microns 'envelope' error, i.e. maximum

allowed displacement in-situ. To achieve this various sophisticated methods have been developed, e.g. interlocking, easily replaceable pre-surveyed shells with extreme precision on-bench survey data. Details on the method and the specific hardware implementation can be found in Section 4.2.

Despite this excellent 'hardware pre-alignment', software methods will have to be deployed in order to both check and fine-tune the in-situ information of the detector elements. There are two categories of software alignment techniques, the so-called Global and Local alignment.

The *Global* alignment uses TPC (+SSD+IST) track information on a statistical basis in order to obtain systematic silicon detector rotations and shifts. Typically a 'rigid body' model is applied (i.e. ignoring possible ladder twists, sagging effects and wafer non-planarity) and a misalignment model is introduced. Then a Taylor expansion with respect to misalignment parameters (3-D shifts and 3-D rotations) is performed looking for deviations of measured hit position from predicted primary track position on a measurement (wafer) plane. The track prediction comes from the detector(s) used as reference, e.g.\ initially the TPC alone, and later the combined TPC+SSD (+IST) tracking. In the next step, from the hit deviations distribution, a misalignment parameter has been calculated as a slope with a straight line fit. A global least-squares fit is also simultaneously performed on all available information. The method is applied iteratively until the fitted parameters reach stability. This global method was first applied to TPC+SSD+SVT data in STAR and it is well developed and understood. It will serve us in the IST alignment but it will need modifications for the PIXEL detector. This is because the Pixel elements (wafers) on a ladder will have deviations from the 'flat plane' hypothesis.

In a *Local* or *Self*-alignment method one aims at the most precise *relative* placement of the detector elements. In this procedure only high precision hit information is used coming exclusively from the detector under local alignment. A successful method using the event vertex constraint was developed and tested on simulations by the BNL-core group and this should be further developed into a working module with data for the HFT complex.

3.6.4. Simulation Framework

The current simulation framework in STAR is based on GEANT-3.0 with custom script extensions to facilitate detector geometry implementation and event generation. It also includes event generators like HIJING, PYTHIA, Phase-space etc. that are interfaced to GEANT. This framework is soon to be abandoned and will be replaced by a ROOT-based geometry and tracking package (VMC, Virtual Monte Carlo). Nevertheless, we are still using it and we will continue to do so in the immediate future. The tasks, and therefore software modules one needs to develop here are: a) the **detector geometry** definition, b) the **detector response** packages (fast and slow simulators), c) track **embedding** in real/raw events, d) a hit **pileup** handler, e) the Association Maker and structures for **evaluation** purposes, and f) Physics **analysis** code (performance, physics etc) capable of handling and evaluating the resulting information. Our group will have to

contribute modules and effort in all these categories. It is worth mentioning here that besides this full and detailed simulation chain the group has developed very useful tools for quick estimates of various detector configurations, resolutions, layouts etc. These tools, sometimes referred to as 'hand calculations' or 'fast Monte Carlo' will keep playing an important role when either a quick turn around is needed or for cross checking purposes.

Detector Geometry Definition

This task is to include in the GEANT-simulated apparatus of the experiment the latest and most accurate/realistic geometry of HFT (IST and PIXEL), since this is the only way to ensure reliability of the resulting efficiency numbers. This task also includes the definition of the active areas of the detector, the hit information and the global positioning matrices of the detector. It has been recently realized that for certain studies (e.g. layer optimization studies, overall tracking efficiencies, 'quick' feasibility studies etc), a simplified version of the geometry could be very useful, a version where average material thickness is included but without detailed outline of the discreet components (cables, ICs, ladder support etc).

Detector Response Simulators

The detector response simulation packages in STAR reside outside the Geant framework. They are actually invoked at the event reconstruction step. Typically there are two or three categories of response simulators: a) *Fast simulators*, which smear the hit position coordinates and assign hit uncertainties based on parameterized analytical functions. The fast simulators run extremely fast and are good for quick studies that do not need detailed implementation of the detector. They are also relatively easy to imlement; we already have an HFT fast simulator in place for all syb-systems, b) *Slow simulators,* which simulates hits at the ADC level (usually obtained from sampling parameterized response functions. A slow simulator is a must when accurate acceptance and efficiency numbers are requested in physics analysis. A slow simulator is also used in embedding as discussed below, and c) *Very Slow simulators*, which track individual electrons through the detector body; from their generation to the readout. This is usually very time consuming and one utilizes this method only in small-scale productions in order to determine or verify the functions used in the first two methods.

A Slow Simulator for the IST detector

The technology similarities between the SSD and IST (both silicon strip detectors with similar Si wafer thicknesses but with SSD being a double-side, crossed strip detector and IST single-side, shorter strip detector) could be beneficial in developing a slow simulator for the IST. The currently under development SSD code could be modified and adapted for the IST needs.

A Slow Simulator for the PIXEL detector

The detailed simulation for STAR Heavy Flavor Track PIXEL silicon detector consists of 4 steps. First, use the information of a charged particle passing through the PIXEL as inputs. The information contains the particle momentum, incident direction, path length in the PIXEL, and the sum of electron-hole pairs it generates. The total number of electrons generated from charged track passing through the silicon sensor is calculated using Bichsel distribution[10]. Second, build the geometry of the detector: one chip of 640 x 640 PIXEL array. One PIXEL is 30um x 50um x 30um, consist of four different layers from top to bottom: Readout electronics layer, diode layer, epitaxial layer and substrate layer. Third, simulate the transportation of electrons generated in the PIXEL[11]: diffusion, recombination and reflection at interfaces between different layers. A Gaussian equation is used to describe the diffusion as a random walk process. The electron recombination rate is dependent on the different doping density of different layers. Finally, calculate the distribution of electrons collected in the PIXEL array as output signal. The left panel of Figure 62 presents the simulated pixel cluster shape from 1GeV charged pion incident at 45-degree angle. The right panel of the figure shows the comparison of the deposited number of electron profile from data [11] and simulation. The two results agree with each other very well. The major problem for this slow simulator is the speed. It takes about 20 minutes to simulate a single charged track and it comes mainly from simulating the electron diffusion process. This is too slow to be used in future large-scale simulation studies.

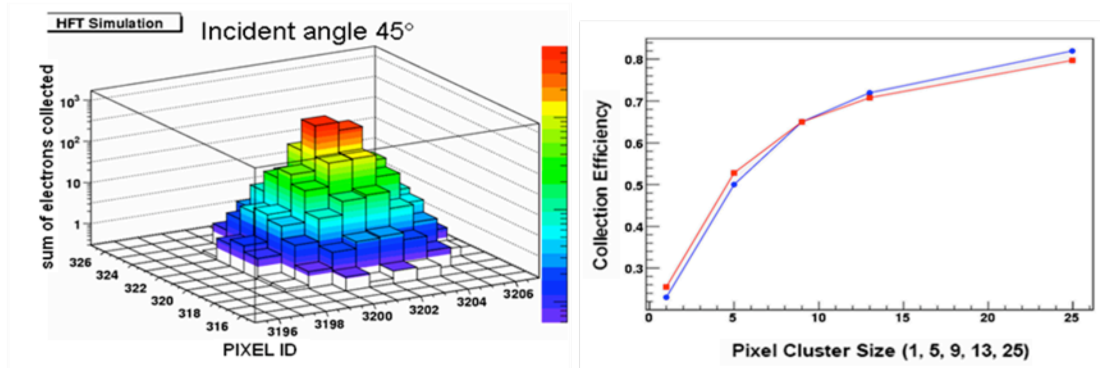


Figure 62: (Left) distribution of number of deposited electrons on pixels from a single charged pion with 45 degree incident angle from the slow simulator; (right) profile of the fraction of deposited number of electrons from simulation (blue) and data [11] (red).

To significantly improve the speed while keeping good accuracy, we developed a simplified method. Instead of simulating diffusion process step by step for each single electron, we calculate the probability distribution function for each electron in a specific space location to be collected by different pixels. Since any electron generated in the PIXEL is independent from each other, by randomly sampling this probability distribution function, we can decide which pixel collected this electron or if the electron recombined before being collected. Following above steps, we collect the pixel IDs that absorb all electrons along a charged track and add them up to obtain the number of electrons deposited in each pixel. To implement this method, we built a fine 3-D grid in a single pixel and calculated the probability distribution function for electron produced

from all grid points using the slow simulator. For any one electron from incident charged track, we directly use the probability distribution function for the grid point that is closest to its production point to determine the pixel ID that collected this electron. Since all PIXELs are identical, we only need to make coordinate transformation if any electron is produced outside the pixel where the grid is built and repeat the same operation to finish the whole simulation for a charged track. The speed of the simplified simulator is a few seconds per charged track. The accuracy depends on the granularity of the grid and can be very good with high granularity. However this speed is still too slow to be used in simulation a central Au+Au collision which generates a few thousands of charged tracks. We are developing the third version of the simulator aiming to increase the speed by two orders of magnitude while keeping good accuracy.

Embedding and Pile-Up

The embedding of simulated tracks into the raw data stream (which provides the best 'background environment' for track/particle reconstruction and therefore the best way to estimate accurate efficiency numbers for physics analysis) has been around the heavy ion community for about fifteen years. It is the merging, at the raw ADC level, of a pedestal-subtracted event, for a given detector, with a few, slow-simulated hits. The resulting output is then passed through the reconstruction chain and the output is compared to MC input (this step is performed by the so-called Association Maker in STAR experiment). During the merging of real data with simulated hits and tracks one read the appropriate calibration tables so the dead areas of the detectors are properly excluded.

IST Embedding

As we mentioned above the IST could benefit from existing or under development SSD embedding code and adapt it with minor modifications

PIXEL Embedding and Pile-up simulation

The embedding task in the PIXEL layers is more complex since cluster and hit finding is done online. Also, in simulations, one has to properly account for out-of-time events, Pile-up hits. To simulate the PIXEL pile-up hits, we produced one standalone ROOT file containing only the required PIXEL hits multiplicity in both inner and outer layers. The hits are produced from GEANT using the same setups as in the production for CD0 simulation. The hits in this file are then merged with the PIXEL hits in every central collision that is pushed through STAR reconstruction software.

According to the CD0 proposal, the pileup hits density for 1x RHIC-II luminosity is $43/cm^2$ on the inner PIXEL layer and $6/cm^2$ on outer PIXEL layer. The pile-up hits densities under different assumption on the RHIC-II luminosity are listed in the following table. For each of the assumed luminosity, we produced one pile-up hits file.

luminosity	Inner later pile-up hits density	Inner later number of pile-up hits	outer later pile-up hits density	outer later number of pile-up hits
0.5xRHIC-II	21/cm2	6600	3/cm2	2638
1xRHIC-II	43/cm2	13514	6/cm2	5276
2xRHIC-II	86/cm2	27000	12/cm2	10550
3xRHIC-II	129/cm2	40500	18cm2	15826

This method neglects the fluctuation of pile-up hits density in different location of PIXEL detector since for every event, only one set of pile-up hits is applied. In the future, we plan to directly apply white noise on the PIXEL detector before reconstruction happens. This will include the local density variation and is an improvement to the old method.

Association Makers

The step of association comes directly after the embedding. Its basic functionality, which already exists in the STAR framework, is to correlate the MC input with the reconstructed output so one can calculate hit, track, decay-vertex etc finding efficiency. This is done either through the use of an embedded key (idtrue) in the hit structure or by 'proximity association' of reconstructed and MC clusters. The later one is less accurate and not suitable for our purposes. Currently the Association software generates a structure that contains enough correlated (matching) information to allow hit/track and partial decay-vertex evaluation. The current output is usable but not optimized for our purposes; one has to go through several steps in order to be able to perform a detailed evaluation. The current scheme will need to be modified or augmented to include vital information that will facilitate our work.

Analysis of Simulated Data

There are software modules needed exclusively during the evaluation of simulations, either full-event simulations or embedding. These are in general smaller, utility-type pieces of code. Most of these modules already exist in some form and it is a minor effort to adapt them to HFT.

3.6.5. Physics Analysis Framework

The physics analysis software is the most critical part in signal extraction. When it comes to physics analysis people use a diverse set of tools and methods to extract the physics signals, most of them developed by themselves. Most of the tools and infrastructure needed is either already in place or under development in current charm analyses. Here we will only indentify the broad areas of physics interests for the HFT mainly for the purposes of recording the institutional interests, responsibilities and commitments. These areas are: a) Charm-meson, b) Charm-baryon, c) B-meson reconstruction and d) possible spin-related signals. These are the areas discussed in the next Section.

3.6.6. Institutional Responsibilities

Institutional commitments

The following discussion reflects and summarizes the software interests of the participating institutions at the time of writing of this CDR. Even though it is possible that institutional interests might get modified and shifted with time, it is expected that institutions with responsibility in key software areas (as discussed above) will provide the manpower needed to deliver their modules.

Resources required

From a review of the required tasks one can categorize the required resources into two broad categories: a) effort contributed by the participating institutes and b) effort expected from collaboration resources. A first estimate is that HFT institutions should contribute at least the equivalent constant effort of three FTEs for the lifetime of the project (about a decade), and the collaboration the equivalent constant effort of about one FTE, mainly in infrastructure areas (simulations, tracking, databases etc). The collaboration areas of contribution appear under the BNL institution label in Table below.

Institutional Responsibilities and Commitments

After consultation with the institutional representatives the following Table summarizes their current interests and commitments to software tasks as outlined and discussed above. At this point only a broad categorization and grouping is attempted and not a detailed outline of commitments within a more general task. Details of implementation will be discussed and defined in the group's weekly meetings.

Software task		BNL	UCLA	KSU	NPI	MIT	LBL	Purdue	
Online									
	IST					X			?
	Pixel						X	X	?
Offline									
Hit Reconstr.	IST					X			
	Pixel						X	X	?
Tracking		X							?
Event Vertex		X		X	X				
Decay Vertex		X		X	X				
Calibration Db	IST					X			?
	Pixel						X	X	
Alignment	IST	X		X		X			
	Pixel	X		X			X	X	
Simulation									
Geometry	IST	X				X			
	Pixel	X					X		
Fast/Slow Sim.	IST			X		X			

	Pixel						X	X	
Embed./Pileup	IST			X		X			
	Pixel						X	X	
Assoc/Analysis		X		X	X				
Physics Analysis									
Charm			X	X	X		X	X	
Bottom			X				X	X	
Λ_C				X	X		X		?
Spin							X		

Other collaboration contributed resources

3.7. Cost and Schedule

4. Resources

5. Appendix 1

5.1. Description of the Pixel RDO System

This document is an extension of the Pixel RDO addendum to the HFT proposal. It is intended to give detailed parameters of the function of the Pixel readout system that will allow for the understanding of the logic and memory and requirements and the functionality of the readout system. We will present the designs of the Phase-1 and Ultimate readout systems under periodic triggering conditions. The simulation of the system response to random triggering of the type expected to be seen at the STAR experiment is ongoing and will be available upon completion. The readout design is highly parallel and one of the ten parallel readout systems is analyzed for each system.

5.1.1. Phase-1 Readout Chain

The Phase-1 detector will consist of two carrier assemblies, each containing four ladders with ten sensors per ladder. The readout is via parallel identical chains of readout electronics. The relevant parameters from the RDO addendum are reproduced in Table 15.

Item	Number
Bits/address	20
Integration time	640 μs
Hits / frame on Inner sensors (r=2.5 cm)	295
Hits / frame on Outer sensors (r=8.0 cm)	29
Phase-1 sensors (Inner ladders)	100
Phase-1 sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5

Table 15: Parameters for the Phase-1 based detector system used in the example calculations shown below.

The functional schematic of the system under discussion is presented in Figure 63.

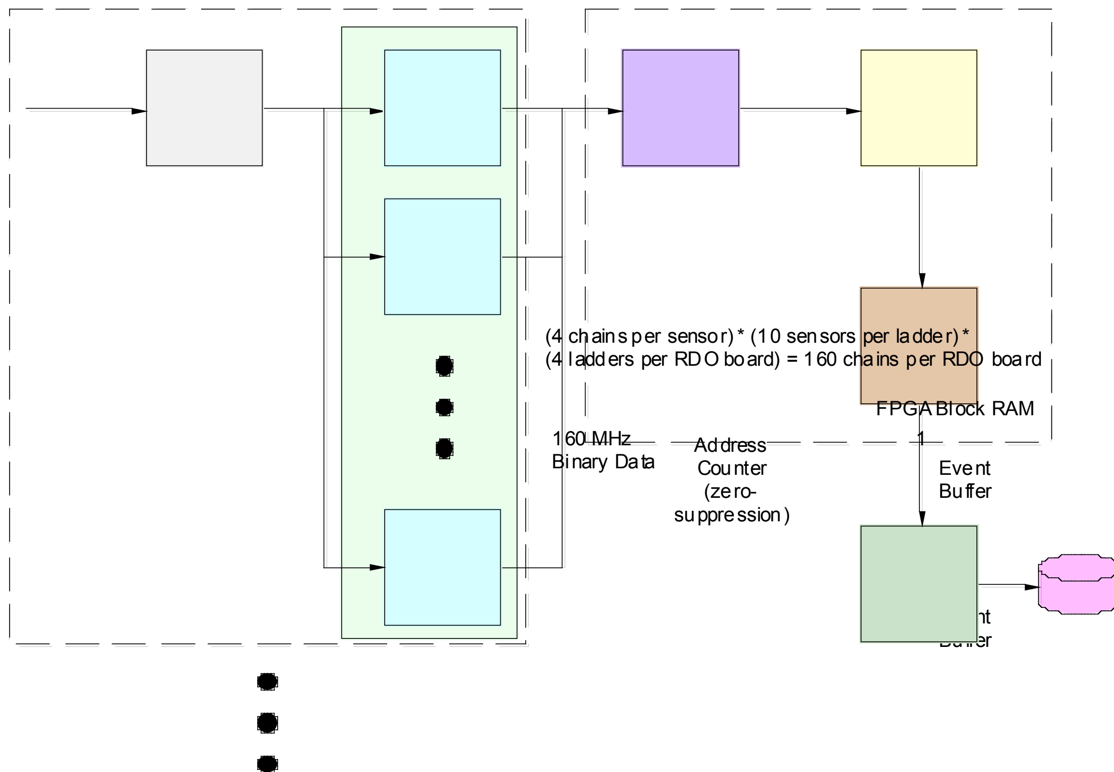


Figure 63: Functional schematic diagram for one Phase-1 sensor based RDO board. Each RDO board services one inner ladder and 3 outer ladders. Each ladder contains 10 sensors.

We will show the system function for two cases. The first is for a periodic trigger rate of 1 kHz. The second is for a periodic trigger rate of 2 kHz. These cases make the scaling clear. In both cases we will use the average (pile-up included) event size. We are currently simulating the dynamic response of the system to the triggering and event size fluctuations seen at STAR and will make this information available after the simulations are completed. It is important to note that the system is FPGA based and can be easily reconfigured to maximize the performance by the adjustment of buffer sizes, memory allocations, and most other parameters. The relevant parameters of the system pictured above are described below;

<u>Data transfer into event buffers</u> – The binary hit data is presented to the address counter at 160 MHz. The corresponding hit address data from the adders counter is read synchronously into the event buffers for one full frame of a 640 × 640 sensor at 160 MHz. This corresponds to an event buffer enable time of 640 μs.

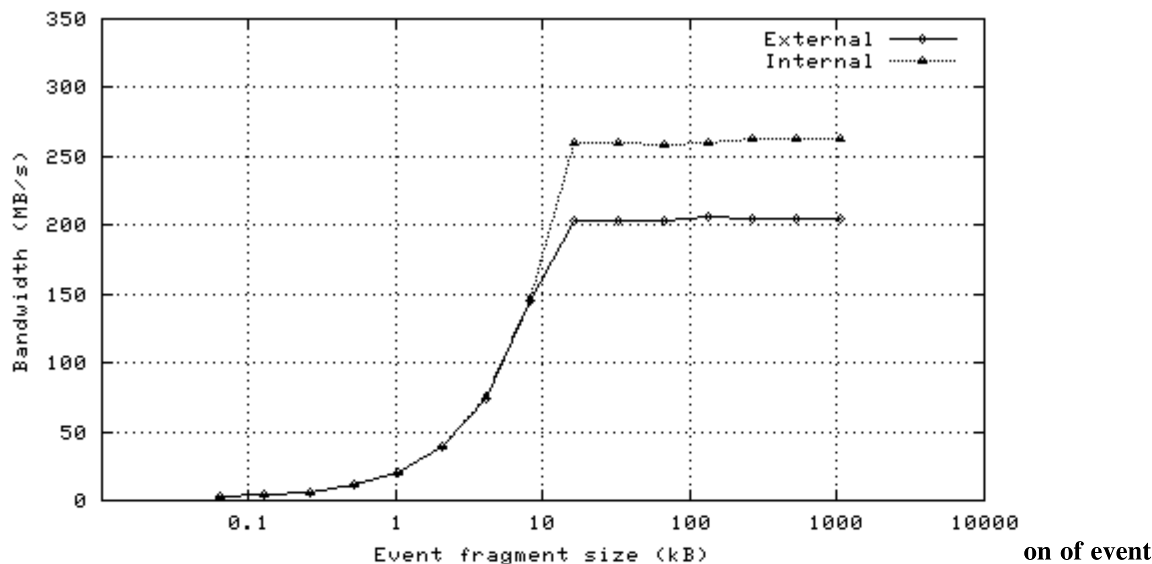
<u>Event Buffers</u> – Each sensor output is connected to a block of memory in the FPGA which serves as the storage for the event buffers. Each block of memory is configured as dual ported RAM and. The overall FPGA block RAM used per sensor output is sized to allow for storage of up to ten average events with event size fluctuation. This leads to a total buffer size that is 20 × the size required for the average sized event (different for inner and outer sensors). The FPGA block RAM will be configured with pointer based

memory management to allow for efficient utilization of the RAM resources. The average inner sensor has 295 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (295 hits) × (20 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 7,375 bits**.** Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each inner sensor output is 73,750 bits or 3,688 20-bit addresses**.

For outer sensors, the event buffer size is calculated similarly. The average outer sensor has 29 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (29 hits) × (20 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 725 bits**.** Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each outer sensor output is 7250 bits or 363 20-bit addresses**.

Data transfer into the RDO buffer via the event builder – This process is internal to the FPGA, does not require computational resources, and can run at high speed. In the interests of simplicity, we will assume a 160 MHz clock to move data in 20-bit wide address words. The event builder first adds a 128 Byte header that contains the trigger ID and other identifying information into the RDO buffer, and then moves the address data from the event buffers into the RDO buffer in 20-bit words. The average carrier event size is [(29 hits / sensor (outer)) × (10 sensors) × (3 ladders) + (295 hits / sensor (inner)) × (10 sensors) × (1 ladders)] × (2.5 hits / cluster) = **9550 address words (20-bit)**. The RDO buffer is 5 × the size required for an average event and is thus **955 kb** in size. The full time required to transfer the address data into the RDO buffer (in 20-bit per clock transfers) is then **59.7 μs**.

Data transfer from the RDO buffer over the DDL link – The RDO buffer is dual-ported and thus readout from the SIU to the RORC can proceed as soon as the RDO buffer begins filling. The data transfer rates for the SIU – RORC combination as a function of fragment size are shown in Figure 64.



on of event fragment size with an internal and external (DDL) data source using two D-RORC channels. From the LECC 2004 Workshop in Boston.

In this case, we will assume that we are padding the 20-bit address data to 32-bit word lengths for DDL transfer. The event size is then (32 bits) **×** (9550 address words) **= 305.6 kb or 38.2 kB.** In this example, our transfer rate is ~ 200 MB / s. This transfer then takes **191 μs.**

Data transfer to the STAR DAQ for event building – The event data is buffered in the DAQ PC RAM (>4GB) until only accepted events are written to disk and then transferred via Ethernet to an event building node of the DAQ system. Level 2 trigger accepts are delivered to the RDO system and transferred via the SIU – RORC to the DAQ receiver PCs. Only the events that have been accepted by level 2 are then built into an event. In this way, the buffer provided by the DAQ PC RAM provides for the elasticity needed for an average event acceptance of 1 kHz

The results of these calculations and discussion are presented below in the chronograms in Figure 65 and Figure 66.

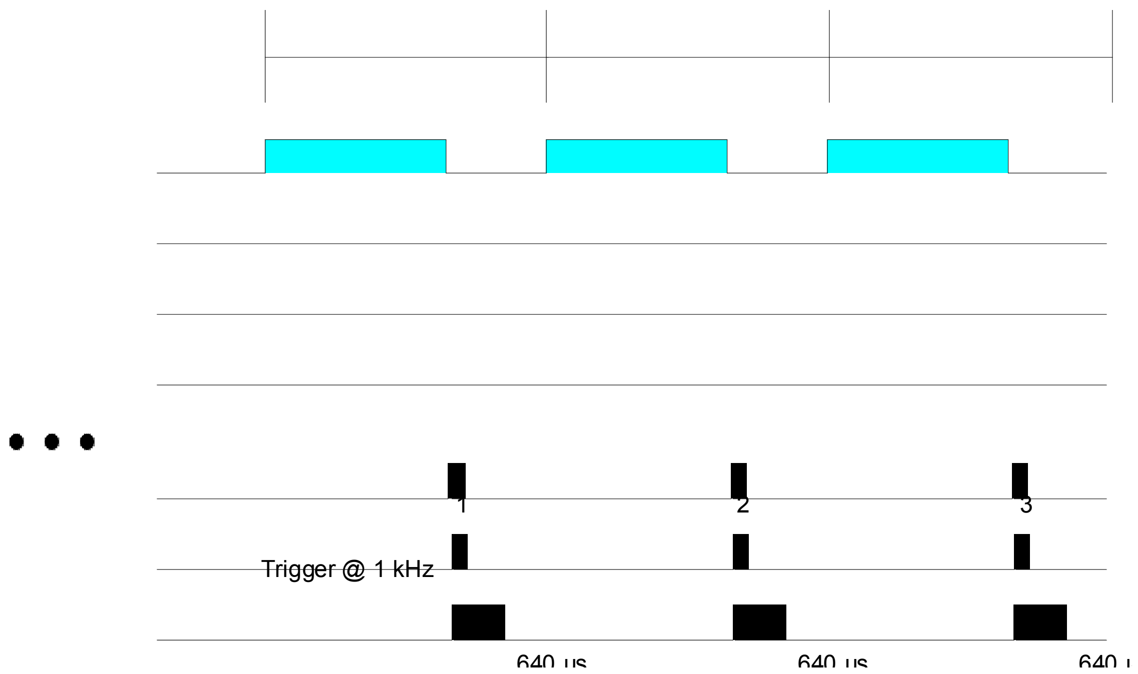


Figure 65: Chronogram of the Phase-1 based readout system functions for a 1 kHz periodic trigger.

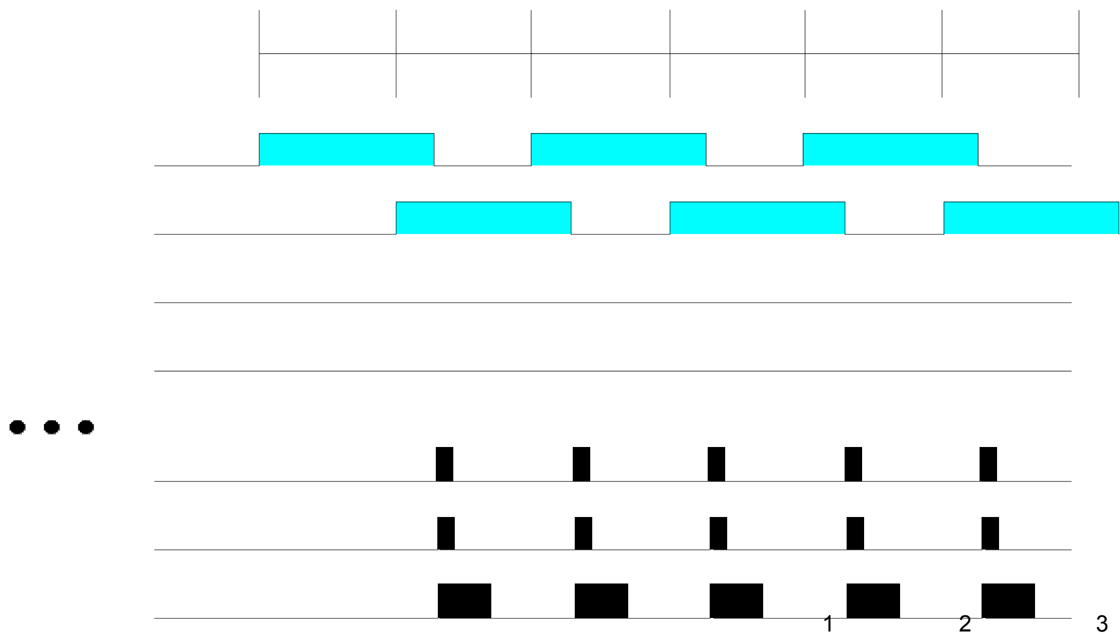


Figure 66: Chronogram of the Phase-1 based readout system functions for a 2 kHz periodic trigger.

The memory resources required in the FPGA / motherboard combination for this readout design are (120 outer sensor readout buffers) × (7.25 kb per event buffer) + (262.5 kb for the RDO buffer) + (40 inner sensor readout buffers) × (73.75 kb per event buffer) + (955 kb for the RDO buffer)= **4775 kb**. The Xilinx Virtex-5 FPGA used in our design

contains 4.6 – 10.4 Mb of block RAM so the entire design should fit easily into the FPGA.

Ultimate Sensor Detector Readout Chain

Again, the Ultimate sensor readout system consists of ten parallel readout chains. The main difference between the Phase-1 sensors and the Ultimate sensors is the inclusion of zero suppression circuitry in the Ultimate sensor, thus only addresses are read out into the RDO boards. In addition, the integration time of the Ultimate sensor is 200 μs and there are two data outputs per sensor. These differences lead to the functional schematic of the readout system shown in Figure 67.

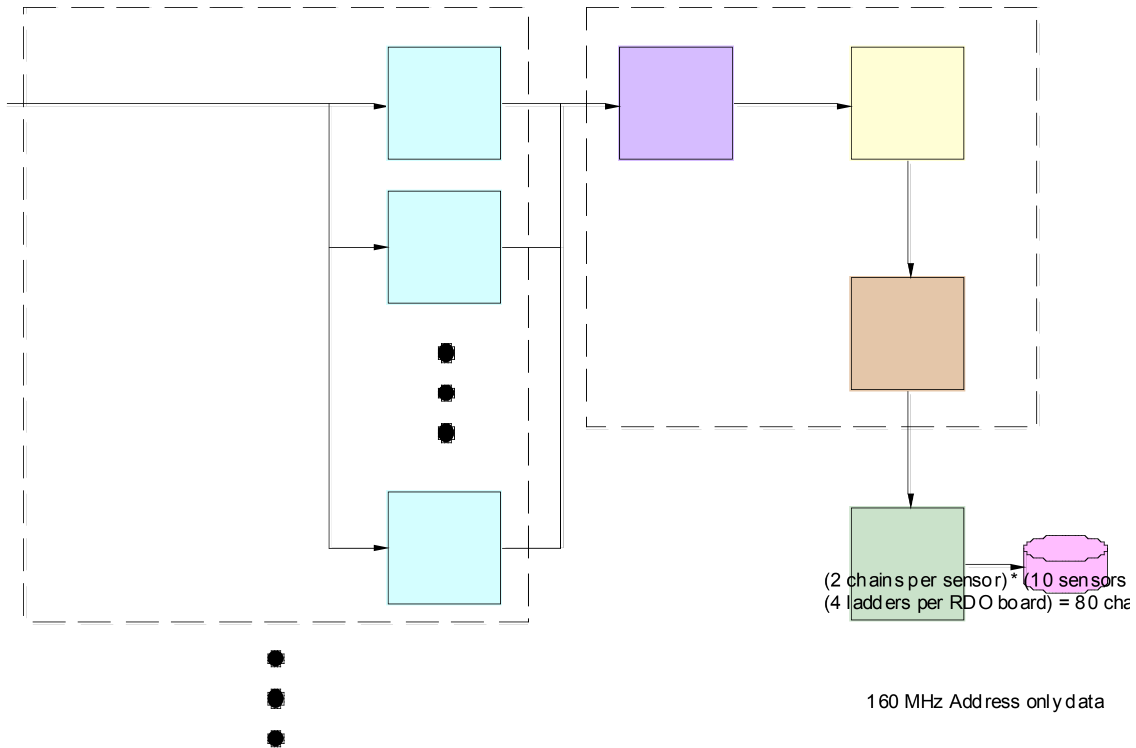


Figure 67: Functional schematic diagram for one Ultimate sensor based RDO board. Each RDO board services one inner ladder and 3 outer ladders. Each ladder contains 10 sensors.

We will show the system function for the same two cases as shown for the Phase-1 readout system. The first is for a periodic trigger rate of 1 kHz. The second is for a periodic data rate of 2 kHz. Again, in both cases we will use the average (pile-up included) event size. The relevant parameters of the Ultimate sensor based system pictured above are described in Table 16.

Item	Number
Bits/address	21
Integration time	200 μs
Hits / frame on Inner sensors (r=2.5 cm)	246
Hits / frame on Outer sensors (r=8.0 cm)	24
Ultimate sensors (Inner ladders)	100
Ultimate sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5
Average Trigger rate	1 kHz

Table 16: Parameters for the Ultimate sensor based detector system used in the example calculations shown below.

Data transfer into event buffers – The 21-bitaddress data is presented to the event buffer 160 MHz. The integration time is now 200 μs giving an event buffer enable time of 200 μs.

Event Buffers – Again, we will calculate the amount of FPGA block RAM required for the event buffering. The average inner sensor has 246 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (246 hits) × (21 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 6150 bits. Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each inner sensor output is 64,580 bits or 3,075 21-bit addresses**.

For outer sensors, the event buffer size is calculated similarly. The average outer sensor has 24 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (24 hits) × (21 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 630 bits. Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each outer sensor output is 6300 bits or 300 20-bit addresses**.

Data transfer into the RDO buffer via the event builder –We will again assume a 160 MHz clock to move data in 20-bit wide address words. The event builder first adds a 128 Byte header that contains the trigger ID and other identifying information into the RDO buffer, and then moves the address data from the event buffers into the RDO buffer in 20-bit words. The average carrier event size is [(24 hits / sensor (outer)) × (10 sensors) × (3 ladders) + (246 hits / sensor (inner)) × (10 sensors) × (1 ladders)] × (2.5 hits / cluster) = **7950 address words (21-bit)**. The RDO buffer is 5 × the size required for an average event and is thus **835 kb** in size. The full time required to transfer the address data into the RDO buffer (in 21-bit per clock transfers) is then **49.7 μs**.

Data transfer from the RDO buffer over the DDL link – The RDO buffer is dual-ported and thus readout from the SIU to the RORC can proceed as soon as the RDO buffer begins filling. Again, we will assume that we are padding the 20-bit address data to 32-bit word lengths for DDL transfer. The event size is then (32 bits) × (7950 address words) **= 254.4 kb or 31.8 kB.** In this example, our transfer rate is ~ 200 MB / s. This transfer then takes **159 μs.**

Data transfer to the STAR DAQ for event building – Again, only the events that have been accepted by level 2 are then built into an event. In this way, the buffer provided by the DAQ PC RAM provides for the elasticity needed for an average event acceptance of 1 kHz

The results of these calculations and discussion are presented below in the chronograms in Figure 68 and Figure 69.

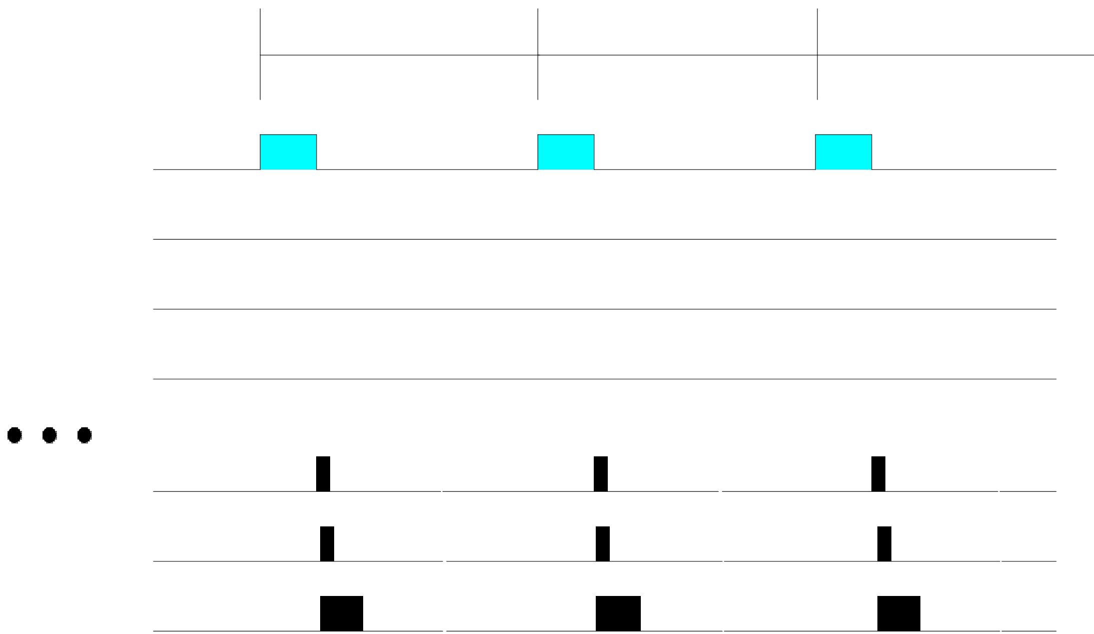


Figure 68: Chronogram of the Ultimate sensor based readout system functions for a 1 kHz periodic trigger.

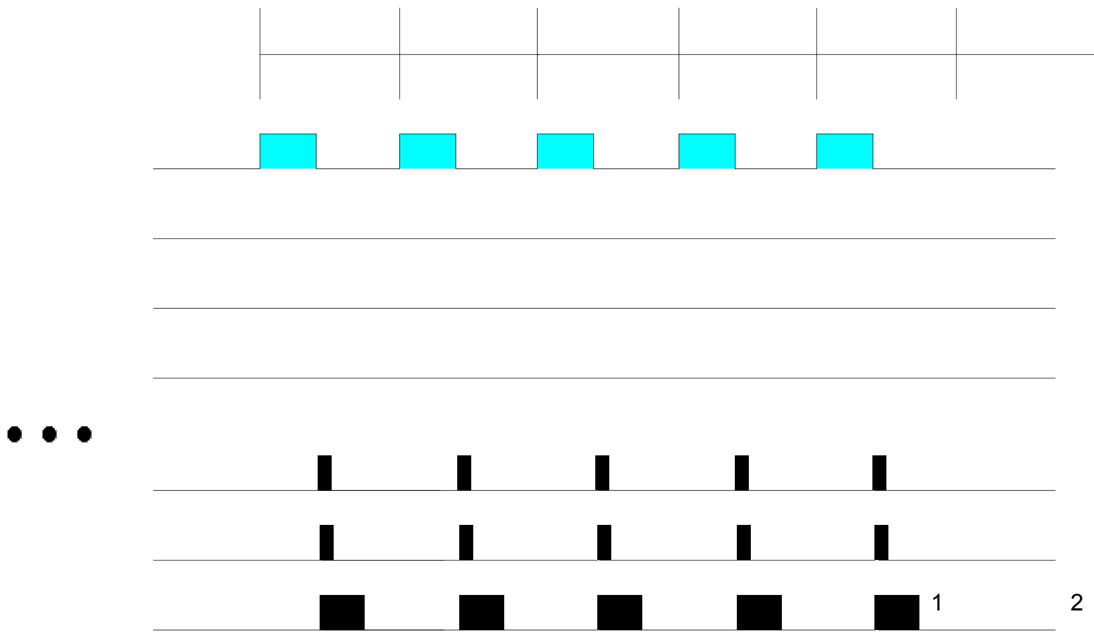


Figure 69: Chronogram of the Ultimate sensor based readout system functions for a 2 kHz periodic trigger.

The system memory resource requirements are somewhat less than those required for the Phase-1 RDO system. This fits easily into the memory resources of the Virtex-5 FPGA.

6. Appendix 2

6.1. Mechanical Design Simulation and Analysis

A number of mechanical design studies have been carried out to find designs that can meet requirements of stability and cooling. The work reported here has been carried out by either ARES corporation or us. These analyses are not complete at this time, but they provide a starting point for prototype work which can be expected to achieve the required performance.

6.1.1. Ladder support Structural analysis

The mechanical design of the pixel support system must meet stringent position stability requirements while also minimizing radiation length. The basic support design analyzed is pictured in Figure 18, but some analysis are also reported for alternative designs that have been considered.

The issues investigated are:

- Ladder backing stiffness required to hold thinned silicon flat against it's tendency to curl
- Support strength to control gravity sag
- Support strength to control deformation from air flow pressures
- Control of thermal expansion induced deformation
- Control of moisture expansion induced deformation
- Support strength to handle insertion loads

Control of Silicon Curl

The pixel chips are mounted on flex cables with a composite backing and these ladders are mounted on a thin large moment carbon composite tubes shown as green in Figure 18. The tubes are the primary source of support and the ladder backers provide support for handling plus these backers must also provide support for the 1 cm overhang of the ladders. In the overhang region the backer provides the only mean for holding the thinned silicon chips flat. Without backing the silicon chips tend to curl as a result of the stresses imposed in the silicon during chip fabrication. A simple analysis shows that a 2 mil thick carbon composite will allow the silicon to curve out of plain by 700 microns. A thicker but less dense backer of perhaps open weave carbon composite that is 10 mils thick will limit the deformation to 30 microns while maintaining a 0.02% X_0 budget for the backer, namely the equivalent of 2 mils carbon composite. This deformation is outside of the 20 microns envelope, but the deformation will be mapped and the stability should satisfy the 20 micron specification.

Control of Gravity Sag

The most critical component for controlling deformation from a variety of sources is the sector tube shown in Figure 18. This structure is in the tracking path and thus requires the most attention to radiation thickness. Analysis of the sector tube control of gravity sag has been carried out by us and by the ARES corporation. The ARES analyses, included details of the composite weave, and showed that a sector tube could be fabricated with a thickness of 120 microns and more than satisfy our 20 micron stability requirement giving a gravitational displacement of less than 6 microns. We have performed a similar analysis, but with an isotropic modulus representation of the composite. This work shows a 5 micron deformation for the detector elements and 35 microns for other parts of the structure, but with the addition of an end lip the analysis gives a gravitational detector displacement limited to 0.6 microns and the maximum displacement of the structure is 4 microns (see Figure 70). These results show that gravity induced distortions are not a problem with this design. As will be shown other contributions to deformation are more significant.

Control of Airflow Induced Deformation

The deformation and vibration induced on the detector support from the cooling air flow requires more study, but preliminary considerations indicate that the current structure could be adequate. The planned cooling air velocity, 8 m/s, has a dynamic pressure

$$p = \frac{1}{2} \cdot \rho_{air} \cdot v^2 = 6 \times 10^{-3} \text{ psi}$$

that acting on the area of the structure is 1.7 times the gravitational force. From the gravity analysis we conclude that the static deformation will be less than 2 microns. Again, vibration studies with prototype structures and possibly computational fluid dynamics (CDF) simulations will be done.

Control of Thermal Expansion Induced Deformation

One of the greatest potential sources of deformation is differential expansion resulting from changes in temperature between powered on and power off. It is planned to spatially calibrate or map the detector structures in a vision coordinate machine with the power off and the structure should not deviate from the map while powered on during operation by more than 20 microns. This requirement was one of the main reasons for choosing the current design with its large moment of inertia and consequently large stiffness. The ladder and beam structure being examined is illustrated in Figure 17 and Figure 18. It was found that the main issue requiring control is the bimetal thermostat effect from differential expansion. The problem is the result of the very large coefficient of thermal expansion (CTE) of the kapton cable compared to the rest of the structure. An analysis of a short section of the ladder shown in Figure 71 illustrates the problem where in this case the thermally induced displacement is 500 microns at the edge of the silicon.

A thermal expansion analysis of ladders plus support shows that by using a very compliant adhesive (3M 200MP) the kapton cable is largely decoupled from the structure greatly reducing the thermal induced bending. Simulation results shown in Figure 72

give a maximum deformation of 9 microns, well inside of the 20 micron requirement envelope.

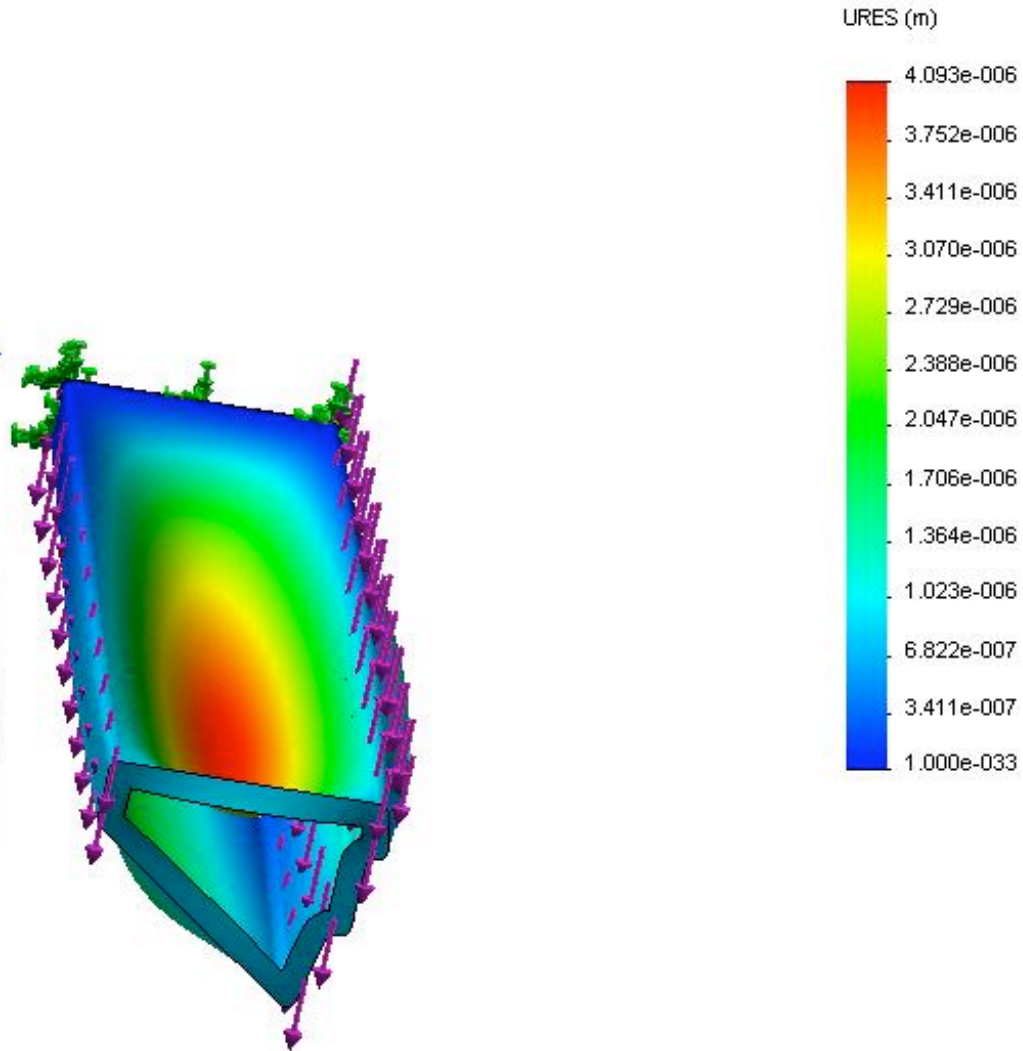


Figure 70: FEA results for gravity deformation of a 120 micron carbon composite support structure carrying 4 detector ladders.

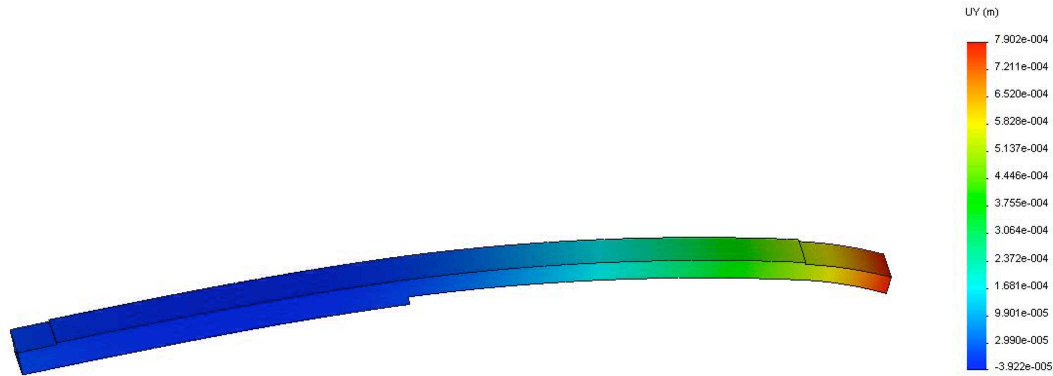


Figure 71: Short section of ladder structure showing problems with excessive thermal bimetal effect bending with using stiff adhesive. The 500 micron displacement resulting from a 20 deg C temperature change is driven by the large CTE of the kapton cable.

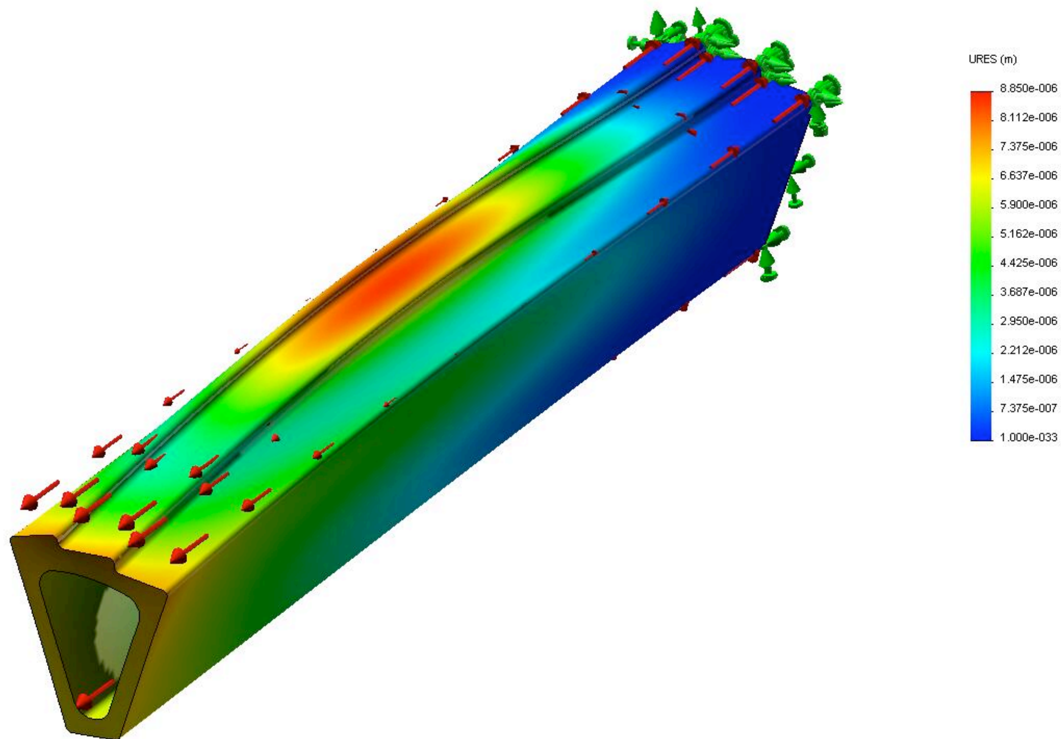


Figure 72: Thermally induced displacement of a sector beam with end reinforcement. The maximum resulting displacement is 9 μm. The beam and end reinforcement is composed of 200 μm carbon composite.

Control of Moisture Expansion Induced Deformation

The carbon composites expand with increased moisture content. There will be a long term reduction in the moisture content from the time of manufacture until completion of operation in the experiment environment which can potentially lead to unacceptable geometry changes. The ARES Corporation has studied this problem for us and has found

a composite layup configuration that meets our 20 micron requirement. This work appears on p. 99 and 102 of their summary report. They recommend a laminate: YSH-50/EX-1515 with a layup: [0, +60, -60]. The FEA analysis gives a maximum displacement of 16 microns. Further analysis and prototyping is required to address this issue. The inclusion of a soft decoupling adhesive may help as it appears to help in the thermal case.

Support strength to handle insertion loads

When the detector is inserted into the final docking position in the center of STAR it engages spring loaded over center latches into the kinematic mounts. The insertion supports have much less stringent stability requirements than the detector ladders since the positioning only has to be good enough to lie inside the kinematic mount engagement window which is ~1 mm, but the support must be able to handle the cocking load of the latches which is on the order of 15 lbs. Displacements must also be limited such that the two half detector cylinders do not collide during the insertion process. A FEA analysis of the supporting hinge structure has been done to check that it is adequate for cocking loads. The results of this analysis, shown in Figure 73, indicate that the design can safely handle the load without undue distortion. The analysis was not done on the latest complete hinge design, but an analysis of one part (see Figure 74) of the latest design shows that it is more than adequate.

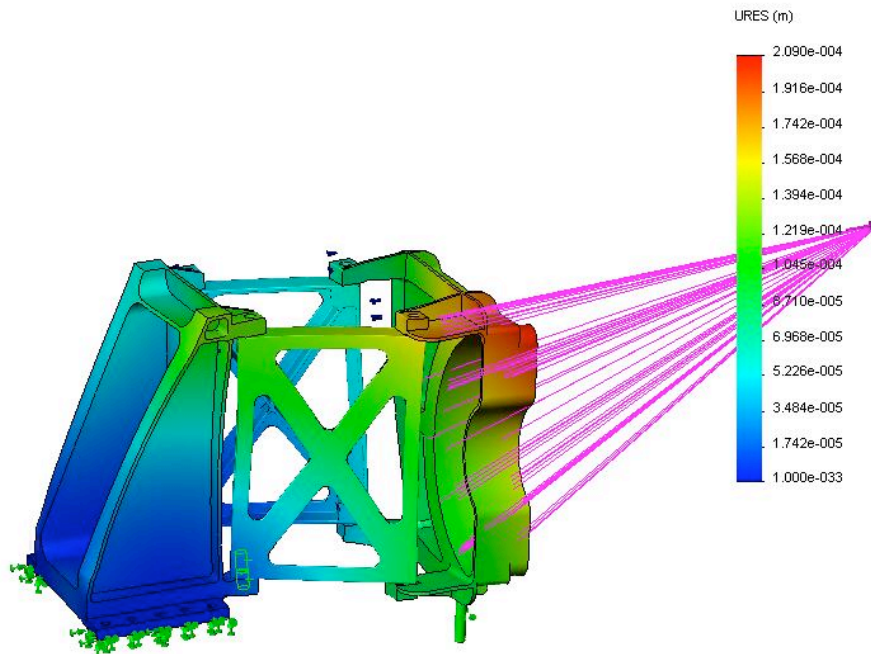


Figure 73: Displacement of an early insertion hinge design under cocking load of the latching mechanism. The displacement in the image is magnified by 140 and the maximum displacement is 210 microns. The pink lines show the position of the remote load as it is carried through the D tube, not shown.

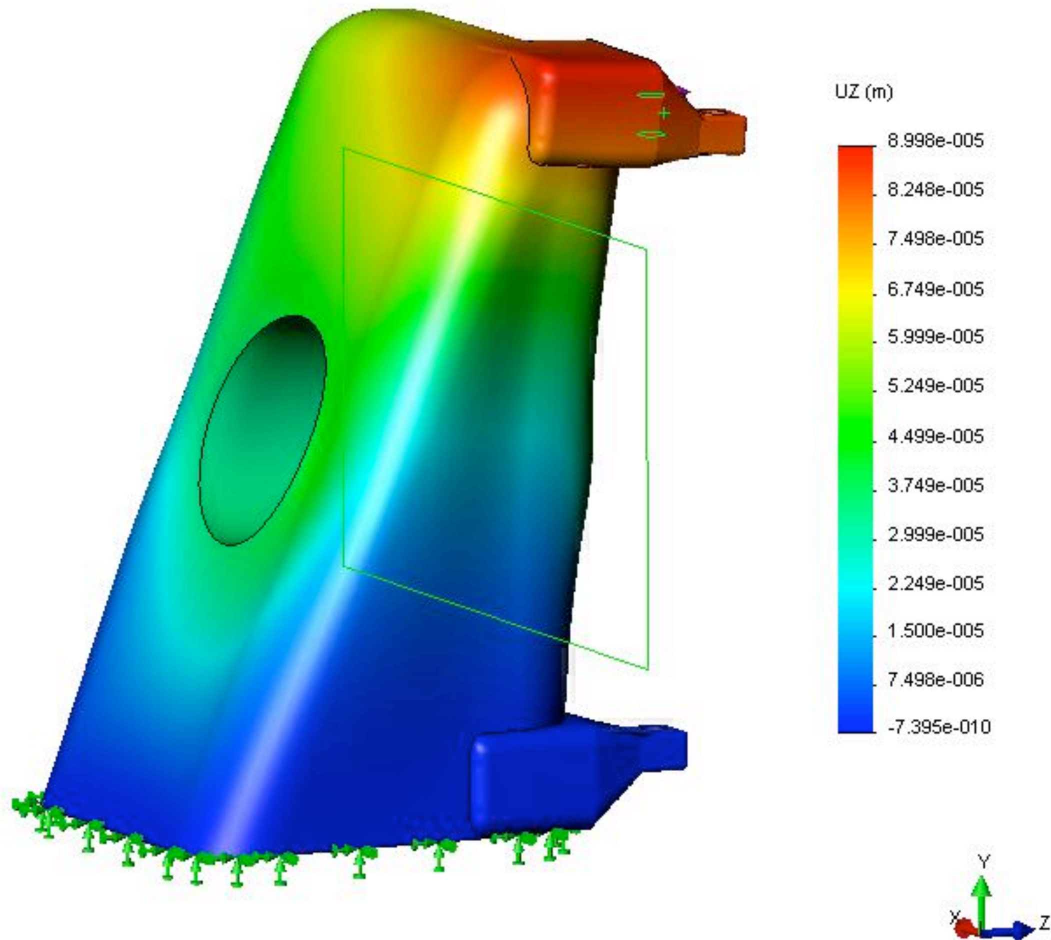


Figure 74: Distortion of support hinge backer under latch cocking load. The flexing in the beam axis direction is 90 microns.

Vibration of STAR central support

In STAR the central inner detectors such as the pixel detector are supported through the OSC and the ISC to TPC end caps. An accelerometer was mounted on the TPC end cap to measure possible vibrations that might couple to the pixel detector and affect position stability. A result from this measurement study (Figure 75) shows the response of a harmonic oscillator as a function of its resonant frequency to vibration if mounted directly on the end cap. This data can be used to set limits on expected vibration of various components and determine whether the performance of the detector is compromised. There are several components of the detector system which each have their own requirements with respect to stability and vibration.

Consider first the vibration of one pixel sector ladder support with respect to the other. This case affects directly the pointing accuracy of multiple tracks to a vertex and therefore the full resolution is required and the vibration should stay below the 9 micron RMS requirement. The fundamental frequency for the sector can be obtained from FEA analysis which gave a 6 micron movement under gravity load. The fundamental

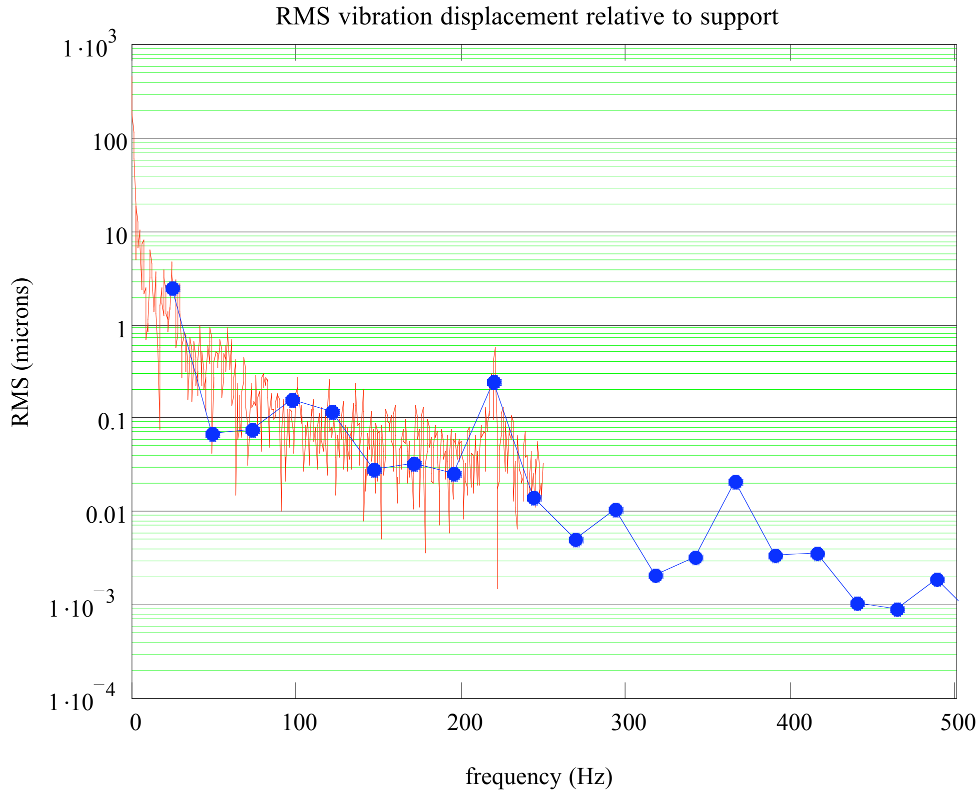


Figure 75: This shows the vibration response of mechanical harmonic oscillator mounted on the TPC end cap as determined with measurements of an accelerometer bolted to the TPC end cap. The two curves represent measurements made using two different methods of recording the data.

frequency is

$$f = \frac{1}{2\cdot\pi}\cdot\sqrt{\frac{g}{d}}$$

or 200 Hz for the 6 micron sag under gravity. From Figure 75 this gives a RMS vibration of .04 microns which is completely negligible compared to our 9 microns requirement. This vibration from this source will actually be significantly less than this because the sector is not directly coupled to the TPC wheel. The less stiff OFC and IFC provide the connection reducing the high frequency coupling.

The next element to consider is the pixel half cylinder as a whole. The stability of this element is most important for track matching from the IST, so the stability of this element should be good enough that it does not compromise the IST pointing resolution, namely it

should be less than 100 microns RMS. It is preferable though to be within the pixel limit since there are overlapping pixels between the two half cylinders. The ARES analysis p. 144 gives a fundamental frequency of 110 Hz for the pixel half cylinder when supported on the kinematic mounts. This, according to Figure 75, gives a RMS vibration of 0.2 microns which again is insignificant.

Finally the vibration of the OFC can be checked. The stability of this element only has to be good enough to not compromise the TPC tracking precision which is ~ 1 mm. It is expected that the OFC will be built with a gravity sag of 1 mm or better which was the number for the old support cones that are being replaced by the OFC. The fundamental frequency for this displacement is 16 Hz which according to Figure 75 gives ~ 4 microns RMS vibration. Again, this is not an issue compared to the 1 mm requirement.

6.1.2. Ladder Cooling Analysis

Air cooling has been chosen for the pixel detector in order to minimize multiple coulomb scattering and a number of studies have been carried out to optimize the air cooling design. Original tests with a heated ladder in a fan driven air stream indicated that ladders with heat loads of 100 mW/cm^2 could be successfully cooled with a moderate air velocity. A study by ARES Corporation, p. 73 found that an airflow velocity of 8 m/s through the sector beam was sufficient to limit the silicon temperature rise above ambient to 13 deg C. To accomplish this however additional cooling fins required under the outer layer of silicon which adds mass and complicates construction.

Bi directional air flow cooling

Since then more extensive, but still preliminary, CDF modeling has been done with air flow over both the inner and outer surfaces of the sector structure. The cooling simulation was run for one sector out of the 10 sectors in the complete pixel cylinder. The air flow path is shown in Figure 24 and Figure 76.

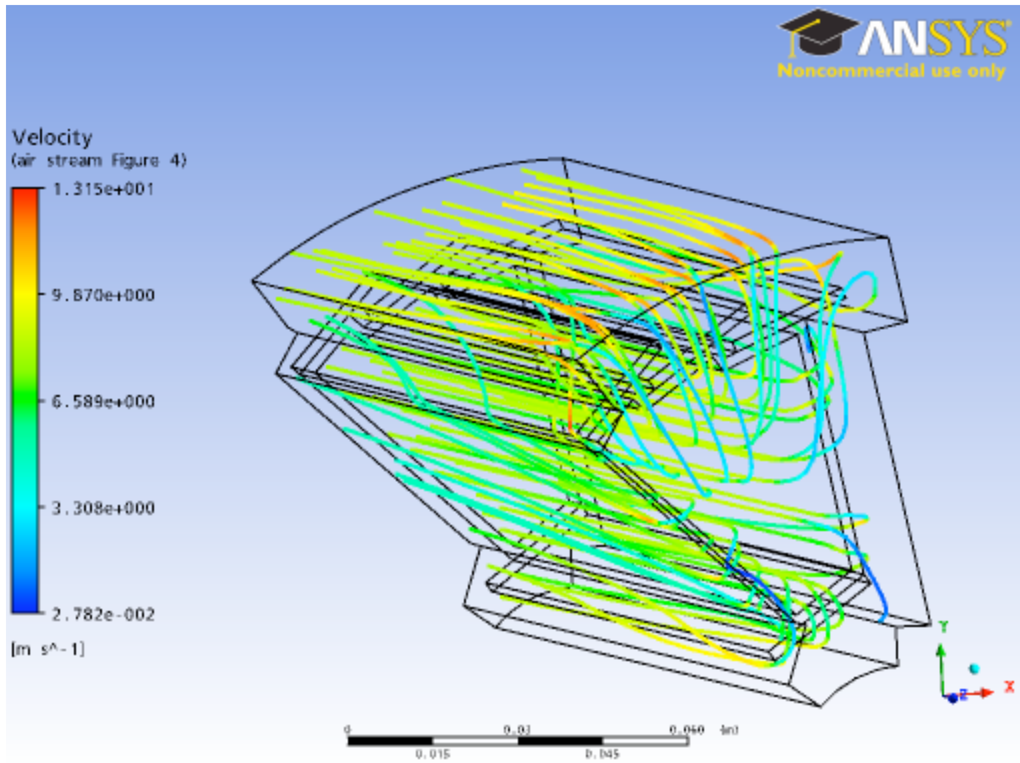


Figure 76: Stream lines showing the cooling air flow. The flow direction is from inside to outside. The color code shows air velocity.

The silicon surface temperature profile is shown in Figure 77.

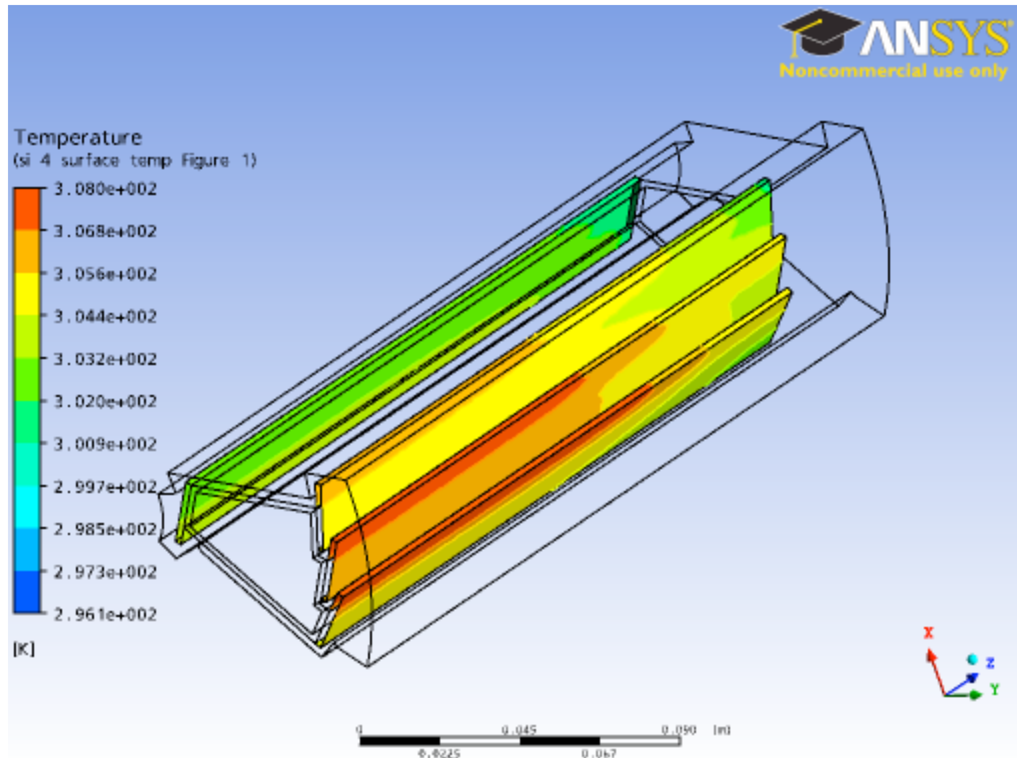


Figure 77; Surface temperature of silicon ladders. The maximum temperature increase above ambient is 12 deg C. The cooling air flows across both the inner and outer surfaces. The air enters from the left on the inside of the support beam, turns around at the right and exits on the left.

In this case an input air velocity of 8 m/s was used. This results in a maximum silicon temperature rise above ambient of 12 deg C which is acceptable. It is interesting to note that the inside ladders next to the beam pipe cool more effectively than the outside ladders. This is because the surface area of the support beam sides provides a significant fraction of the cooling.

The total air flow in this case for the full pixel detector barrel is ~280 CFPM and the temperature rise in the air for the total power of the ladders, 240 W, is 1.5 deg. C. This is a very small rise in the air temperature, so alternatives can be considered with reduced total air flow which would result in a smaller air cooling system.

Alternative air flow design

An alternative design has been investigated with reduced total air flow volume and an increased air velocity at the surface to improve the heat transfer. In this design the high velocity air flow is in the transverse direction local to the ladder surface (see Figure 78). The air flows through narrow slits in the ladder support beam from outside into the sector beam.

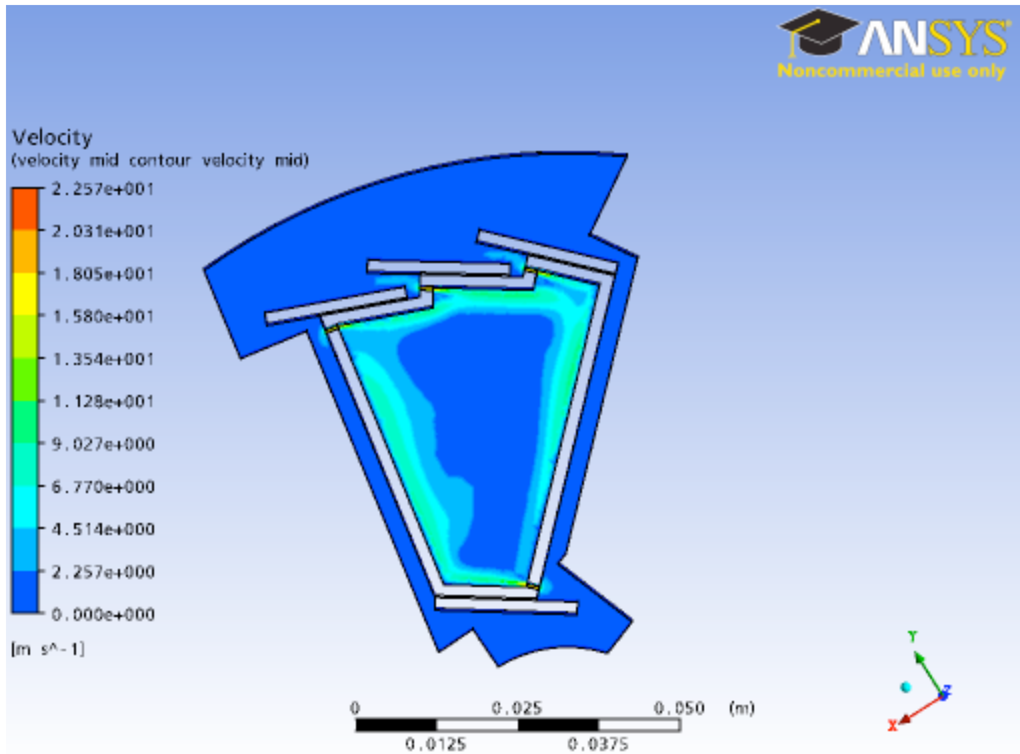


Figure 78: Sector cooling with transverse jets of cooling directed to the inside of the sector beam support structure through thin slots. The air velocity profile is shown in color. The air velocity near the surfaces beneath the ladders is 11 m/s.

The calculated surface temperature as shown in Figure 79 gives a maximum silicon temperature above ambient of 14 deg C. This is not quite as good as the performance with the simpler longitudinal bi directional cooling design with air flow over both inside and outside surface. For this reason future development will focus on the simpler longitudinal flow design.

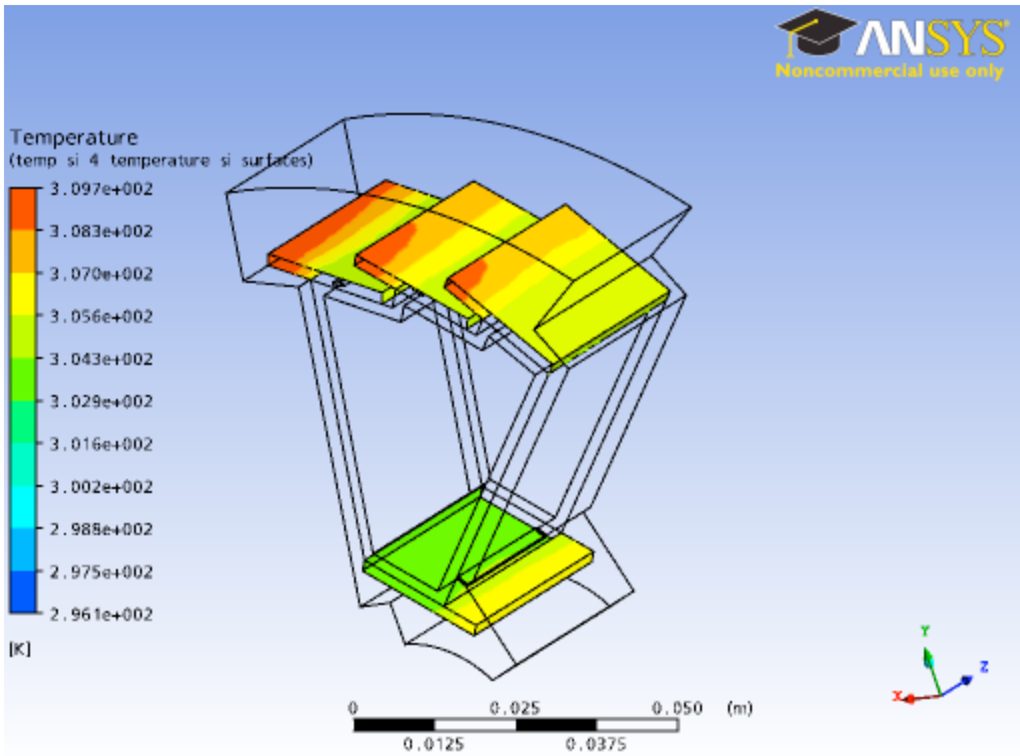


Figure 79: Silicon surface temperature profile for the transverse cooling jet design.

7. Appendix 3

LVDS Data Path Testing Discussion

The readout system architecture for the Phase-1 and Ultimate sensors to be used in the Pixel detector for the Heavy Flavor Tracker upgrade at STAR contains a high speed digital data path that is required to read out the sensor hits during the sensor integration time. This data path is well described in the addendum to the HFT proposal and can be found at http://rnc.lbl.gov/hft/hardware/docs/Addendum_rdo_2007_12_26.pdf. The RDO sensor data interface path requires that LVDS data move over a total distance of 6 – 8 meters with a speed of 160 MHz for Phase-1 and 125 MHz for Ultimate. 1-2 meters of this distance is over high impedance fine twisted pair wire. Since this design is challenging, though it works on paper, it is prudent to make a prototype set of testing boards and check the performance of our design as a precursor to starting a production design for the final set of readout boards. A diagram of the physical layout of the parts of the Pixel RDO system is shown as Figure 80.

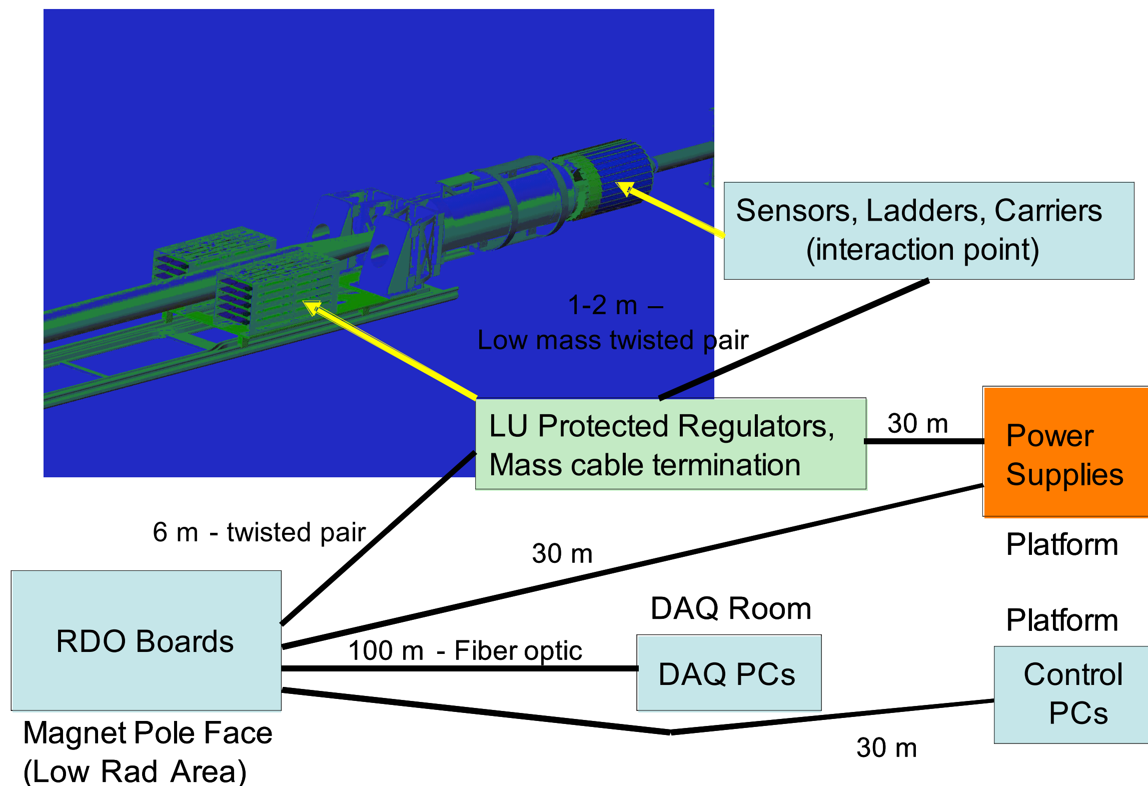


Figure 80: Physical layout of the RDO system.

To accomplish this testing task, we have constructed a set of PCBs that mock the components expected to be used in the final system. A functional system diagram is shown in Figure 81. We intend to produce a system that is a mockup of the complete data path for a single ladder starting and returning from the Virtex-5 development board. The wire used to connect the system boards will also be the same as what we expect to use in the final system. The fine twisted pair wire bringing LVDS signals to and from the ladder

are 42 AWG Wiretronic part # 2-42QPN-05 in two tested lengths, 1.0 m and 2.3 m. The cables carrying the LVDS signals from the mass termination boards to the Virtex-5 interface readout boards are 3M type 3644 CL2 rated.

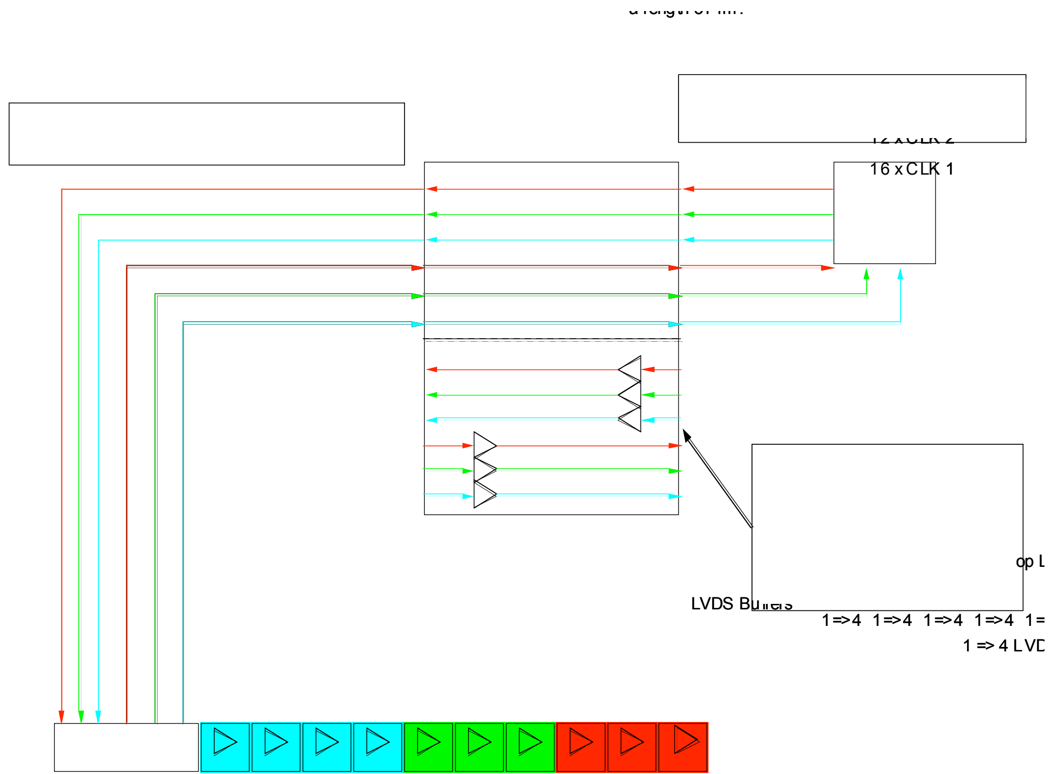


Figure 81: Functional block diagram of the LVDS data path test system.

Hardware

There are four basic components to the test system.

1. Mock Ladder – We have constructed a mock ladder. Since Phase-1 sensors are not available, we have used a LVDS 1:4 fan-out chip SN65LVDS104 to take the place of the Phase-1 sensor. The mock ladder contains ten SN65LVDS104s on 2 cm spacing, and six FIN1108 8-port LVDS repeater chips as buffers at the end of the ladder. The mock ladder receives 3 input LVDS signals that are multi-dropped in groups of 4, 3 and 3. Correspondingly, there are 40 outputs that are buffered at the ends of the mock ladder and carried to the Mass termination board. The mock ladder is constructed of standard FR4 with copper traces and has a finish thickness of 0.032” for 4 layers. We have constructed two mock ladders. They are identical except for the fine twisted pair signal wire lengths of 1.0 and 2.3 meters. A photograph of the mock ladder is shown as Figure 82.

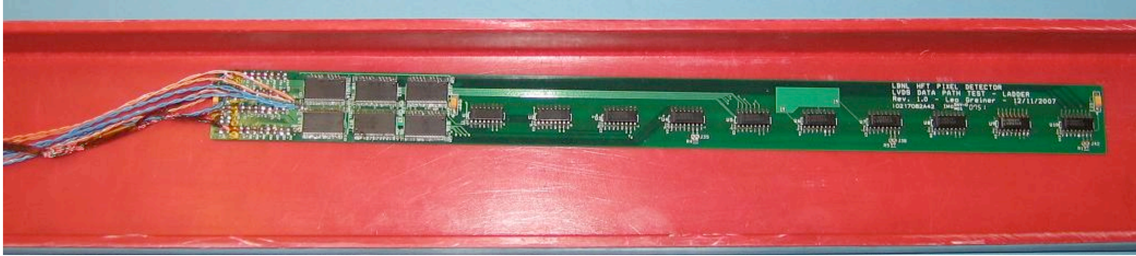


Figure 82: Mock ladder PCB as used in the tests.

2. Mass termination board – The mass termination board (MTB) is a close model of what we expect to have for a single ladder in the final system. Latch-up protected power is generated on the MTB and delivered to the mock ladder via 24 AWG wire. In the interest of testing multiple possible signal paths, the MTB used in these tests has two possible data paths. One is straight through from input to output connectors. The other is buffered with the same FIN1108 parts used on the mock ladder. A photograph of the MTB is shown as Figure 83.

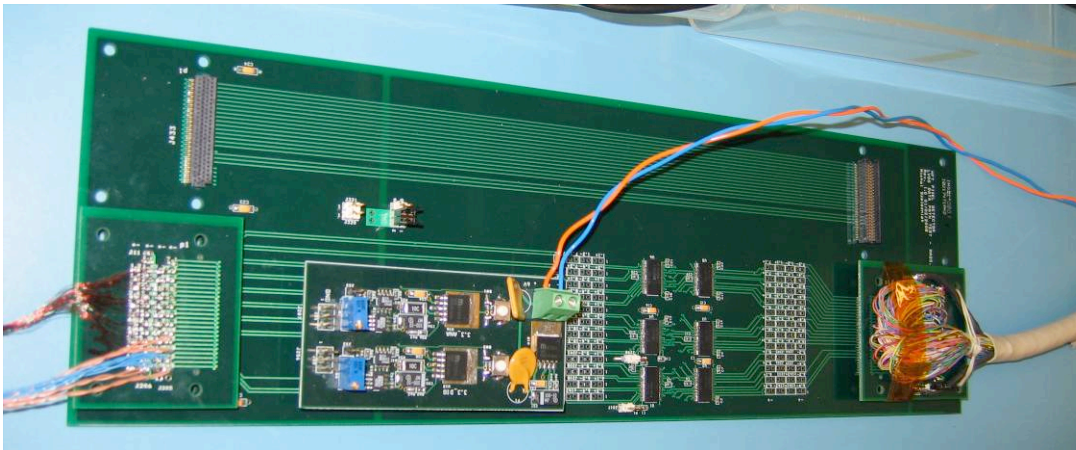


Figure 83: Mass termination board as used in the test. Ladder connection is to the left of the board, 6m cable to Virtex5 interface RDO board is on the right. The daughter card mounted to the middle of the board supplies latch up protected and monitored power. Note that there are two data paths. One is un-buffered and the other is buffered through Fin1108 LVDS buffers.

3. Virtex-5 interface – The Virtex-5 interface board (V5IB) attaches to the Xilinx Virtex-5 development board with a 1200 contact points. The data signals into and out of the Xilinx V-5 are buffered on the V5IB with FIN1108s. There are test points to look at all differential signals.

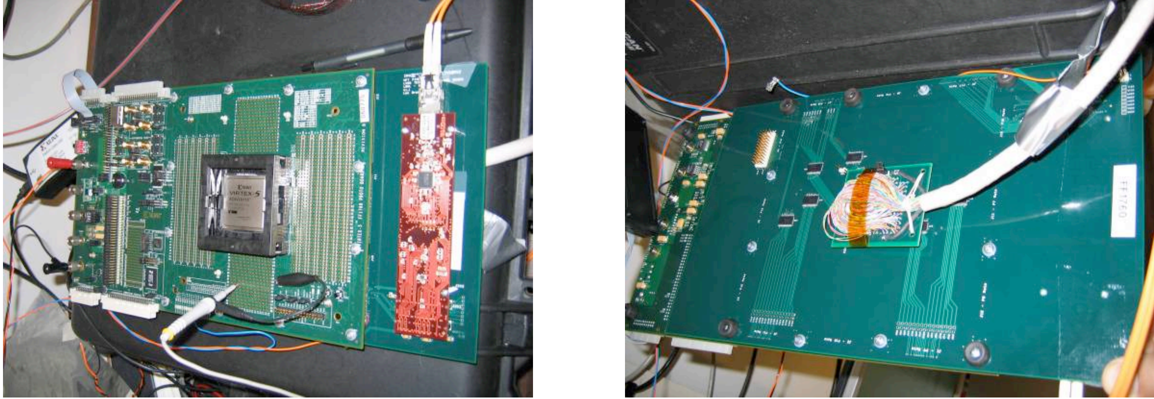


Figure 84: Vertex-5 interface board mounted to the Xilinx Virtex-5 development board. The top view is on the left showing the Xilinx Virtex-5 development board on top with the SIU visible on the V5IB. The photograph on the right shows the cable attachment and test points on the V5IB.

Firmware and Software

The firmware and software developed for the test have the primary task of measuring the time offsets needed to calibrate the IODELAY elements in the Virtex-5 FPGA. The IODELAY element is a function in the Xilinx Virtex-5 family of FPGAs that allows for the adjustment of the latching time on any input pin(s) with a very fine granularity. This is the essential functionality that allows us to do a channel by channel adjustment for each input. This compensates for all fixed time shifts in the system due to cable lengths, buffer propagation times, etc and allows the data transfer to be limited only by the intrinsic system jitter. There are two modes for operation of the firmware. The first mode of operation is a calibration of the system. In this mode, the firmware sends a single pulse through each channel of the system. The transit time through the system is measured for each LVDS channel and that data is sent over the fiber optic communication link (SIU) to the software in the DAQ RDO PC. The firmware then executes a sequence of steps where the timing of the latching of data into each of the FPGA inputs is varied in 75 ps steps via the IODELAY element and the transition of the received pulse from one clock cycle into the next is observed. This procedure is repeated 20 times for each input to map the range of the jitter envelope. The data is transferred via the SIU into the software in the DAQ PC where it is used to calculate the optimum delay setting for each individual input that places the average midpoint of the data pulse at the FPGA latch time. This data is then transferred back into the FPGA to set the optimum delay for each i/o pin and the FPGA is then set to the bit error rate mode. In this mode, pseudo random data is generated and transferred (with different offsets) over the three data outputs. In the firmware, each data path is checked against what was sent and errors are counted.

Operation of the LVDS Test System

The Virtex-5 development board generates 3 streams of pseudo random data that are fed through the data path chain and returned to the V5IB. Each stream of data is compared to what was sent and any errors are counted. The results are then displayed on LEDs on the V5 development board and can be read out over the SIU interface. In this way we have tested the following;

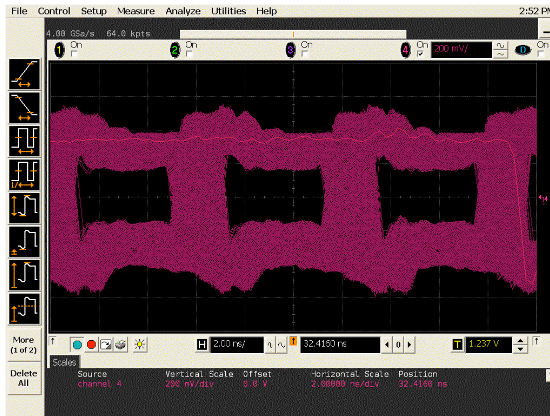
- 1 full data path for a complete ladder.
- Multi-drop LVDS distribution in groups on 4, 3, 3.
- Cross-talk through the whole system – each muti-drop group carries different random data.
- The signal paths on the PCBs and the cabling are as comparable as possible to the final implementation.
- External SIU communication and software/firmware to set IODELAY for each channel.
- Bit error rate for different read out frequencies, paths, cables, etc.

Results

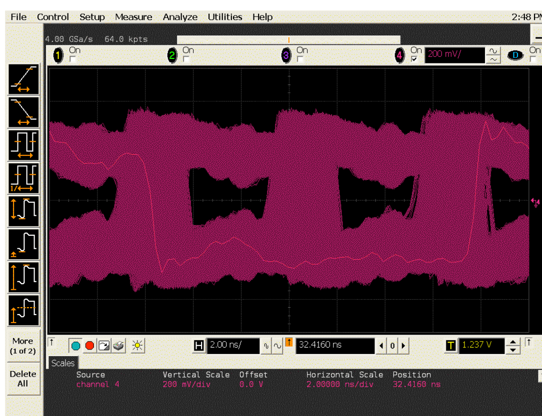
The test system was used to evaluate the system response to data transfer frequency, fine twisted pair wire length and buffering in the data path on the MTB. Some representative eye patterns are shown below.

Oscilloscope pictures with 2ns per division:

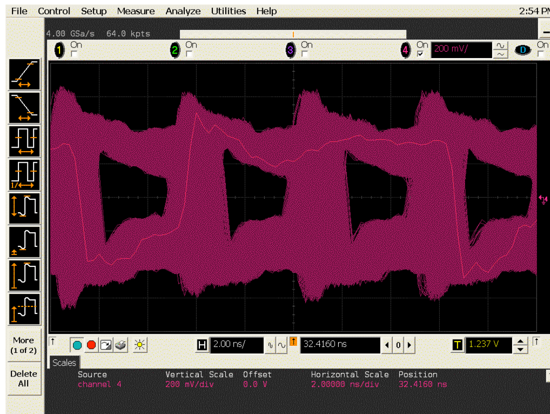
Buffered path 160 MHz 1.0 m cables



Un-buffered path 160 MHz 1.0 m cables



Buffered path 200 MHz 1.0 m cables



Un-buffered path 200 MHz 1.0 m cables

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