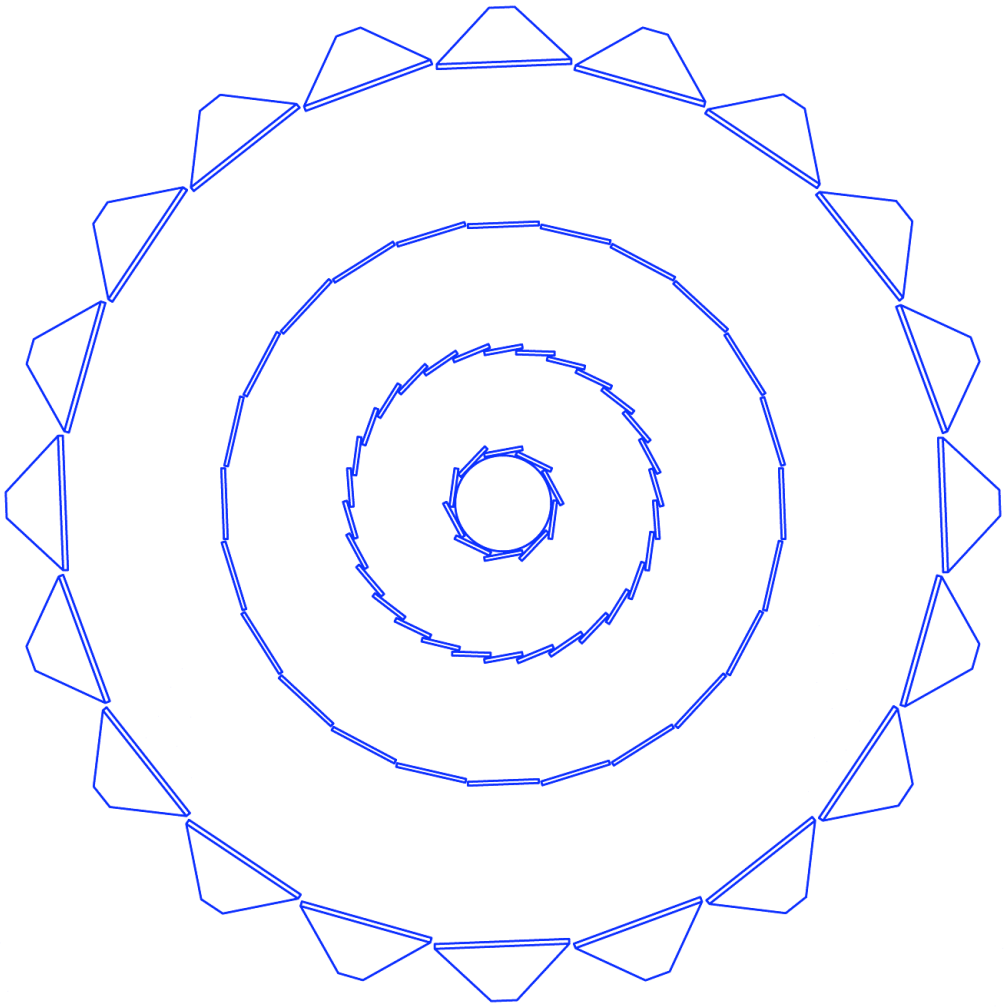
The STAR Heavy Flavor Tracker

Conceptual Design Report



Date: **November 4, 2009**

A Heavy Flavor Tracker for STAR

D. Beavis, R. Debbe, J.H. Lee, M.J. LeVine, R.A. Scheetz, F. Videbaek, Z. Xu
Brookhaven National Laboratory, Upton, NY 11973

J. Bielcik, M. Krus
Czech Technical University, 115 19 Prague, Czech Republic

L.E. Dunkelberger, H.Z. Huang, S. Sakai, G. Wang, C. Whitten Jr.
University of California, Los Angeles, CA 90095

J. Bouchet, J. Joseph, D. Keane, S. Margetis, V. Rykov, J. Vanfossen, W.M. Zhang
Kent State University, Kent, OH 43210

J. Kapitan, V. Kushpil, M. Sumbera
Nuclear Physics Institute AS CR, 250 68 Rez/Prague, Czech Republic

G.Visser
Indiana University Cyclotron Facility
Bloomington, IN 47408

J. Baudot, A. Brogna, G. Claus, R. De Masi, A. Dorkhov, G. Doziere, W. Dulinski, M. Goffe,
A. Himmi, C. Hu-Guo, F. Morel, A. Shabetai, M. Winter, I. Valin, G. Voutsinas
Institut Pluridisciplinaire Hubert Curien, Strasbourg, France

J. Bessuille, B. Buck, D. Hasell, J. Kelsey, R. Milner, R. Redwine, B. Surrow,
G. Van Nieuwenhuizen, S. Steadman
Laboratory for Nuclear Science
Massachusetts Institute of Technology, Cambridge, MA 02139

E. Anderssen, X. Dong, L. Greiner, F-X. Luo, H. Masui, H.S. Matis, H.G. Ritter, E. Sichtermann,
T. Stezelberger, X. Sun, M. Szelezniak, J.H. Thomas, C. Vu, H.H. Wieman, N. Xu, Y. Zhang
Lawrence Berkeley National Laboratory, Berkeley, CA 94720

A. Hirsch, X. Li, B. Srivastava, F. Wang, W. Xie
Purdue University, West Lafayette, IN 47907

S. Bouvier, B. Erazmus, A. Geromitsos, G. Guilloux, S. Kabana, C. Renard
SUBATECH – Ecole des Mines, Nantes, France

G.W. Hoffmann, J.J. Schambach
University of Texas, Austin, TX 78712

Table of Content

List of Figures

List of Tables

1. Introduction

The Heavy Flavor Tracker (HFT) is a state-of-the-art micro-vertex detector utilizing active pixel sensors and silicon strip technology. The HFT will significantly extend the physics reach of the STAR experiment for precision measurements of the yields and spectra of particles containing heavy quarks. This will be accomplished through topological identification of mesons and baryons containing charm quarks, such as D^o and Λ_c, by the reconstruction of their displaced decay vertices with a precision of approximately 50 μm in p+p, d+A, and A+A collisions. The combined measurements of directly identified charm hadrons and of the total non-photonic electrons will enable us to identify the bottom production at RHIC, including the bottom production cross section and R_{AA} and v_2 of the decay electrons.

The HFT consists of 4 layers of silicon detectors grouped into three subsystems with different technologies, guaranteeing increasing resolution when tracking from the TPC towards the vertex of the collision. The Silicon Strip Detector (SSD) is an existing detector in double-sided strip technology. It forms the outermost layer of the HFT. The Intermediate Silicon Tracker (IST), consisting of a layer of single-sided strip-pixel detectors, is located inside the SSD. Two layers of silicon pixel detector (PXL) are inside the IST. The pixel detectors have the resolution necessary for a precision measurement of the displaced vertex. With the HFT, the Time-of-Flight detector and the TPC we will study the physics of mid-rapidity charm and bottom production.

The pixel detector will use CMOS Active Pixel Sensors (APS), an innovative technology never used before in a collider experiment. The APS sensors are only 50 μm thick with the first layer at a distance of only 2.5 cm from the interaction point. This opens up a new realm of possibilities for physics measurements. In particular, a thin detector (0.37% of a radiation length per layer) in STAR makes it possible to do the direct topological reconstruction of open charm hadrons down to very low transverse momentum by the identification of the charged daughters of the hadronic decay.

2. Physics Motivation

The primary motivation for the HFT is to extend STAR's capability to study heavy flavor production by the measurement of displaced vertices and to do the direct topological identification of open charm hadrons. The yield and distribution of bottom hadrons will be estimated from charm production and non-photonic electron measurements but also via the impact parameter reconstruction of their decay electrons. Heavy quark measurements are a key component of the heavy ion program at RHIC as it moves from the discovery phase to the systematic characterization of the dense medium created in heavy ion collisions. The primary physics topics to be addressed by the HFT include heavy flavor energy loss, flow, and a test of partonic thermalization at RHIC. These measurements have been identified as necessary goals for the RHIC program in the Nuclear Physics Long Range Plan and in the RHIC mid-term scientific plan.

From a precise measurement of the spectra and the production ratios of charm hadron states, we will be able to extrapolate to the total yield for charm quark production. Furthermore, the open charm production rate is high enough at RHIC that the coalescence process becomes relevant for charmonium production. Knowledge of the total production cross-section for charm quarks is also essential as a baseline for J/ψ measurements. A meaningful answer to the question of J/ψ production at RHIC requires knowledge of the charm production cross-section in heavy ion reactions.

A unique advantage of STAR due to its full azimuthal coverage is the detailed studies of charm-charm correlations. In pQCD, heavy quarks are produced back-to-back at relatively large Q^2. The angular correlation will be modified in HI collisions due to the interactions between the heavy quarks and the medium. How much and how fast the changes of the heavy quark angular correlation depends on the nature of the medium. Therefore if we study the change of the D-D angular correlations we could extract the properties of the medium. Note that such study is more suitable for collisions at RHIC as the leading order dominates the production. At higher beam energies, such as LHC, the high-order contributions become more important, so the angular correlation analysis will be less obvious, more complicated. The effect of 'partonic wind' on charm quark correlations in high-energy nuclear collisions is studied in several theoretical papers[1] with D anti-D correlations as a sensitive probe for thermalization in high-energy nuclear collisions.

The observation of an enhancement in the ratio of baryon to meson production for particles containing light quarks was one of the interesting early observations in the RHIC program. This also was one of the supporting arguments for the quark coalescence model. With the HFT we will be able to measure the production rate for the Λ_c baryon. This will also allow us to study in detail the meson to baryon ratio for charm particles as a further test of the coalescence hypothesis. It will also help understand whether the Λ_c baryon is formed by a direct combination of a c quark with a ud di-quark (2-body process resulting in higher ratio values) or a 3-body combination.[2,3] The baryon to meson ratio is also important for the understanding of the flavor dependence of the energy loss mechanism.

The masses of charm and bottom quarks are about 1.25 GeV and 4.7 GeV, respectively, much higher than the predicted initial temperature of about 0.4 GeV for the matter produced in high-energy nuclear collisions at RHIC. Because are heavy, they are produced predominantly in the initial state and their intrinsic properties will not be affected by QCD interactions during the subsequent evolution. Therefore, heavy quarks can be used to probe the properties of the medium created in heavy ion collisions. The radiation of gluons is kinematically suppressed for heavy

flavor quarks passing through the medium: thus they should lose less energy than the light quarks. An important measurement to be made with the HFT is R_{CP}, the ratio of charm mesons and electrons from bottom decays produced in central Au+Au collisions to the binary-scaled production rate in peripheral Au+Au (R_{CP}) or minimum-bias p+p collisions (R_{AA}). Current measurements using non-photonic electrons as a measure of the abundance of charm and bottom hadrons indicate that the energy loss for heavy quarks is unexpectedly high and inconsistent with our current understanding of pQCD models. Based on the non-photonic electron data the theory of heavy quark energy loss is uncertain and may be completely wrong, especially with regards to bottom. The ability to separate and identify charm and bottom contributions is of crucial importance for such measurements. In this document we put emphasis on the charm sector because of the unique HFT capabilities in fully reconstructing the charm decays. From a physics point of view the bottom hadrons are equally important. It is important to point out that the bottom contribution can be determined only once the total charm contribution has been measured.

Another important study to be made with the HFT is a measurement of the elliptic flow of D-mesons down to very low p_T values. It is generally accepted that elliptic flow is established in the early partonic phase. If charm quarks, with a mass much larger than the temperature of the system, undergo elliptic flow then it has to arise from many collisions with the abundant light quarks. Thus, flow of charm quarks can be taken as a probe for frequent re-scatterings of light quarks and is an indication of thermalization that may be reached in the early stages of heavy ion collisions at RHIC. We believe that proof of thermalization constitutes the last step in the characterization of the strongly interacting matter created at RHIC. These important measurements require a very thin detector to push the measurement down to very low transverse momenta where elliptic flow is manifest.

Without the HFT upgrade the STAR experiment will not be able to execute the comprehensive heavy flavor program proposed here. However, STAR has been able to complete some initial charm measurements with the TPC alone, and with the data from the recent Run-7 STAR might be able to make limited progress towards an initial estimate for the B-meson contribution to the spectrum of the non-photonic electrons in Au+Au collisions.

The complete physics case for the HFT has been presented in the HFT proposal[4] and has been vetted in the HFT Science Review. In this Conceptual Design Report we will present the physics capabilities of the HFT in terms of low p_T charm, charm flow, charm suppression, as well as results obtained since the CD-0 review on Λ_C measurements, and the capability to study bottom production. The charm flow and charm suppression have been presented in detail already in the original proposal. Here we will present a brief summary of these two items and concentrate on the low p_T charm as well as Λ_C and B meson reconstruction capabilities.

2.1. Analysis Procedure

We start with a brief outline of our simulation procedures that are common to all results presented here. Details can be found in the HFT proposal.[4] The simulations presented here are performed (or updated) using an environment incorporating a simplified but up-to-date detector configuration (unless otherwise noted). Fast simulators have been used for PXL, IST, and SSD detectors, while a slow simulator has been used to simulate the TPC response. In all cases we use Au+Au events at 200 GeV.

We used 10 k central Hijing Au+Au events as the basic environment where particles under study (e.g. D^0, Λ_C and B mesons) are embedded in each event. These 'vanilla' events were also used to estimate the background. For D^0 production we made the conservative assumption of a charm

yield of dN/dY = 0.002 per binary collision, about half the cross-section measured by STAR.[5] The events were produced in the standard STAR geometry, simulation and tracking environment. A new beam pipe with a radius of 2 cm and a thickness of 0.0762 cm was used. The PXL pile-up hit density corresponds to the expected RHIC-II luminosity ($50*10^{26}$ $cm^{-2}s^{-1}$).[6] The beam diamond was assumed to be 0.01 cm in X-Y and a conservative 20 cm in Z with a Gaussian distribution. In the simulations we only generated events within ±5 cm from the detector center in Z direction in order to increase their usefulness. This constraint of the event vertex position is experimentally feasible at the L0 trigger level. Such a cut is absolutely necessary during data taking in order to ensure PXL hits for the decay products of heavy flavor. Minimum-bias event rates are not affected by this constraint, only high p_T electron triggered ("High Tower" trigger in the electromagnetic calorimeter) event rates are affected. For a realistic beam-diamond size of about 15 cm this will reduce the useful event rates by about a factor of two.

In order to study the effects of detector thickness, we simulated two cases. The "thin" configuration has a PXL thickness of 0.32% of a radiation length (X_0) and an IST thickness of 1.32% X_0. In this configuration the PXL thickness is slightly lower than that of the current design with 0.37% X_0. The "thick" configuration (PXL = 0.62% X_0 and IST = 2.32% X_0) explores the effect of roughly doubling the PXL and IST thicknesses. The "thick" detector is purely a hypothetical scenario, an extreme case used in these studies and it is a gross overestimate of any current alternative design.

2.2. D^0 Mesons

For the charm studies 5 D^0 were embedded in each Hijing event with 100% branching ratio (BR) decay to the channel $D^0 \rightarrow K^- + \pi^+$ (the measured BR is 3.83%). In order to have good statistics at high p_T, the embedded D^0 p_T was input as a flat distribution. At low p_T (< 3.5 GeV/c), a power-law distribution with input parameters of $\langle p_T \rangle$ = 1 GeV/c and n = 11 was used as the input D^0 distribution to reduce the statistical error of the efficiencies. The pseudo-rapidity distribution was generated flat in ±1 unit and also flat in azimuth. The daughter particles (K and π) were identified via selection of the square of the mass distribution (m^2) provided by the Barrel Time-of-Flight detector (TOF) with 100 ps timing resolution. A new geometry, a more realistic particle identification procedure and a more accurate background estimate are the main improvements since the CD-0 presentations.

The D^0 was reconstructed with the same topological cuts as those in CD-0 so that the results could be compared to each other. Figure 1 shows the topology of a D^0 decay and Table 1 gives the values of the specific cut-set used in reconstruction. This is an adequate set for these studies but it is not fine-tuned; studying the experimental distributions will do this. Additional TOF m^2 cuts were applied at low p_T (< 3 GeV/c) for K-π identification. Tracks with large m^2 were rejected as protons. At high p_T (> 3 GeV/c), K and π cannot be separated, so the only m^2 cut applied is for proton rejection. Effects of the K-π misidentification are included in the simulation.

Figure 2 shows two examples of expected invariant mass distributions at low (left panel) and high (right panel) transverse momentum values. Both plots are extrapolations to 500 M events based on the analysis of our 10 K event sample after proper scaling. Only statistical errors are shown. For the specific set of cuts one sees that the lower p_T distributions are high in combinatorial background mainly due to multiple scattering. The reconstruction to as low p_T values as possible will allow the precise determination of charm cross-sections using minimal extrapolation factors while integrating over p_T and the precise knowledge of spectra at intermediate and low p_T will allow for a precise determination of bottom contributions and flow measurements of both flavors.

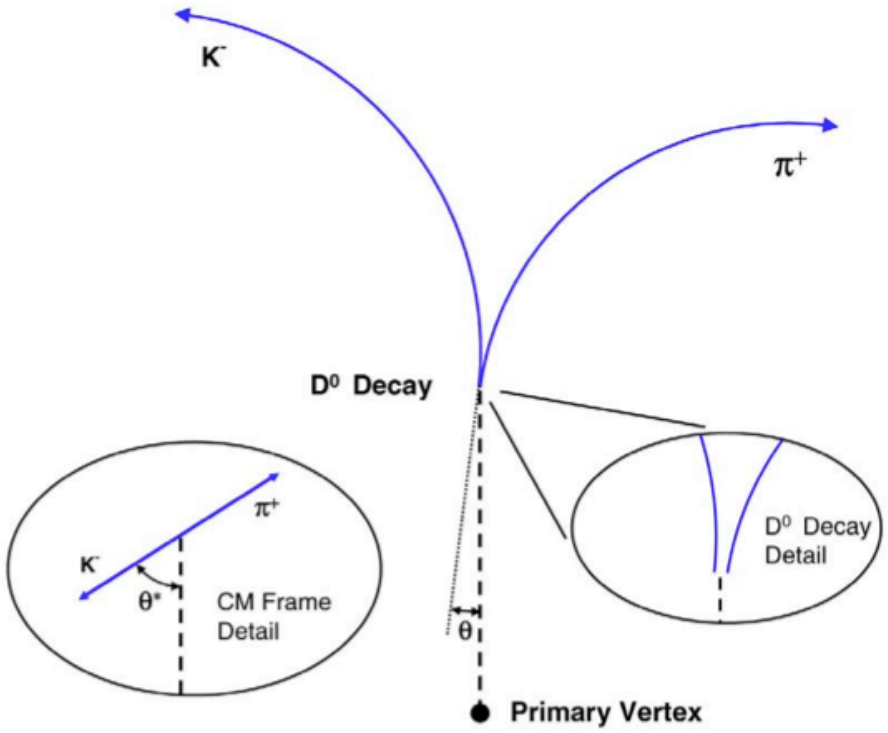


Figure 1: Topology of D^0 decay and cut variable definition.

Cuts	D^0
TPC hits	> 15
Pseudo-rapidity range	± 1.0
PIXEL hits	2
DCA (primary vertex)	≥ 50 μm
$DCA_{\pi K}$	≤ 50 μm
cos (θ)	≥ 0.98
Δm	≤ 35 MeV/c^2

Table 1: The set of cut values used for D^0 reconstruction.

The D^0 reconstruction efficiency in Au+Au central collisions is shown in Figure 3. The filled symbols represent the efficiencies extracted with power-law distributed embedded D^0, whereas the open circles are for an embedded flat D^0 p_T distribution. The triangles show the fraction of the decays where both daughter tracks were successfully reconstructed in the system. We also required that both tracks had two hits in the PXL detector. This represents the upper limit for signal reconstruction efficiency. The circles show the fraction of the reconstructed decays after our set of cuts has been applied to reduce background to acceptable levels. This latter curve depends strongly on the choice of cuts. Above 2 GeV/c the D^0 efficiency is of the order of 10% (remember that the branching ratio for this specific decay channel is not included in this number). Below 2 GeV the efficiency rapidly drops to 0.1% at about 500 MeV/c transverse momentum.

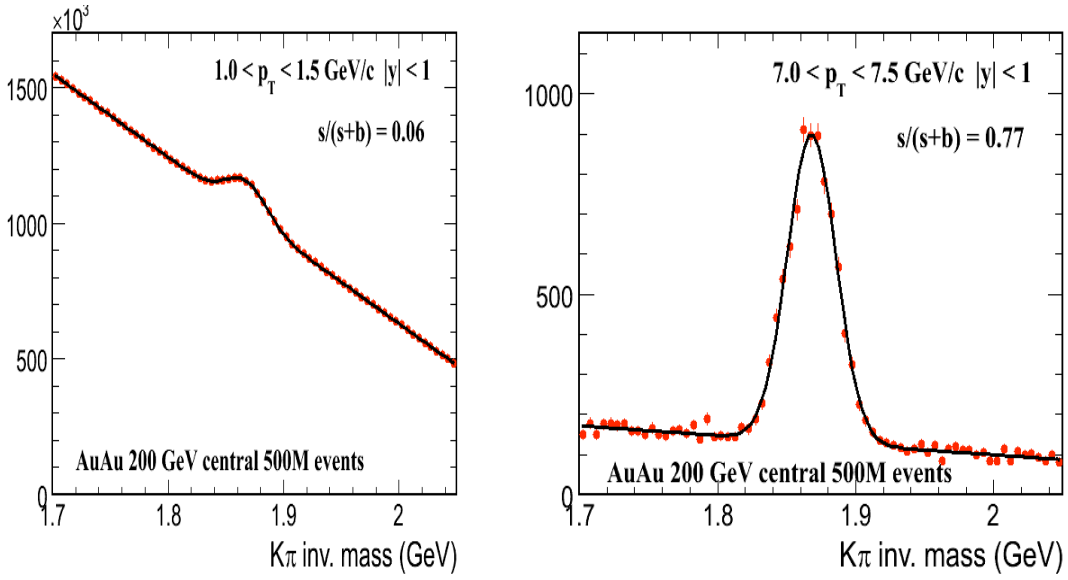


Figure 2: Estimated D^0 invariant mass distributions for two p_T intervals. The estimate was based on simulations with 10 K events and depends on the specific values of reconstruction cuts.

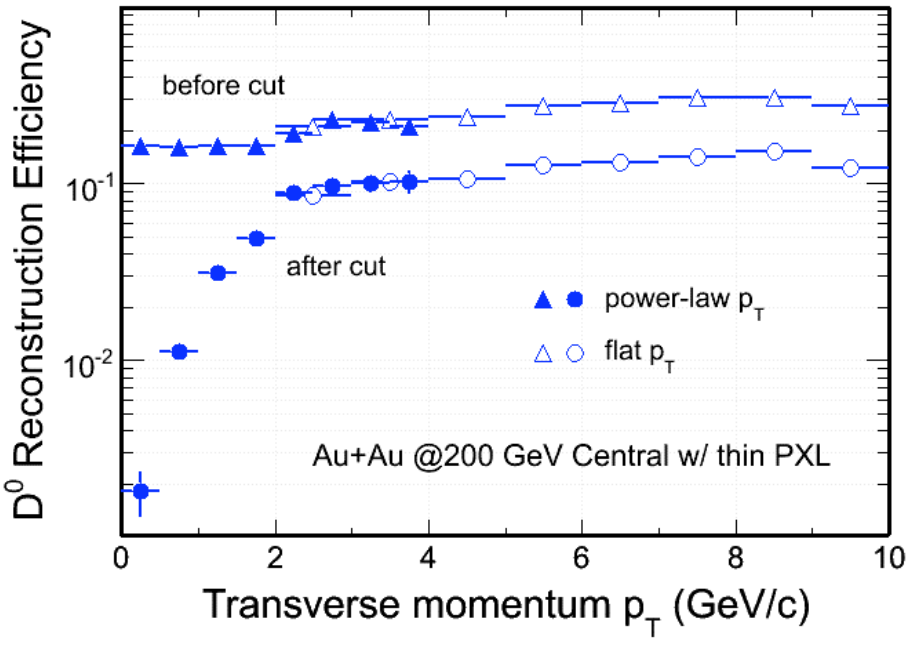


Figure 3: D^0 reconstruction efficiency as a function of p_T. Filled symbols are for a power law input distribution and open symbols are for a flat (in p_T) input distribution.

For the calculation of the signal significance the reconstructed D^0 signal was scaled to match the expected D^0 production yield times the branching ratio per central Au + Au collision. The distribution of the background was scaled to the expected background level by taking into account sources such as random combinations, particle misidentification and high p_T proton contamination. Due to small statistics and large fluctuations of the Hijing background at high p_T, we used an exponential function to extrapolate the background shape to empty bins at higher p_T.

The difference of the background shape while varying the cuts was used as a tool to estimate systematic uncertainties.

Figure 4 shows the signal significance distributions for the PXL with flat p_T (open circles) and with power-law p_T (filled circles). The systematic errors are estimated from the difference of the background shape by varying cuts. The power-law p_T distribution was used to more realistically simulate the statistical errors at low p_T. We see clearly the capability to measure D^0 as low p_T as 0.5 GeV/c, a value well below the expected mean p_T value of about 1 GeV/c. With the HFT we will be able to very accurately determine the total charm cross-section and spectra with minimal extrapolations. Since our simulation sample is limited (10K events), all error bars shown in the following figures are statistical only and based on the values shown in this figure. Background fluctuations could contribute another factor of up to about sqrt(2) but those cannot be adequately simulated in this small sample.

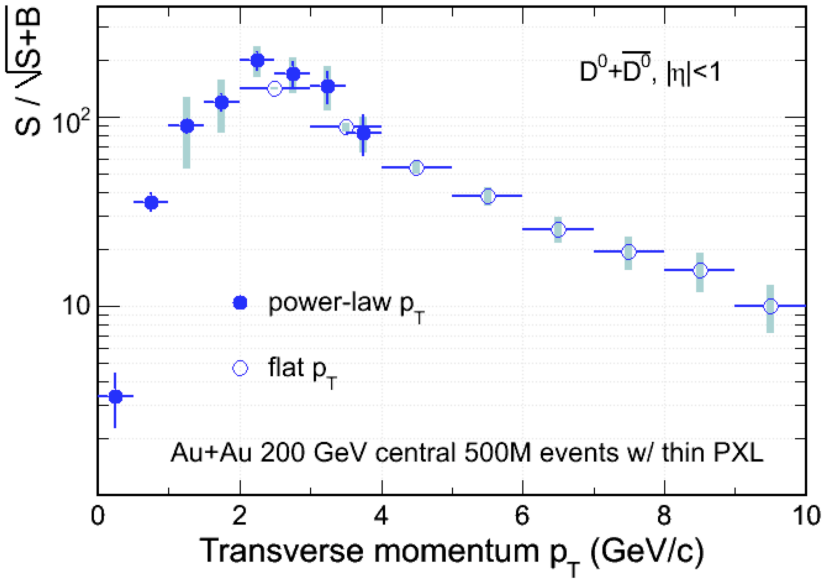


Figure 4: D^0 reconstruction significance as a function of p_T. Filled circles are for a power law distribution and open circles are for a flat distribution.

Figure 5 shows the anticipated D^0 p_T spectrum. Notice the broad range of p_T reach and the expected accuracy of the points. This sample is expected to be the result of a single year's run (about 6 months of RHIC running). We observe that we can achieve good signal significance for a wide range of transverse momentum values, starting almost at zero p_T (a realistic cut off value for an acceptable S/N ratio is around 300 MeV/c). Our simulation procedure is not yet optimized. For example all the cuts used so far are fixed pT cuts. Consequently, all our estimates represent lower limits for efficiencies. Initial studies suggest that by using pT dependent cuts, e.g. through the use of Support Vector Machines, gains in efficiency at low pT can be realized. In the following (unless otherwise noted) we use the thin PXL configuration as the default one.

2.3. Performance of Alternate Configurations

As part of our work addressing questions from the CD-0 Review we have addressed several hypothetical scenarios or risk factors. Two of those are presented here as supplementary material to document those results.

One risk factor refers to the case where either the IST or SSD sustains a catastrophic failure and are not available. Studies have shown that charm physics will not be possible with the existing tracking algorithms in the case where both detectors fail.

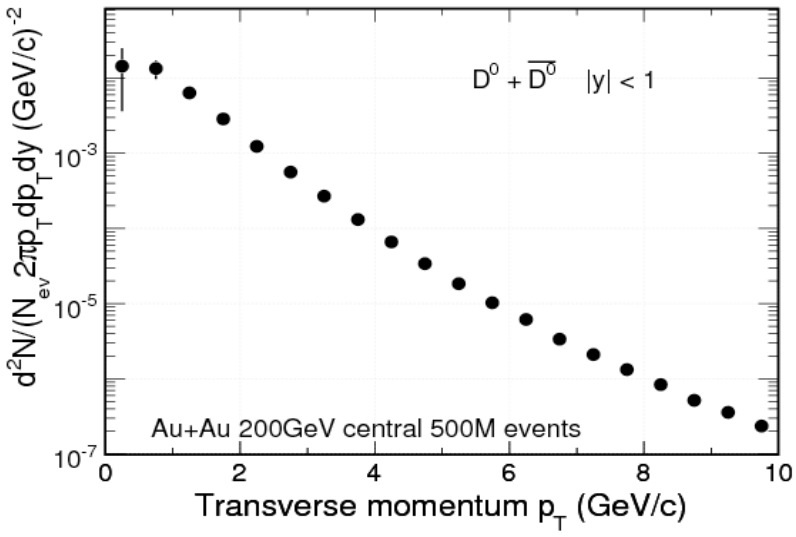


Figure 5: Estimated statistical accuracy for reconstructed D^0 spectra. Errors shown are statistical only.

The second scenario is rather technical and it has to do with the PXL layer thickness. In our studies we simulated two thickness scenarios that differ by a factor of two in order to get a feeling for the system performance as a function of layer thickness.

2.3.1. System Performance without SSD or IST

We performed simulations where either the entire SSD or the entire IST detector was not functional, i.e. the hit information was not available to the tracking packages. The impact on physics observables of this scenario comes exclusively through its modification of the overall system tracking efficiency, since the PXL layers primarily determine the pointing accuracy of HFT. The results are shown in Figure 6 (full simulation) as the single-track reconstruction efficiency for pions. The black points show the efficiency of the full system, the blue points the efficiency in the case of dead-IST and the red points the efficiency for dead-SSD.

As we analyze the results we should keep in mind that one of the design goals of HFT was to have built-in redundancy in tracking just for this case, i.e. the failure of a critical, intermediate tracking layer. The simulation shows that for the no-SSD case we suffer an average loss of efficiency of about 5-8% depending on p_T. For the no-IST case the number is similar, i.e. the detectors can act as a backup of each other. By squaring the absolute single track efficiency in the various cases, as obtained by the full simulations, we can estimate the expected loss of signal

(D^0) efficiency, which turns out to be about 5% on the average *absolute* efficiency loss or about 20% *relative* loss (from ~25% to ~20%).

On top of this efficiency loss we also expect a slight increase of the background levels, since any single track inefficiency results in an increased rate of ghost tracks. This level is expected to be minimal after the selection software cuts are applied. Full simulation studies showed that the level of ghost tracks (before cuts) increases by 0-10%, depending on p_T. Therefore the impact on the S/N is expected to be minimal. We conclude that the loss of an entire layer of the intermediate tracking system has a sizeable impact on the system performance but, until repairs are done, the key physics measurements could be carried out. As a final note on this subject let us remember that this failure analysis used the tracking software without any modifications. In real-life, tracking optimization techniques will be deployed in order to clean up and recover part of the lost efficiency; therefore what is presented here is a rather extreme, pessimistic scenario.

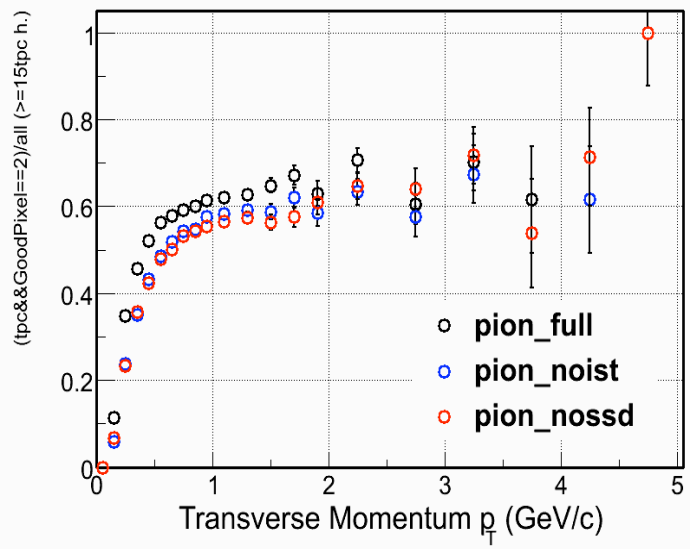


Figure 6: Single track reconstruction efficiency for the full HFT (black), the HFT without the IST (blue) and the HFT without the SSD (red) points.

2.3.2. System Performance for two PIXEL Thicknesses

Our original simulations were carried out using a radiation length of 0.28% for the first pixel layer and a radiation length of 0.14% for the beam pipe. Here we address the physics risk due to increases in the radiation length. The important parameter to be examined is the impact parameter of the pixel detector. The impact parameter resolution (accuracy of pointing to the vertex) can be expressed in the following form:

$$\sigma^2 = \frac{\sigma_1^2 r_2^2 + \sigma_2^2 r_1^2}{(r_2 - r_1)^2} + \frac{\theta_{mcs}^2 r_1^2}{\sin^2(\theta)}$$

where σ1 and σ2 are the position resolutions on each detector layer, r1 is the inner layer radius and r2 is the outer layer radius and θ_{mcs} is the multiple coulomb scattering angle in the first layer of the detector. θ is the angle of entrance into the detector relative to the

beam line. The second term, the projection error due to the multiple coulomb scattering, is the parameter of interest and it is this term that dominates the detector performance. The multiple coulomb scattering angle is given as:

$$\theta_{mcs} = \frac{13.6\,(MeV/c)}{\beta\ p}\sqrt{\frac{x}{X_0}}$$

where x/X0 is the fraction radiation length and represents the radiation length for both the inner pixel layer and the beam pipe. In this approximation the beam pipe is assumed to be at the same radius as the inner pixel detector layer. The original vertex projection resolution, which has been used for our simulations, is:

$$\sigma = 13\mu m \oplus \frac{22\ GeV}{p \cdot c}\mu m$$

As the design of the ladder has matured the radiation length of the ladder has increased from 0.28% to 0.37%. This increase is the result of adding another carbon composite backing layer plus additional adhesive. This was necessary to maintain sufficient position stability (position stability affects the first term of the pointing resolution expression). The current ladder design has been extensively analyzed for position stability, so further design changes should not be necessary in order to meet the stability requirements. The greatest risk to increased ladder radiation length is the aluminum-Kapton cable. We have a vendor that should be able to produce an aluminum-Kapton cable, but aluminum-Kapton has traditionally been difficult, so there is the risk that we might have to use copper in place of the aluminum. If this is required the radiation length of the ladder will increase from 0.37% to 0.51%.

There was also an increase in the beam pipe thickness. The only manufacturer, Brush Wellman, was originally comfortable building a 0.5 mm beryllium beam pipe, but they have subsequently argued that 0.75 mm would be much less risky and less expensive. The degradations in the impact parameter resolution resulting from these various changes are summarized in Table 2. The last entry in the table is for a copper ladder cable. This is the worst case and results in a pointing resolution that is 32% worse than the original design which was simulated.

Configuration	Beam pipe X_0	Ladder X_0	Impact parameter resolution, MCS term	% resolution degradation over original
original	0.14%	0.28%	22 GeV·μm/p·c	
current with aluminum	0.23%	0.37%	26 GeV·μm/p·c	19%
current with copper	0.23%	0.51%	29 GeV·μm/p·c	32%

Table 2: Summary of radiation length and impact parameter resolution. The original HFT PIXEL design is compared with the current ladder design and the worst-case example where the aluminum in the ladder cable is replaced with copper.

It should be noted that even with these increases the worst-case ladder radiation length is still less than 1/2 that of pixel detectors in ATLAS, ALICE or PHENIX.

Full system performance simulations (see Figure 7) show that increasing the radiation length of the first pixel layer from 0.32% to 0.62% reduces the significance factor by a factor of 2 in the p_t region around 0.5 GeV/c. Note this set of values are slightly different from the values discussed above (37% and 51%) but in the same general range.

The reduction in significance results in an increased data sample to achieve the same statistical uncertainly as specified in the following expression.

$$N = \frac{1}{U^2}\left(\frac{1}{s} + \frac{b}{s^2}\right)$$

N is the number of events required to achieve a signal measurement uncertainty U, s is the mean signal per event and b is the mean combinatoric background per event in the peak measuring window.

This mean that a factor of 4 increase in data is required for p_T less than 1.5 GeV/c to achieve the same statistical significance and to make up for the 30% increase in the radiation length of the first pixel layer. We can expect some improvement in this increase by optimizing the cuts. The proposal statistics is based on 500M events. It is plausible to collect twice that statistics in a 10 week Au+Au run. It might require additional computing resources over what is currently projected to be available, so careful planning and revisiting software will be called for. Design improvements in the ladder flexible cable are under study, which could result in fewer layers. This could restore the ladder radiation length to 0.3% while still using copper conductors.

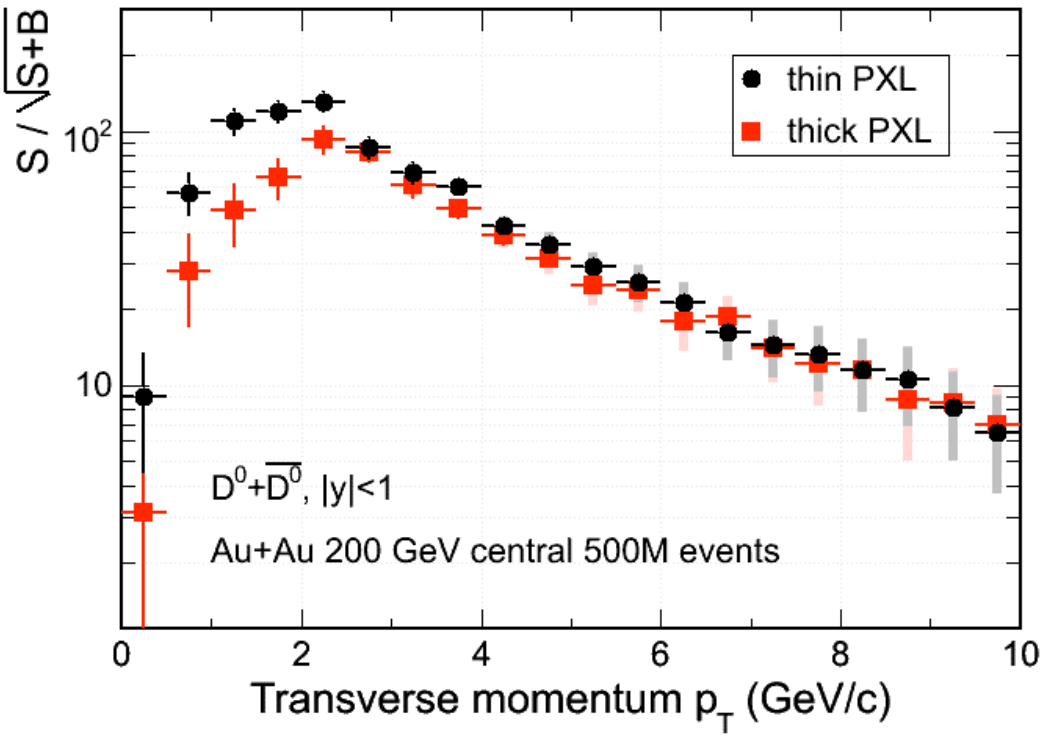


Figure 7: A measure of the significance factor from simulation for the PXL layer with a radiation length of 0.32% and 0.62%.

2.4. Charm Flow

At RHIC partonic collectivity has been well established via the measurements of hadrons containing light quarks (u, d, and s). Recent v_2 results from multi-strange hadrons, phi mesons and Omega baryons, further confirm this important discovery.[7] Charm quarks are abundantly produced at RHIC energies. Due to their high mass and small interaction cross-section, the strength of elliptic flow of heavy flavor hadrons may be a good indicator of thermalization occurring at the partonic level. If all quarks in heavy flavor hadrons flow with the same pattern as the quarks in the light flavor hadrons, this indicates frequent interactions between all quarks. Hence, thermalization of light quarks is likely to have been reached through partonic re-scattering.

Figure 8 shows what precision in flow measurement can be reached with 500 M minimum-bias events taken in STAR with the HFT. The red points show expectations from a transport model[8] for the case that the charm quark has the same size partonic flow as measured for the light quarks. The green points show the limiting case where the charm quark has zero partonic v_2. A measurement close to the red points would mean that frequent rescattering has induced collectivity for the heavy quark, while a measurement close to the green points would indicate little partonic rescattering and thus no thermalization. Our measurement is expected to fall between those limits. It is obvious that the HFT will allow for a precision measurement that will shed light on the question of thermalization.

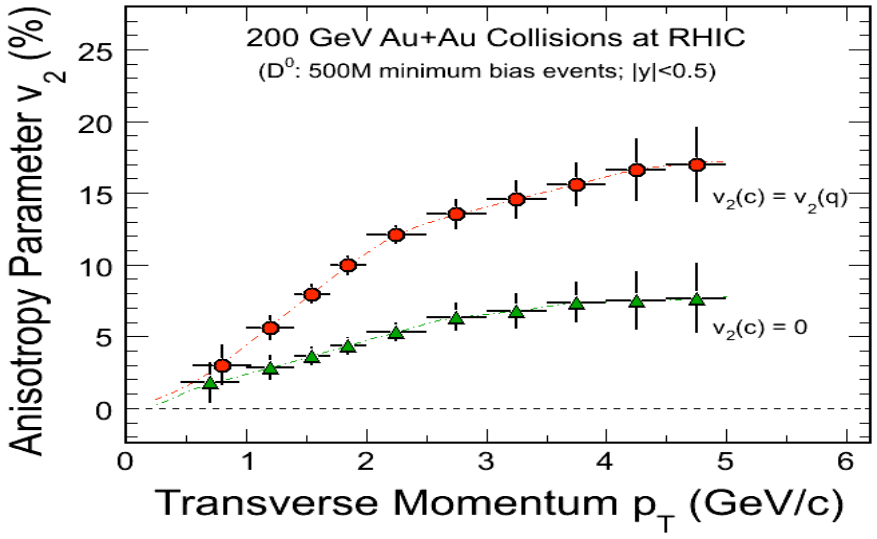


Figure 8: Precision projections of the v_2 measurement as a function of p_T for the case where charm flows the same way as light quarks (red) and for the case where charm does not flow (green).

2.5. Heavy Quark Energy Loss

The discovery of a factor of 5 suppression of high p_T hadrons ($5 < p_T < 10$ GeV/c) produced in Au+Au collisions at RHIC and the disappearance of the away-side jet has been interpreted as evidence for jet quenching.[9,10] This effect was predicted to occur due to radiative energy loss of high energy partons that propagate through a dense and strongly interacting medium.[11] The energy loss of heavy quarks is predicted to be significantly less compared to light quarks because

of a suppression of gluon radiation at angles $\Theta < M_Q/E$, where M_Q is the heavy quark mass and E is the heavy quark energy. This kinematic effect is known as the "dead cone" effect.[12] However, a recent measurement of the nuclear modification factor,[13] R_{AA}, for non-photonic electrons, the products of charm and bottom hadron decay, yielded the surprising result that heavy quarks may also be strongly suppressed in the medium. This clearly indicates that the energy loss mechanism is not yet understood. This fact has triggered new theoretical developments.[14,15] In order to make progress in understanding the nature of the energy loss mechanism, it is important to measure R_{AA} or R_{CP} for identified D mesons.

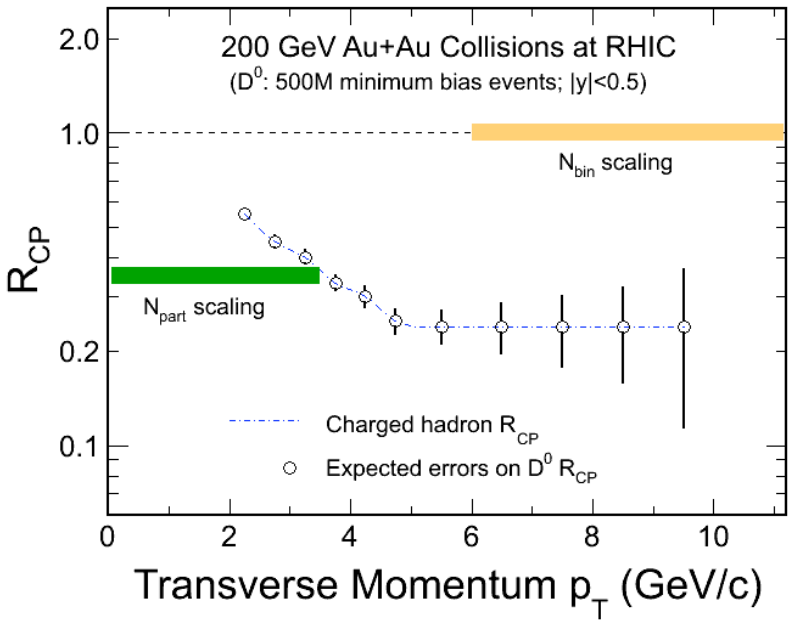


Figure 9: Expected errors for the R_{CP} measurement as a function of p_T.

Figure 9 shows the precision for R_{CP} that can be achieved with 500 M minimum-bias events in STAR with the HFT under the assumption that the suppression for heavy quarks is of the same size as the suppression for the light quarks. With the HFT STAR will be able to perform a precision measurement of R_{CP} of D mesons.

2.6. Λ_C-Baryons

In central Au+Au collisions at RHIC, a baryon to meson enhancement has been observed in the intermediate p_T region ($2 < p_T < 6$ GeV/c).[16,17] This is explained by a hadronization mechanism involving collective multi-parton coalescence rather than independent vacuum fragmentation.[18] The success of the coalescence approach implies deconfinement and the development of collectivity of the light quarks prior to hadronization.

Since Λ_c is the lightest charmed baryon and its mass is not far from that of the D^0 meson, a similar pattern of baryon to meson enhancement is expected in the charm sector.[19] Λ_C/D^0 enhancement is also believed to be a signature of a strongly coupled quark-gluon plasma.[20] Therefore it would be very interesting to measure R_{CP} of Λ_c baryons and compare it to R_{CP} of D^0 mesons. In addition, Λ_c/D^0 enhancement could be an explanation[21] for the large suppression of high-p_T electrons from

charm and bottom decays.[22] With the HFT STAR will be able to identify Λ_c baryons and to perform a measurement of R_{CP}.

2.6.1. Measurement Method

Λ_c baryons can be reconstructed through their hadronic p-K^--π^+ decay channel (BR 5.0 %), despite the very short decay length of $c\tau$ = 59.9 μm. Reconstruction of intermediate resonances through their respective decay channels will improve the Λ_c reconstruction, but it is not yet included in our simulations. By selecting only tracks with a large distance of closest approach to the event primary vertex, DCA, most of the background from primary tracks is rejected. This cut depends on the p_T of the Λ_C and ranges from 40 μm to 80 μm.

To select 3-track combinations coming from primary Λ_C decays, further topological cuts are used: a well-reconstructed Λ_C decay vertex (daughter tracks intersect within ~2 sigma) and a Λ_C momentum pointing back to the primary vertex. The final cut is on the three-particle invariant mass ($2.27 < m_{inv} < 2.30$ GeV/c^2).

2.6.2. Simulation Procedure

10K central Au+Au HIJING events have been used to estimate the combinatorial background. In order to enhance statistics at high p_T, 5 Λ_C with a flat p_T spectrum have been inserted into each event. The Λ_C were decayed through the p-K^--π^+ channel. The events were simulated with a vertex position of ± 5cm from the detector center.

In order to rescale the flat distribution, we assumed a power-law shape for the Λ_C spectrum with $\langle p_T \rangle$ = 1.0 GeV/c, and n = 11. The yield estimate (for no Λ_C/D^0 enhancement) assumed a Λ_C/D^0 ratio of 0.2.[19] A dN/dy = 0.002 per binary collision has been used as the expected D^0 yield.

To estimate the Λ_C signal and background in peripheral collisions, binary scaling, N_{bin}, with R_{CP} similar to that of charged hadrons[23] was assumed for the signal and $(N_{part})^3$ scaling for the background (3-particle combinations). For particle identification (PID) of daughter tracks, the STAR Time of Flight (TOF)[24] performance was assumed to separate pions from kaons for $p_T <$ 1.6 GeV/c and protons from pions and kaons for $p_T < 3.0$ GeV/c with 90% efficiency.

The Λ_C analysis relies on un-triggered data, as there is no obvious way to implement a trigger. Therefore, large datasets of minimum-bias and central events will be needed. With the recent implementation of DAQ1000 upgrade, the STAR data acquisition is able to reach a sustained DAQ rate of over 500 events per second. With this rate and an estimated 40% accelerator and detector duty factor, about 500 M events will be recorded per month. In order to accumulate 500 M central events and 500 M peripheral (60-80%) events, we will record 250 M central events and 2 B minimum-bias events of which we use the 250 M most central events and 500 M peripheral events. This will take a run of more than 4 months in length and makes the Λ_C measurement a goal for the second or third year of HFT detector operation.

2.6.3. Results

Figure 10 shows that a secondary decay vertex displaced by $c\tau$ = 59.9 μm can be separated from the event primary vertex. Note, that this corresponds to a mean decay length of a Λ_C at mid-rapidity with a transverse momentum of about the Λ_C mass, where the $\beta\gamma$ factor is equal to one.

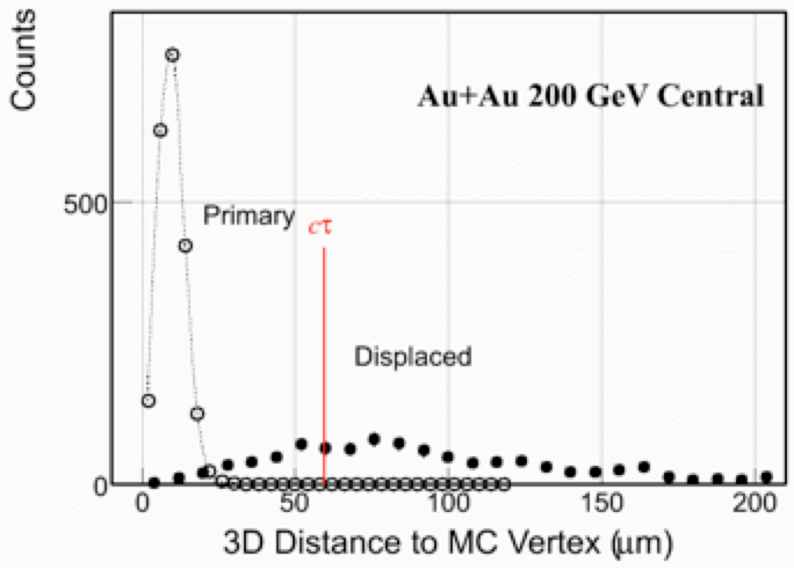


Figure 10: Open circles show the primary vertex resolution in central Au+Au collisions. Solid circles show the Λ_C decay vertex resolution. The mean decay distance, $c\tau$ = 59.9 μm, for the Λ_C is shown to guide the eye. Each decay length was scaled by the appropriate $c\tau$ factor to provide a universal peak for the purpose of illustration.

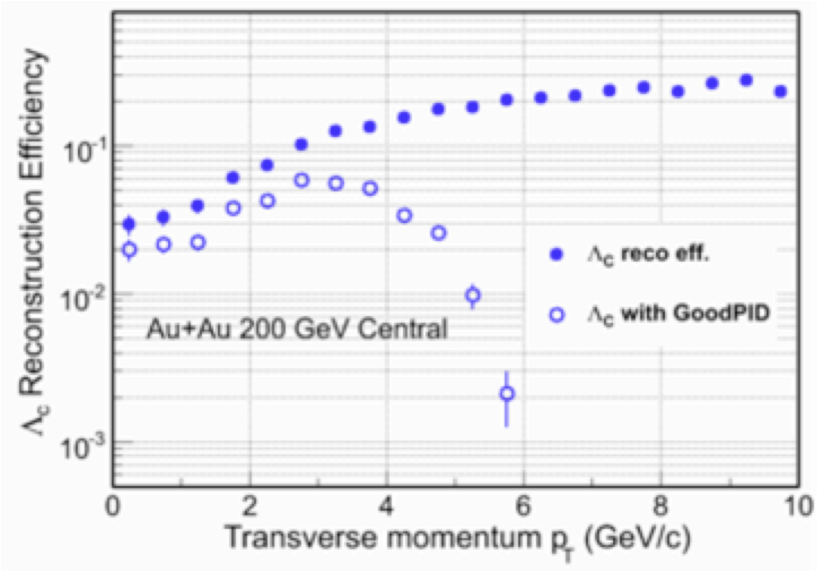


Figure 11: Acceptance and efficiency for Λ_C reconstruction.

Figure 11 shows the combined acceptance and tracking efficiency for Λ_C (filled circles) in the pseudorapidity interval $|\eta| < 1$. For this plot, that represents an upper limit in signal recovery, we required (for purity purposes) the daughter tracks to have good hits (not pile-up hits) in the PXL

detector. In real life one applies a set of cuts to reduce the background levels to acceptable values typically at the expense of reduced signal efficiency. Those cuts also suppress ghost tracks (ghosting in HFT is a strong function in p_T and it is at < 10% level for tracks with p_T above 1 GeV/c, before cuts).

Since the ΛC decays into three daughter particles, its reconstruction efficiency is lower than that of the D0. Estimates of the combinatorial background due to particle misidentification at high p_T for this three-body decay is complicated. In this study we require full identification for all daughter particles, which imposes an upper p_T limit for decay particles. This effective p_T acceptance cut causes the decrease in Λc efficiency at high p_T in Figure 11 (open circles).

A topological cut optimization procedure was performed for both central (0-10%) and peripheral (60-80%) collisions, to maximize the signal significance, $S/\sqrt{(S+B)}$. The results are shown in Table 3 and in Table 4.

p_T [GeV/c]	$S/\sqrt{(S+B)}$	S/(S+B)	Λ_C produced	Λ_C observed
2-3	4.4	0.03	23M	632
3-4	4.3	0.12	7.3M	149
4-5	8.7	0.77	2.4M	98

Table 3: Signal significance, purity and number of produced and reconstructed Λ_C in 500 M central Au+Au collisions (for no Λ_C/D^0 enhancement). Decay branching ratio, acceptance, efficiency and topological cuts are taken into account.

p_T [GeV/c]	$S/\sqrt{(S+B)}$	S/(S+B)	Λ_C produced	Λ_C observed
2-3	4.6	0.66	940k	32
3-4	5.5	0.82	410k	37
4-5	4.4	0.55	180k	35

Table 4: Same as Table 3, for 500 M peripheral Au+Au collisions.

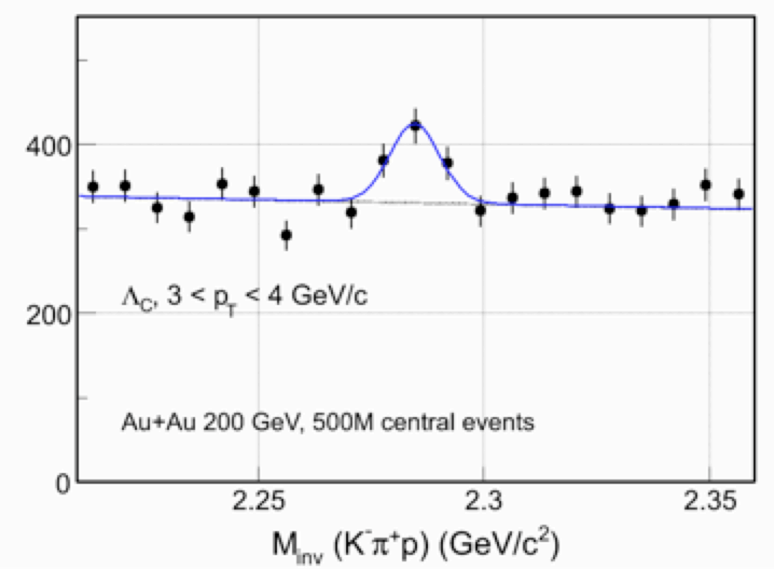


Figure 12: Simulated invariant mass peak and expected levels of signal and background for p_T 3-4 GeV/c, in 500 M central Au+Au collisions, assuming no Λ_C enhancement.

The estimated invariant mass peak for a 3-4 GeV/c p_T bin is shown in Figure 12. A three-sigma signal could not be achieved for $p_T < 2$ GeV/c with this data sample. However, for $p_T > 5$ GeV/c, a good significance could be achieved without requiring daughter track PID information.

Figure 13 shows the estimated statistical errors for the Λ_C/D^0 ratio, for the case where there is no baryon enhancement, i.e. that the ratio is equal to 0.2 and flat in p_T, in black and for the case of the same enhancement as for Λ/K^0_S in red. Given the D^0 yield and $c\tau$, the errors coming from its measurement are negligible.

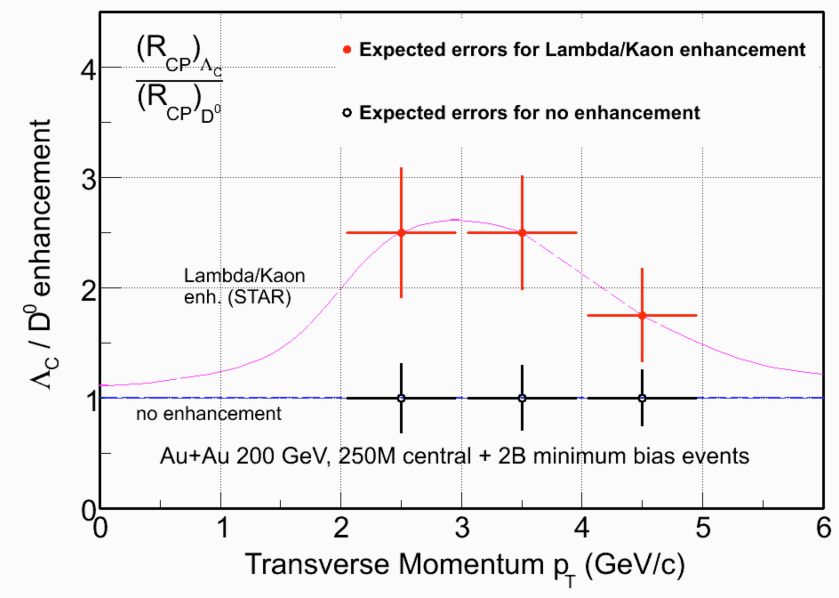


Figure 13: Statistical errors of the Λ_C/D^0 ratio for the case of no enhancement and of Λ/K^0_S-like enhancement.

2.6.4. Summary

The feasibility of Λ_C reconstruction with the HFT has been shown using a Monte Carlo simulation with STAR reconstruction and tracking software. The measurement of the Λ_C/D^0 ratio will allow us to determine if the baryon enhancement seen in the light quark sector will extend to heavy quark hadrons. We expect to improve the significance of this measurement through improved analysis techniques and through extending the analysis to resonant intermediate states and improving the reconstruction efficiency at low p_T.

2.7. B Mesons

Due to their large mass the bottom and charm quarks are expected to behave differently from the light quarks in a QGP. As already argued in Section 2.5, it is very important to directly identify bottom and charm mesons. At low transverse momentum the charm contribution is dominant in the electron spectrum. At a p_T of about 5 GeV/c PYTHIA[25] predicts both contributions to be equal while at higher p_T bottom production is dominant. Independent measurements of bottom quark production are essential to disentangle different heavy meson production mechanisms and provide crucial information on medium properties. Also, measurements of bottom mesons are

important to clarifying the J/ψ production mechanism in the medium. Apart from the primordial production, a significant fraction of J/ψ comes from B meson decay. Measurements on B meson production will allow us to subtract the contribution from the B-decay to J/ψ production.

With the current detector configuration (TPC and BEMC), the B contribution to the non-photonic electron spectrum (NPE) was estimated[26] to be about 50% at p_T > 5 GeV/c with large uncertainties. With the HFT, the measurements will dramatically improve. With RHIC-II luminosity B mesons will be measured using different approaches, the 'D-subtraction' method from the NPE spectrum and semi-reconstruction of B-decays into either an electron (B -> e + X) (e.g. non-primary, non-photonic electrons) or into a J/ψ, which is then reconstructed via the semi-leptonic or other decay channels. From these three methods the best result will be obtained using the 'reconstruction' of the semi-leptonic B-decays and the D-subtraction method. The J/ψ method is still under development. It has the potential of becoming a powerful tool if a trigger can be implemented to enhance event rates since the product of two very small branching ratios greatly suppresses the useful rates. Nevertheless, in the following we briefly discuss this as well as the other methods. It is important to realize at this point that the HFT exceeds the required pointing capabilities for B meson reconstruction ($c\tau \sim 490$ μm). It is only the low production rates, relative to possible background sources, that make this measurement a challenging one. This, in turn, makes the possibility of a B trigger an important tool in enhancing the purity of the event sample.

2.7.1. Measurement of B Using the 'D-Subtraction Method'

This method is a straightforward extension of the non-photonic electron spectrum (NPE) currently used by both PHENIX and STAR to obtain rough estimates of heavy flavor production. The precise determination of the D meson spectra by the HFT will allow for an accurate estimate of the charm contributions to the total NPE spectra thus allowing for a direct estimate of bottom production. Since the NPE technique is very mature right now there is no need to further elaborate on this application.

2.7.2. Measurement through B → J/ψ + X Decays

As already discussed, this method has limited applicability for now. We will briefly outline its main components because we believe it holds great potential and we will pursue it and develop it further. The main idea is that a B meson can also be identified through its decay into J/ψ. Here we explore the method developed by CDF[27] to calculate the pseudo-cτ of J/ψ and apply a cut to distinguish direct J/ψ from J/ψ from B decay. Figure 14 illustrates how the relevant variables are defined. The pseudo-cτ is defined as $c\tau' = \vec{L} \cdot \frac{p_T^{\psi}}{|p_T^{\psi}|} \cdot \frac{M_{\psi}}{|p_T^{\psi}|}$, where $\vec{L}$ is the path length between the J/ψ production point and the collision vertex, M_{ψ} is the J/ψ mass and p_T^{ψ} is the J/ψ p_T which is required to be larger than 1.25 GeV/c. We define DCA as the distance of closest approach between paired electrons. The pseudo-cτ is less than 15% smaller[28] than the actual B meson cτ. In this analysis, the only physical background considered is direct J/ψ production including feed-down contributions from higher mass charmonium states. Charm continuum and Drell-Yan might have similar levels of contributions. The background due to the random combination of electron pairs is removed via subtracting the same sign electron pairs when analyzing mass and

pseudo-cτ distributions. The signal is a mixture of $B^{\pm}$ and B^{0} mesons with a 1.094% branching ratio for the decay to J/ψ.[29]

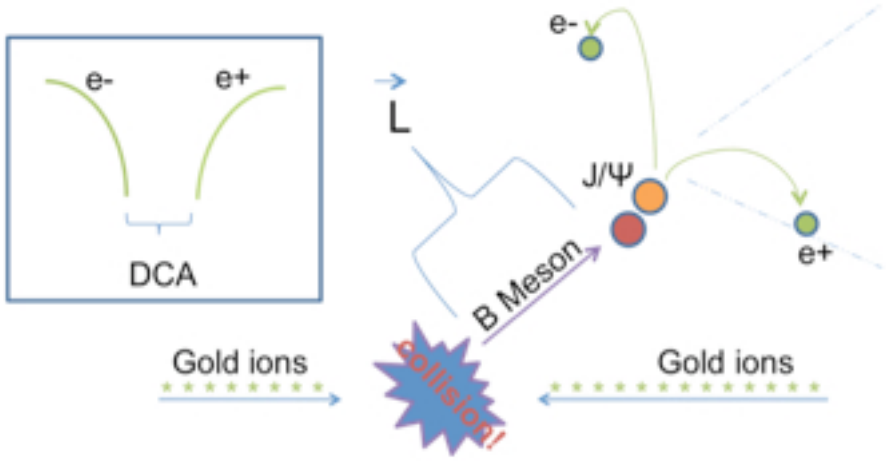


Figure 14: Definition of variables used in the analysis.

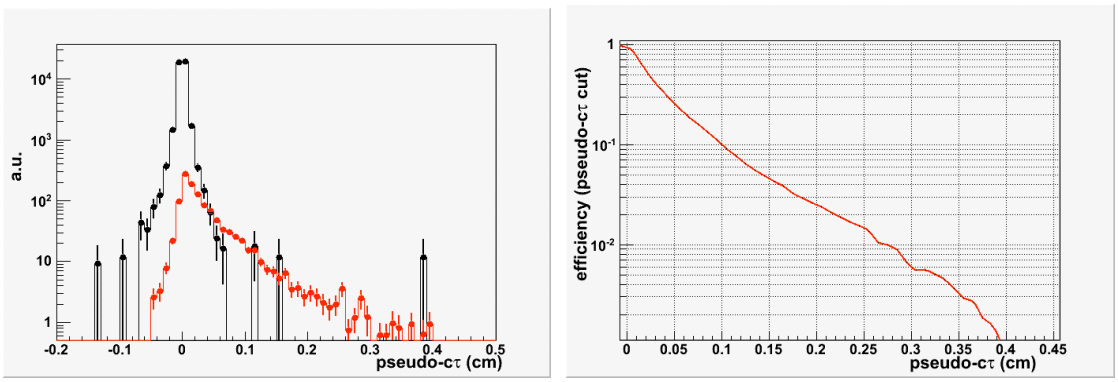


Figure 15: Left panel: pseudo-cτ distributions for direct and B-decay J/ψ in central Au+Au collisions after including PXL detector pile-up effects. The black and red histograms are from direct and B-decay J/ψ, respectively. The right panel shows the efficiency under different pseudo-cτ cuts for B-decay J/ψ.

Figure 15 shows the pseudo-cτ distribution for B-decay and direct J/ψ in most central Au+Au collisions and the efficiency with different pseudo-cτ cuts assuming PXL pile-up effects at RHIC-II luminosity. We used the normalization from 200 GeV p+p collisions. The FONLL calculation predicts the total $b\bar{b}$ cross-section in p+p collisions at RHIC to be 1.87 μb leading to 3.74 μb for B meson production. Measurements from PHENIX p+p collisions[30] show that the total direct J/ψ → e^{+} + e^{-} production is about 178 nb. Taking into account the B → J/ψ → e^{+} + e^{-} branching ratio, we obtained a yield ratio of direct J/ψ over B-decay J/ψ of 65. With a pseudo-cτ cut at 700 μm, about 20% of the B-decay J/ψ survive the cut. Almost all of the direct J/ψ are rejected while a few have a large pseudo-cτ. In the following estimate, we assume a 100% rejection of direct J/ψ.

The total number of B → J/ψ → $e^+ + e^-$ events recorded at |Zvtx| < 5 cm during a RHIC-II 12-week run is:

- In p+p collisions
  - Maximum: 1698 ± 41 J/ψ at $p_T \geq 1.25$ GeV/c.
  - Minimum: 374 ± 19 J/ψ at $p_T \geq 1.25$ GeV/c.
- In Au+Au collisions
  - Maximum: 2734 ± 52 J/ψ at $p_T \geq 1.25$ GeV/c
  - Minimum: 512 ± 23 J/ψ at $p_T \geq 1.25$ GeV/c.

Here we assume 100% trigger efficiency and that the combinatorials have the same pseudo-cτ distribution as the direct J/ψ. We also assume that the pseudo-cτ cut rejects all background and we neglect TPC pile-up effects. However, the L0 J/ψ trigger performance in STAR will need to be improved to efficiently trigger on low p_T J/ψ. The total L0 trigger rate for firing the TPC gated grid is limited to 750 Hz.[31] We can assume that 100Hz can be assigned to the B → J/ψ analysis.

In Au+Au collision, the maximum collisions rate is 32 kHz. This requires a rejection factor of 64 to fit into the bandwidth after including the factor of 5 with |Zvtx| < 5cm cut. The J/ψ L0 topology trigger[32] can provide a rejection of ~10 with a J/ψ efficiency of 20%. That means the maximum number of B → J/ψ in one RHIC year is about 85.

In p+p collision, the maximum rate is 2 MHz and it requires a rejection of 4000 to fit into the bandwidth after including the factor of 5 with |Zvtx| < 5 cm cut. The J/ψ L0 topology trigger can provide a rejection of ~1000 with a J/ψ efficiency of 36%. This means the maximum number of B → J/ψ in one RHIC year is about 153. These limited rates make it necessary for either a different approach in background rejection (that will preserve much more signal) and/or the development of an efficient (high-level) trigger. With the new TOF detector installed it is possible to correlate TOF and BEMC at L0 with a granularity of 240x300.[33] This is expected to enhance the trigger performance. We will be able to study this trigger using the data from Run-9 and revisit this otherwise very promising technique.

2.7.3. Measurement through B Semi-leptonic Decays

In this section we explore the possibility of identifying the B-meson through its semi-leptonic decay B → e + X by exploring the large impact parameter of the decay electrons. D mesons also have such a decay channel. This is the dominant source of 'background' electrons. One has the choice of either subtracting this D contribution from the total signal or trying to separate the signal by exploring the difference of a factor of four in lifetime. For the latter approach we utilize the impact parameter (DCA) method used by the ALICE collaboration[34] to separate electrons of B decays from those from D decays. Since B mesons have mean proper decay lengths of about 500 μm, their decay electrons are characterized by large impact parameters with respect to the interaction vertex. With the two pixel layers DCA will be measured with a resolution of $\sigma_{d0} \sim 20$ μm for $p_T \geq 2$ GeV/c. A cut imposing a minimum value of DCA rejects a large fraction of the electrons from light meson decays and photon conversions, as well as primary pions misidentified as electrons. For central Au+Au collisions the reconstructed event vertex resolution is about 3 μm in the R-ϕ and Z coordinates, which provides the precision to distinguish the distance of closest approach to the primary vertex (DCA) of the electrons from D and B semi-leptonic decays due to their different cτ, shown in Figure 16.

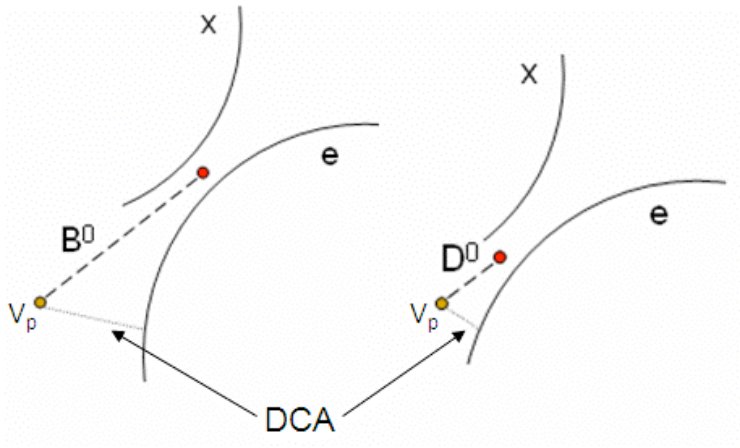


Figure 16: The difference of the DCA of daughter electrons from D^0 and B^0 semi-leptonic decays.

We used 10 K HIJING central (b < 3 fm) Au+Au events with the vertex Z (beam) coordinate between -5 and 5 cm for the best utilization of the pixel layers as discussed earlier. These events were enriched with B mesons decaying into the channel under study. The embedded events then went through the standard STAR data reconstruction. One hundred test particles, D^0, D^+, B^0, B^+, were embedded flat in p_T (0.2-20 GeV/c) in each event. The pseudo-rapidity is flat in ±1 units around mid-rapidity and flat in azimuth. The p_T spectra were weighted using the STAR measured D^0 spectrum for D mesons and FONLL calculations for B mesons. D^0 and D^+ were forced to decay semi-leptonically (D^0, $D^+ \rightarrow e + X$) with 100% branching ratio. Since B^0 and B^+ are very similar in this simulation, we will use B to represent both of them. B mesons decay to 75% into the semi-leptonic channel $B \rightarrow e + D^* + X$ and to 25% into the semi-leptonic channel $B \rightarrow e + D + X$. The fraction of the process $B \rightarrow D^* \rightarrow D \rightarrow e$ is relatively small. We only simulate $B \rightarrow e + X$ and $B \rightarrow D \rightarrow e$. These channels are later scaled by the fragmentation ratio (FR) and branching ratio (BR) in the final analysis. Table 5 lists the $c\tau$, mass, FR and BR for these particles.

Particles	$c\tau$ (μm)	Mass (GeV/c^2)	$q(c,b) \rightarrow X$ FR	$X \rightarrow e$ BR
D^0	123	1.865	0.54	0.0671
D^+	312	1.869	0.21	0.172
B^0	459	5.279	0.40	0.104
B^+	491	5.279	0.40	0.109

Table 5: D and B meson parameters.

Due to larger $c\tau$, the DCA distribution of B electrons is expected to be broader than that of $D^0 \rightarrow e$. Since D^+ $c\tau$ is closer to that of B mesons, it becomes a challenge to distinguish them by electron DCA distributions only. However, the D^+ reconstruction via hadronic decay (e.g. $D^+ \rightarrow K + \pi + \pi$) can provide a precise constraint on p_T distributions of the decay electrons. Thus together with the electron DCA distributions, we will be able to separate D and B meson production with the HFT.

The HFT also has good electron reconstruction efficiency, which is about 60% independent of pT and it includes the TPC's overall 85% tracking efficiency. For particle identification we used the

TOF detector for low p_T and the BEMC for high p_T and realistic TPC dE/dx. Good electron candidates were selected with number of total fit points > 15, pseudo-rapidity in ±1, and with two pixel hits required on the track. All electrons from photon conversions outside of the pixel detector can be removed with this requirement. The main background sources in this analysis are electrons from photon conversions in the beam pipe or the first pixel layer and electrons from π^0 and η Dalitz decays. The background from other hadron decays overall is small and negligible at high p_T. We assume that the background p_T is decreasing exponentially and use this to extrapolate to empty bins at high p_T. To estimate the background, we embedded 50 π^0s with flat p_T distribution in each Hijing Au+Au central event and with the same branching ratio of 50% for conversions and Dalitz decays. The p_T distributions in the analysis were weighted by the PHENIX π^0 spectrum. All the electrons from photon conversions outside of the pixel detector can be rejected with two pixel hits required on the track. The leftover electrons from photon conversions in the beam pipe and part of the first PXL layer are coming from about 0.3% X_0. The radiation length of π^0 Dalitz is about 0.77% X_0. The η Dalitz is about 20% of π^0 Dalitz decays assuming no p_T dependence. From the photonic to inclusive electron ratio measured in STAR during Run-4, the background of photon conversion and Dalitz can be scaled to the material corresponding to the level in future runs. The DCA distributions of the background in two p_T bins are shown as the dot-dashed curves in Figure 17, and the p_T distributions of the background are shown as curves in Figure 18.

The electron DCA distributions from different decay processes were normalized by the corresponding FR and BR, and the total electron yield was normalized to STAR measured non-photonic electron (NPE) spectrum. The (B→e) / NPE ratio was normalized to fit STAR measured data (from e-h correlation). Figure 17 shows the electron DCA distributions at $2.4 < p_T < 3$ GeV/c (top panel) and at $4.8 < p_T < 5.4$ GeV/c (bottom panel) for $D^0 \rightarrow e$ (red), $D^+ \rightarrow e$ (green), $B \rightarrow e$ (blue) and $B \rightarrow D \rightarrow e$ (purple). The dot-dashed curves are from background DCA distributions. The black solid curve presents the total electron DCA distribution, which was normalized to the STAR measured NPE spectrum.

With data we will use the different DCA distributions to fit the total DCA distribution to extract the raw yield of each source of electrons statistically. The D meson p_T distributions from our measurements via hadronic decay channel will constrain the $D \rightarrow e$ distribution. By subtracting the $D \rightarrow e$ DCA distribution in each p_T bin from the total DCA distribution, the electrons from B meson decays can be obtained.

From the DCA distributions and the efficiency, the $D \rightarrow e$, $B \rightarrow e$ and $B \rightarrow D \rightarrow e$ spectra can be obtained. The statistical errors were estimated for 50 M central Au+Au events (no special trigger), shown in Figure 18.

Figure 19 shows the ratio of the number of electrons from bottom decay to the number of electrons from charm and bottom decay as a function of p_T. For low p_T the ratio and the expected errors are calculated from 50 M Au+Au central events (open circles). For the high p_T region we used a "high tower (HT) in EM calorimeter" trigger sampling 500 μb^{-1} luminosity (filled circles). For an estimate of the HT luminosity of 500 μb^{-1} we used the following formula: 50kHz/500Hz*0.5*0.2*500M/10 per barn. Here 50 kHz is the expected maximum collision rate, 500 Hz is the rate for Au+Au minimum-bias, the effective luminosity is assumed to be half of the total plus a reduction factor of 5 from cutting on event vertex Z-position, $|V_Z| < 5$cm. Assuming 500 M Au+Au minimum-bias events accumulated a factor of 10 is the fraction of central 0-10%. The final statistical errors are including the effect of HT trigger efficiency as a function of p_T, which is experimentally estimated from our Run-8 HT trigger efficiency. The blue lines represent

the band of uncertainty of FONLL calculations.[35] Open stars show preliminary results for 200 GeV p+p collisions.[36]

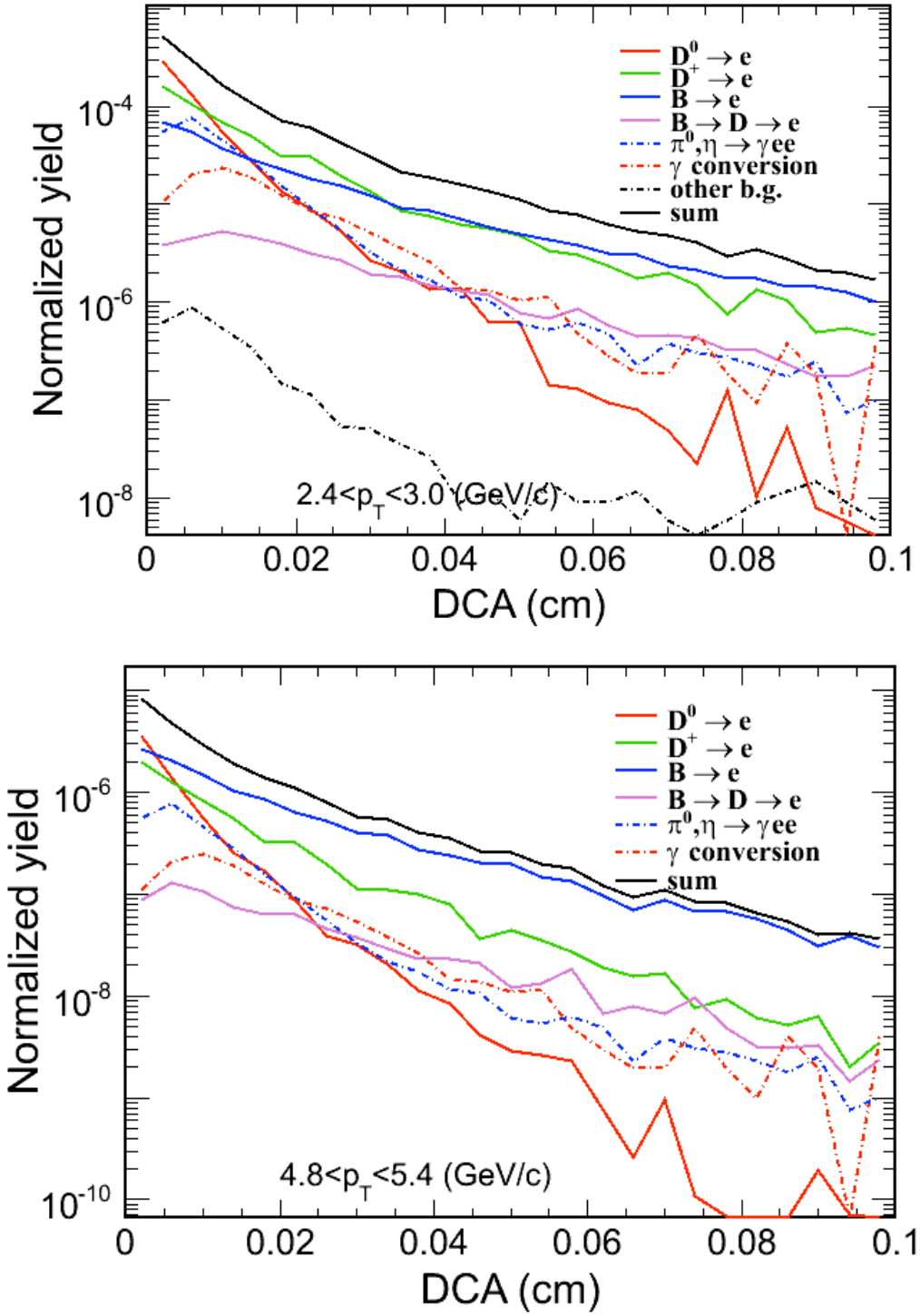


Figure 17: The electron DCA distributions for D and B meson semi-leptonic decay for two different p_T regions.

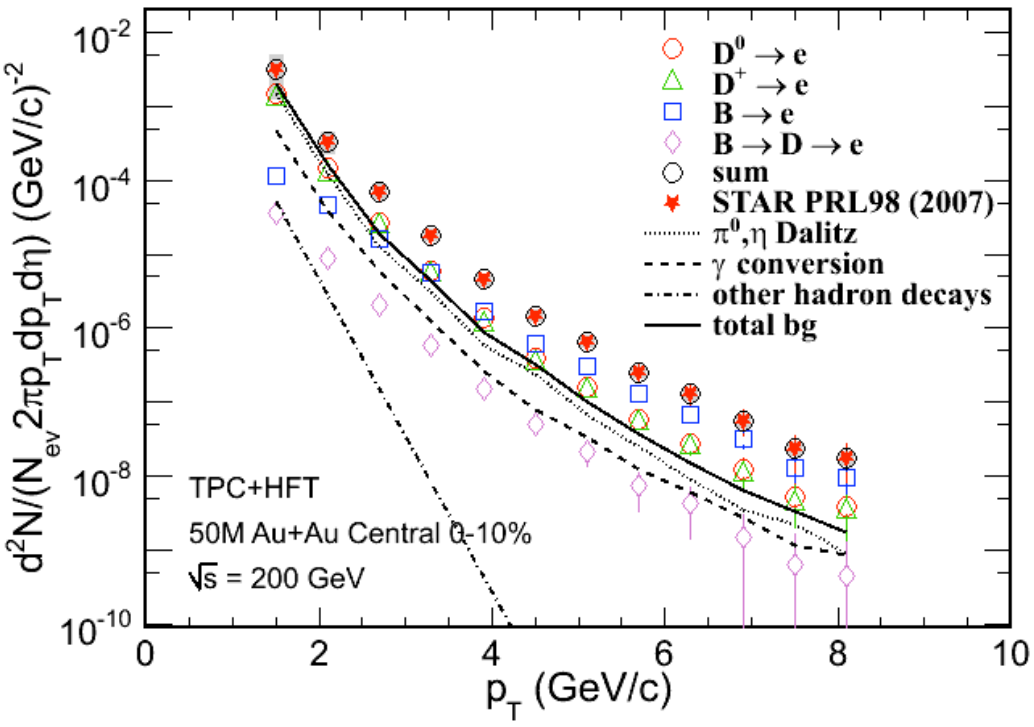


Figure 18: Electron spectra from B and D meson semi-leptonic decay. The expected errors as a function of p_T were estimated for 50 M Au+Au central events.

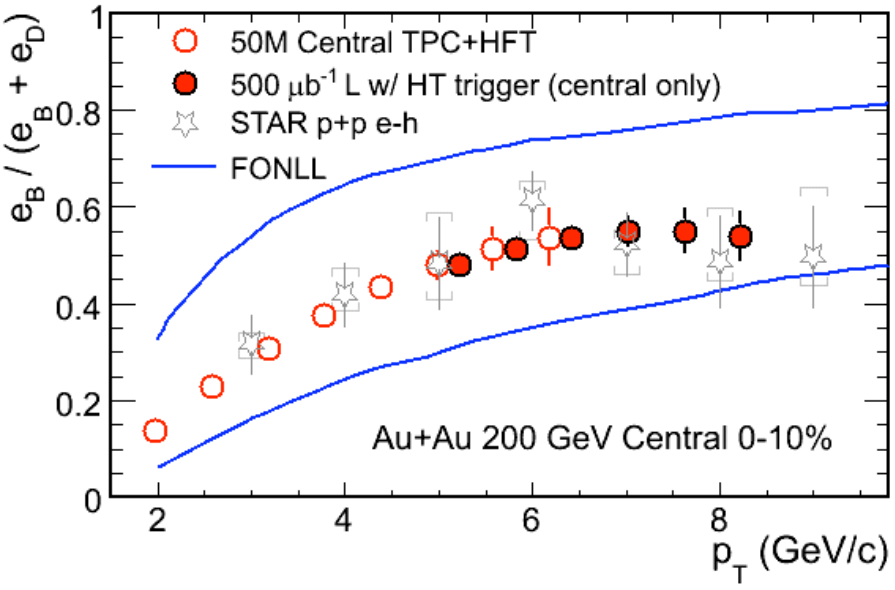


Figure 19: The (B→e)/NPE ratio as a function of p_T. Expected errors are estimated for 50 M Au+Au central events (open circles) and 500 μb^{-1} sampled luminosity with a "high tower" trigger (filled circles). Open stars represent preliminary results from 200 GeV p+p collisions.

Figure 20 shows the estimated precision for a measurement of R_{CP} of non-photonic electrons from D (red) and B (blue) decay as a function of p_T, where we assume the respective R_{CP} (dotted

curves) from a theoretical calculation of the T-matrix approach to heavy quark diffusion in the QGP.[37] For low p_T R_{CP} and the expected errors are calculated from 500M Au+Au central events (open symbols). For high p_T we used a "high tower" trigger sampling 500 μb^{-1} luminosity (filled symbols).

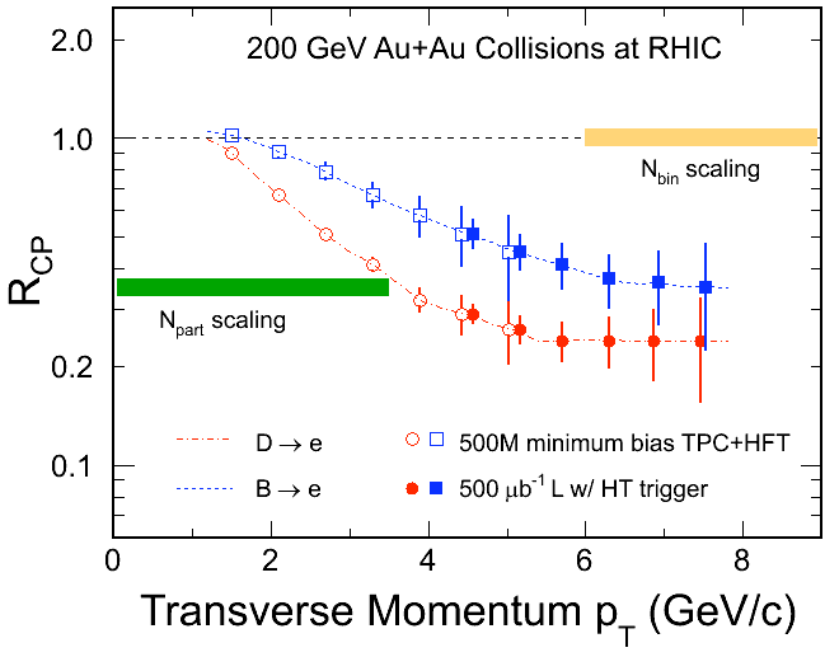


Figure 20: Nuclear modification factor R_{CP} of electrons from D meson and B meson decays. Expected errors are estimated for 500 M Au+Au minimum-bias events (open symbols) and 500 μb^{-1} sampled luminosity with a "high tower" trigger (filled symbols).

The relative fractions of D → e and B → e can be varied by different cuts on the electron DCA distribution. This can be used to measure the elliptic flow parameter of electrons for both D → e and B → e following the equation:

$$v_2^{NPE} = r \times v_2^{B \to e} + (1-r) \times v_2^{D \to e}, \qquad (1)$$

Here r is the (B→e)/NPE ratio. Table 6 shows two ratios from two cases of different DCA cuts in one of the p_T bins of $4.8 < p_T < 5.4$ GeV/c shown in Figure 19.

Case	Cut (μm)	e(D) eff. (%)	e(B) eff. (%)	r=e(B)/NPE
I	< 50	45.5	22.3	0.325
II	> 200	15.3	39.6	0.718

Table 6: Ratios for two different DCA cuts.

From the v_2 of the non-photonic electrons from different DCA cuts we can extract the electron v_2 for both, D → e and B → e. We also will have a precise measurement of the v_2 of D mesons as a

function of p_T via reconstruction from the hadronic decay channel, which constrains the D → e v_2 due to decay kinematics. Thus the v_2 of B mesons decaying into electrons can be obtained.

In order to estimate statistics of the electron v_2 measurement we assume that the v_2 of D mesons follows a transport model with quark coalescence and does not drop at high p_T. The red dashed curve in Figure 21 shows the D meson v_2 for the case that the charm quark has the same size partonic flow as measured for the light quarks (v_{2c}=v_{2q}). The blue dashed curve shows the limiting case where the charm quark does not flow (v_{2c}=0). Both curves are already shown in Figure 8. We use the form factor decay to generate D → e v_2 distributions, shown as red open circles and blue open squares for the corresponding two cases. The ratio r = (B→e)/NPE is taken from STAR e-h correlation shown in Figure 19. The v_2 of non-photonic decay electrons is taken from the PHENIX[38] measurement. The B → e v_2 can be obtained from equation (1). The statistic errors shown in Figure 21 are estimated for both, D → e v_2 (red and blue bars) and B → e v_2 (black bars), with 500 M Au+Au minimum-bias events. A possible Λ_c enhancement in Au+Au is not taken into account in the v_2 estimate.

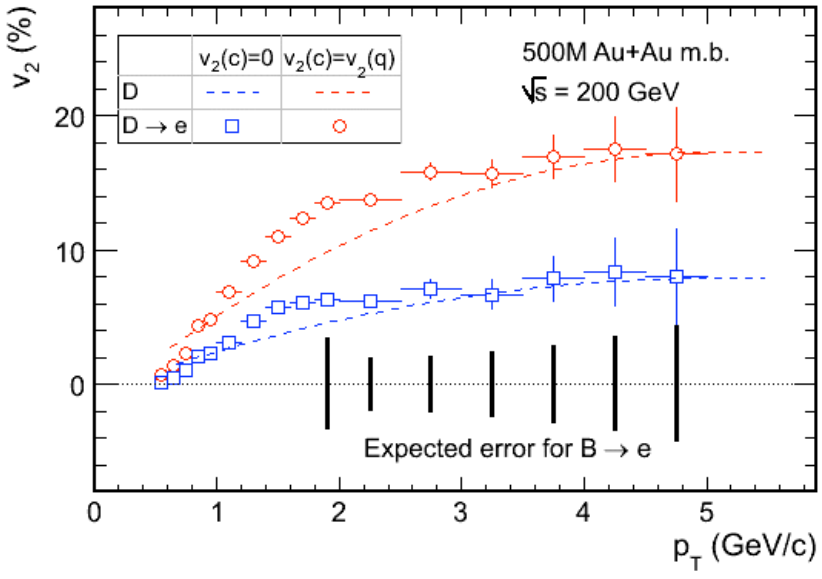


Figure 21: Expected statistical errors of D → e and B → e v_2 for 500 M Au+Au minimum-bias events.

2.8. W Production at Mid-rapidity

The STAR experiment has recently completed in Run-9 a program, collecting data during the first collisions of polarized proton beams at a beam energy of 250 GeV, giving rise to a center-of-mass energy of 500 GeV. This marks the beginning of a multi-year program studying the polarization of anti-quarks inside the proton using the production of $W^{\pm}$ bosons which are produced only at an appreciable rate above ~500 GeV in center-of-mass energy of colliding proton beams. This research effort has long been stressed as a key element of the RHIC Spin program.[39,40]

A dedicated program by the PHENIX and STAR collaborations is devoted to the understanding of the gluon polarization. Results obtained by both collaborations have been included now in a

first global analysis together with data from polarized deep-inelastic scattering (DIS) experiments constraining the degree to which gluons are polarized.[41] The net contribution of the gluon spin to the proton spin for momentum fraction of the gluon between 5% and 20% is very small. This finding is dominated by data collected at RHIC by the PHENIX and STAR collaborations in polarized proton-proton collisions at a center-of-mass energy of 200GeV.

The outer silicon layers of the HFT system, the IST and the SSD, will be available for 500 GeV p+p running. We show in this section that these detectors can improve the measurements in the high luminosity running.

2.8.1. Mid-rapidity W Program at STAR

In spite of the large body of DIS data which provided a strong constraint on the combined quark and anti-quark contribution of about 25% to the proton spin, polarized DIS measurements have important limitations. In particular, they do not directly provide information about anti-quark distributions. Hence the interest in high-energy polarized proton-proton collisions, which could offer new insight, complementary to DIS using parity violating processes in polarized proton-proton collisions.

The production of $W^{-(+)}$ bosons provides an ideal tool to study the spin-flavor structure of the proton. $W^{-(+)}$ bosons are produced in $\bar{u}+d$ $(\bar{d}+u)$ collisions and can be detected through their leptonic decays, $e^{-}+\bar{\nu}_e$ $(e^{+}+\nu_e)$, where only the respective charged lepton (electron/positron in the case of STAR) is measured.

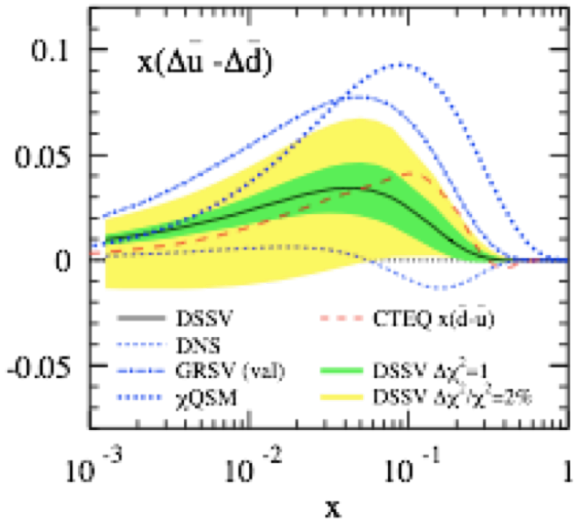


Figure 22: Difference of polarized u-antiquark and polarized d-antiquark distribution functions as a function of x for different global fit results, DSSV, DNS and GRSV.[42] The result obtained by the DSSV fit is shown together with uncertainty bands for $\Delta\chi^2$=1 and $\Delta\chi^2/\chi^2$=2%. Also shown is a model prediction from the chiral quark soliton model.

The difference of unpolarized anti-quark distribution functions as obtained by the CTEQ global analysis is shown for comparison. Figure 22 provides an overview of the current understanding of polarized anti-quark distribution functions, quantified as the difference of the respective anti-u ($x\Delta\bar{u}$) and anti-d ($x\Delta\bar{d}$) helicity distribution functions.[42] The DSSV global fit results in a difference of $x(\Delta\bar{u}-\Delta\bar{d})$ with a tendency to be larger than zero. A model calculation within the

chiral quark soliton model also shows a positive difference. It has long been expected that non-perturbative QCD effects play an important role to account for the observed asymmetries in the production of anti-u and anti-d quarks. Various model calculations suggest an even larger difference for polarized anti-u and anti-d quarks.

The theoretical framework of extracting polarized quark and anti-quark distribution functions based on measurements of parity-violating single spin asymmetries is very well developed. This provides a firm basis to use W production measurements in polarized proton-proton collisions at a center-of-mass energy of 500 GeV in a global analysis. At mid-rapidity, STAR will rely on the STAR TPC augmented in the future by high precision inner silicon detectors. The impact of additional tracking capabilities at mid-rapidity based on the combination of the IST and SSD layers profiting from their fast readout capabilities will be discussed. At forward rapidity, new tracking capabilities will be provided by a Forward GEM Tracker (FGT) consisting of six triple-GEM detectors currently under construction.

The wide-rapidity calorimetric coverage of the STAR experiment based on the BEMC and EEMC provides an important basis to carry out a program of W production using various tools for electron/hadron discrimination.

The forward/backward rapidity region of the EEMC yields large sensitivity to polarized anti-quark distribution functions. In addition, a leading order analysis of measured asymmetries is possible in this kinematic region, allowing to relate directly measured asymmetries to polarized distribution functions at leading order. In general, the ultimate extraction of polarized distribution functions will proceed through a full global analysis. In the case of STAR, this will be possible using measurements at mid-rapidity and forward/backward rapidity.

Figure 23 shows quark and anti-quark distributions for different global fit results (top) together with leptonic asymmetries as a function of the lepton rapidity for $-2.5 < \eta_e < 2.5$ (bottom) for the same set of distribution functions. It is both the forward and mid-rapidity kinematic region that provides important constraints on anti-quark distribution functions. Kinematic regions where quark polarizations dominate, yield large parity violating asymmetries. This will provide an important consistency check of already well-known quark distributions functions and points to the universality nature of polarized distribution functions. Those distribution functions are probed at RHIC as shown in Figure 23 at the mass scale of the W boson mass, which is substantially larger than the scales accessible in polarized lepton-nucleon scattering experiments.

2.8.2. Electron/Hadron Separation at Mid-rapidity

The yield of W boson signal events (weak interactions) over QCD background (strong interactions) is expected to be very small. The suppression of QCD background over W boson signal events by several orders of magnitude is accomplished by using the highly segmented STAR Electromagnetic Calorimeters (EMC), requiring an isolation criteria suppressing jet events, and vetoing di-jet events based on the measured away side energy. Establishing a first W signal over QCD background is an important milestone and was a physics goal of the recently completed 500 GeV data taking period in Run-9.

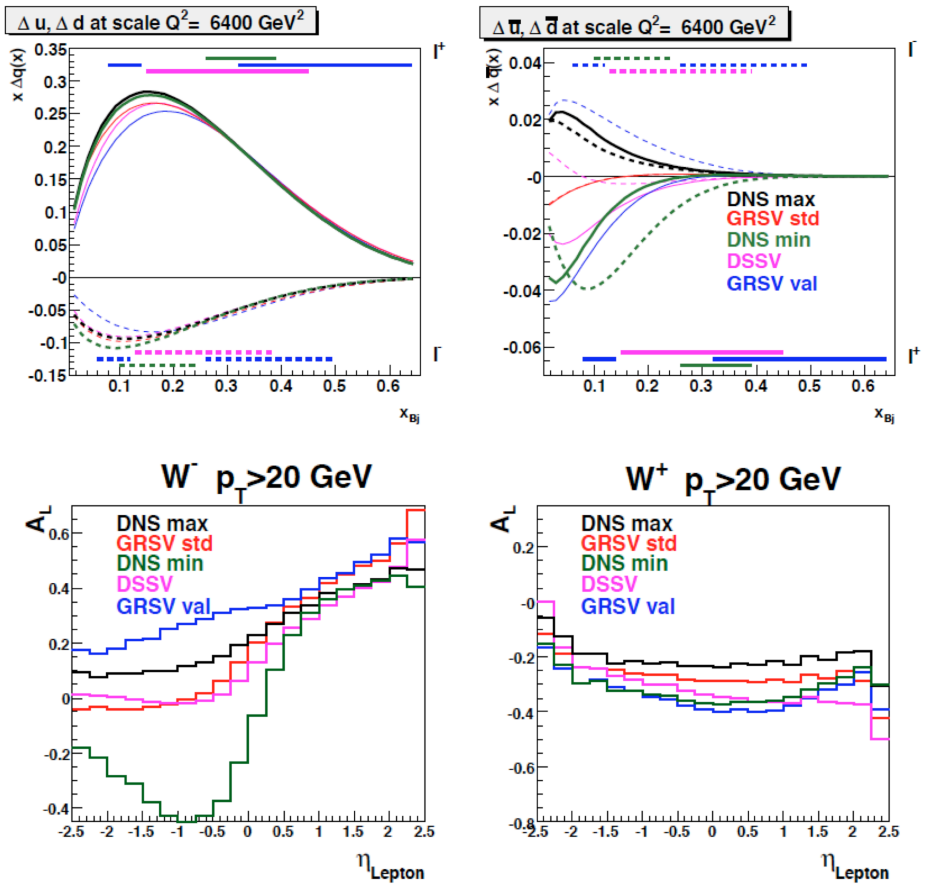


Figure 23: Quark and anti-quark distributions for different global fit results (top) together with leptonic asymmetries as function of the lepton rapidity for $-2.5 < \eta_e < 2.5$ (bottom).

2.8.3. Charge-sign Discrimination at Mid-rapidity

The measurement of a parity violating single spin asymmetry separately for W^+ and W^- requires the ability to efficiently separate the charge for electrons and positrons at large transverse momentum. This poses a new challenge on the understanding and calibration of the STAR TPC. A series of fast simulations have been performed using the IST/SSD combination to aid in improving the high-p_T tracking capability in addition to a vertex constraint and the TPC. For the TPC two cases have been examined. One in which all sectors (inner and outer) contribute and one in which only the outer TPC sectors contribute due to potential degraded performance at 500 GeV running in polarized proton-proton collisions. This is considered to be the worst-case scenario. Figure 24 shows the normalized momentum resolution as a function of the electron transverse momentum. The momentum resolution has been normalized in all cases to the Vertex plus standard TPC configuration. A drastic degradation of the momentum resolution - as expected - is found for the case where no TPC inner sectors are taken into account. This scenario is significantly improved to be even better than the Vertex plus standard TPC configuration if one adds precision hits of the IST. There is no improvement if in addition precision hits of the SSD layer are added. This is not surprising since both layers are rather close to each other compared to the overall scales of the TPC. In addition, there is a clear improvement if one considers the Vertex plus standard TPC configuration and adds hits of the IST. Besides an improvement of the momentum resolution including an IST layer in particular for a degraded TPC inner sector

configuration, the single-track efficiency has to be as well considered. As shown in Figure 24 (right), the single-track efficiency with the IST only (similar for SSD only configuration) in addition to the Vertex and TPC configuration yields a very low efficiency. This efficiency - as expected - is to a large extent restored if one adds in addition precision hits from the SSD layers.

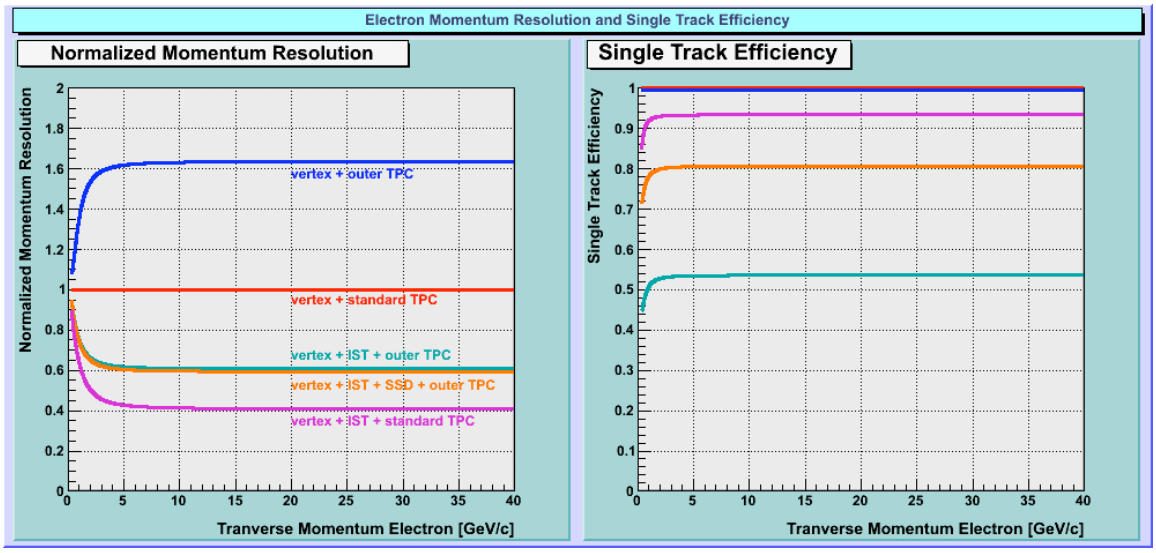


Figure 24: Normalized momentum resolution (left) and single track efficiency (right) as a function of the electron transverse momentum for different tracking configurations: Vertex and standard TPC (outer and inner sectors) (red), Vertex and only outer TPC sectors (blue), Vertex, IST and only outer TPC sectors (cyan), Vertex, IST, SSD and only outer TPC sectors (green) and Vertex, IST and standard TPC (yellow).

In summary, the combination of precision hits from the IST and SSD layers plays a critical role for efficient high-p_T track reconstruction which will be critical for the W program of charge-sign reconstruction of high-p_T electron/positron tracks in particular taking into account a degraded performance of the TPC inner sectors during 500 GeV running. Here we even assumed that the TPC inner sectors are not even available at all. Again, this defines the worst possible scenario.

2.8.4. Projected Performance of W Production

The expected performance in charge-sign discrimination probability, which enters directly the measurement of a charge-separated single-spin asymmetry AL is shown in Figure 25. The charge-sign discrimination probability is shown as a function of pT for an outer TPC configuration with different assumed vertex resolutions ranging from 0.5mm to 3mm. Adding the IST/SSD combination restores the charge-sign discrimination at 100% and leads to the assumed level in Figure 26. As discussed earlier, it is the combination of the IST/SSD system, which is required for efficient charge-sign discrimination at high pT for the case of where the inner TPC sector system is degraded in its performance. A vertex requirement alone together with the TPC outer system will not lead to 100% charge-sign discrimination in particular for those cases where the vertex resolution is degraded due to the availability of the outer TPC system only. It should be understood that no charge-sign discrimination is available without a vertex requirement. However, in those cases the precision hits of a IST/SSD system restores as well the required charge-sign discrimination.

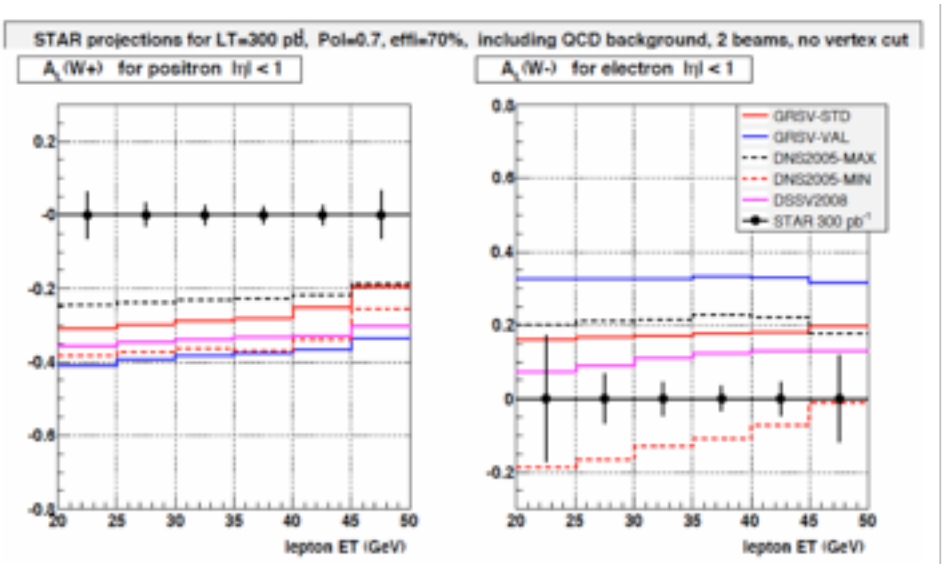


Figure 25: Projected uncertainties for 300pb-1 and 70% beam polarization of AL as a function of ET in the mid-rapidity acceptance region of the STAR BEMC (-1 < η < 1).

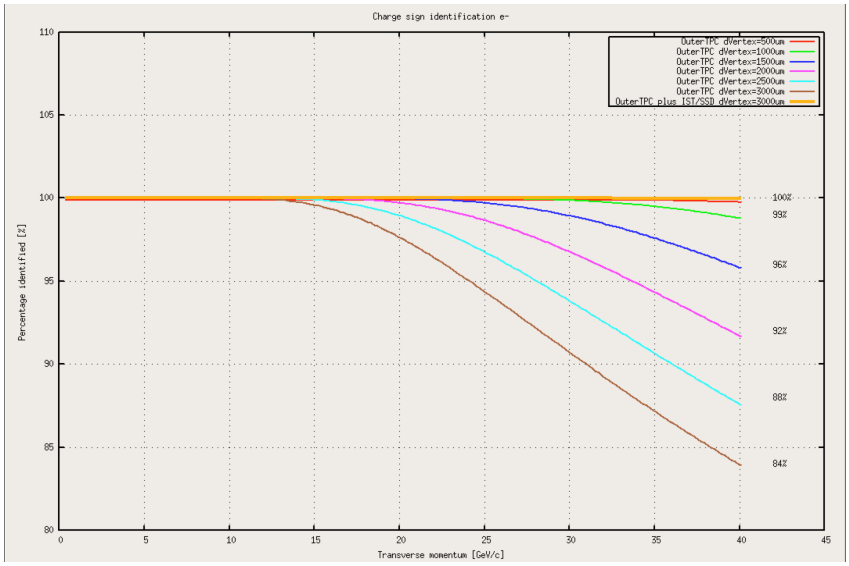


Figure 26: Percentage of charge sign discrimination for different configurations.

3. Functional Requirements

3.1. General Design Considerations

STAR is a large acceptance experiment with full azimuthal coverage at mid-rapidity in the pseudo-rapidity range |n| < 1. With the TPC as a central detector and a current readout speed of about 1000 Hz STAR is considered to be a "slow" detector as far as single particle observables are concerned. Even after the DAQ upgrade to 1000 Hz in 2009 the readout speed will be limiting the single particle capabilities of STAR. The real strength of STAR, good particle identification and full azimuthal coverage, come into play when correlations or multi-particle final states are studied. Good particle identification and full azimuthal coverage have been the bases for the enormous success of the STAR physics program.

When it comes to identifying rare processes, like heavy flavor production with multi-particle final states, full azimuthal coverage will be of utmost importance. Thus, full azimuthal coverage is a prime design requirement for the HFT.

Another important requirement is to keep a very low overall material budget in order to limit the effects of multiple scattering and of conversions. Our goal is to overall reduce the radiation length of the inner tracking and support system compared to the status when the SVT was the STAR inner tracking detector.

The performance requirements listed below are selected so that if the detector meets those requirements, the detector will be able to achieve the physics requirements. Fulfillment of the performance requirements can be completely determined shortly after the installation of the HFT.

The Performance requirements are summarized in Table 7.

Pointing resolution for kaons	< 50 μm
Thickness of first PXL layer	< 0.4 % X_0
Internal alignment PXL	< 20 μm
Internal alignment IST and SSD	< 300 μm
PXL integration time	< 200 μs
PXL and IST Readout speed and dead time	Follow STAR DAQ-1000, no more than 5% additional dead time
SSD dead time	<7% at 750 Hz
Detector hit efficiency	> 95%
Live channels for PXL and IST	> 97%
Software and procedures ready	Tested and functional software

Table 7: HFT Performance requirements.

3.2. Pointing Resolution

Heavy flavor hadrons have extremely short life times ($c\tau \sim 50$ μm). Identifying such a short displaced vertex requires extremely good pointing resolution. This is especially important for the identification of low transverse momentum decays where small gains in pointing resolution lead to large gains in detection efficiency. The pointing resolution in R-ϕ and in Z-direction are shown in Figure 27 as a function of p_T.

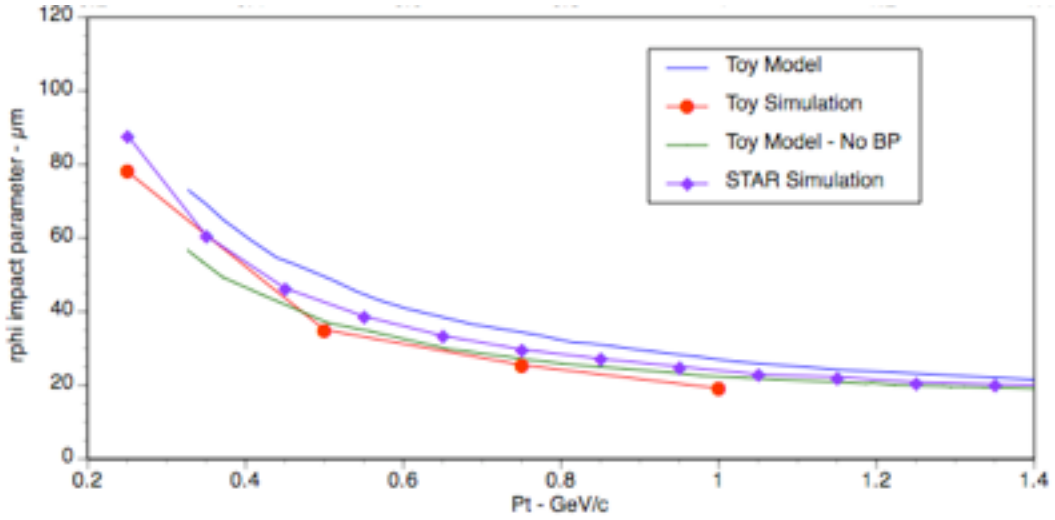


Figure 27: Comparison of three different types of simulations to determine the pointing resolution in the R-ϕ direction at the vertex for kaons. The three methods are a Toy Model, Fast Simulation, and the full STAR Simulation. Each method has different assumptions and slightly different parameters but overall, the agreement is good. In the figure's legend, BP is short hand for "beam pipe". From Reference [4].

We require a pointing resolution of better than 50 μm for kaons of 750 MeV/c. 750 MeV/c is the mean momentum of the decay kaons from D mesons of 1 GeV/c transverse momentum, the peak of the D meson distribution.

The pointing resolution that will be achieved by the HFT can be calculated from the design parameters, and from the results of surveys of the sensor ladders

3.3. Multiple Scattering in the Inner Layers

The precision with which we can point to the interaction vertex is determined by the position resolution of the PXL detector layers and by the effects of multiple scattering in the material the particles have to traverse. The beam pipe and the first PXL layer are the two elements that have the most adverse effect on pointing resolution. Therefore, it is crucial to make those layers as thin as possible and to build them as close as possible to the interaction point.

We have chosen a radius of 2 cm for a new beam pipe. Making this radius even smaller would make the STAR beam pipe the limiting aperture of the RHIC ring. This is not a desirable situation. The central section of the beam pipe will be fabricated from beryllium. Such a beam

pipe will have a minimal wall thickness of 750 μm, equivalent to 0.21 % of a radiation length. The beam-pipe is not part of the HFT project, but is procured with these specifications.

The two PXL layers will be at a radius of 2.5 cm and 8 cm, respectively. The sensors will be thinned down to 50 μm and the ladders will be fabricated in ultra-light carbon fiber technology. The total thickness of the first PXL layer will be the equivalent of 0.4 % of a radiation length. With those parameters, the contributions to the pointing resolution from multiple scattering and from detector resolution will be about equal for 1 GeV/c particles.

The radiation lengths of the two innermost structures, the beam pipe and the first PXL layer, are design parameters.

3.4. Internal Alignment and Stability

The PXL and the IST positions need to be known and need to be stable over a long time period in order not to have a negative effect on the pointing resolution. The quality of the data will depend on alignment and long-term stability. This is especially important for the PXL detector that needs to be installed and removed on a short time scale.

The alignment and stability need to be better than 300 μm for the IST and SSD and better than 20 μm for the PXL.

Those parameters can be determined from a survey.

3.5. PXL Integration Time

Compared to IST and SSD, the PXL is a slow device with a long integration time. All events that occur during the integration or lifetime of the PXL will be recorded. This makes assigning PXL hits to a particular track in the TPC a difficult pattern recognition problem.

From detailed simulations we have concluded that at RHIC II luminosities the detection and reconstruction efficiency for D-mesons is not appreciably degraded due to multiple events and tracks in the PXL if the integration time of the detector is smaller than 200 μs.

The PXL integration time is a design parameter.

3.6. Readout Speed and Dead Time

In the absence of a good trigger for D-mesons it is imperative for the measurement of rare processes to record as many events as possible and as required by the physics processes. In STAR the speed of the DAQ-1000 is the limiting factor for the number of events recorded when the readout of the TPC is required. In order not to add significant dead-time to DAQ, the PXL and IST readout speed needs to be compatible with that of DAQ-1000 and the dead-time such that the PXL and IST do not contribute more than 5% of the total dead time. The SSD readout speed needs to be compatible with the STAR DAQ speed and should not add more than 7% dead time at 750 Hz data acquisition rate.

Readout speed and dead time are design parameters.

3.7. Detector Hit Efficiency

The hit efficiency of PXL and IST detectors is essential for good detection efficiency. In the case of secondary decay reconstruction, the hit inefficiency of each detector layer enters with the power of the number of reconstructed decay particles into the total inefficiency.

In order to keep inefficiency low, we request that each individual detector layer has a hit efficiency of better than 95%.

The hit efficiency of each detector layer can be measured on the bench before installation.

3.8. Live Channels

Dead channels in the PXL and IST will cause missing hits on tracks and thus lead to inefficiencies in the reconstruction of decay tracks. Therefore, the number of dead channels needs to be as low as possible.

The impact of dead channels on the overall performance will be minimal if more than 97% of all channels are alive at any time.

The number of dead channels can be determined immediately after installation of the detectors.

3.9. Software and Procedures Ready

Analysis, Alignment, and Calibration procedures and software are necessary for the ability to analyze data and to extract physics information. The detector performance can only be realized if software and procedures are in place and fully functional.

Software and procedures are ready when test data or simulated data can be processed through the official STAR analysis chain.

4. Technical Design

4.1. Requirements and Detector Design

The HFT will extend the STAR physics capabilities to the identification of short-lived particles containing heavy quarks through reconstruction and identification of the displaced vertex at mid-rapidity. STAR has 2π azimuthal coverage and to match this, the HFT is required to have 2π azimuthal coverage.

In order to identify short displaced vertices the HFT is required to have excellent pointing resolution of the order of 50 μm. A two-layer high-resolution vertex detector placed close to the interaction vertex can achieve good pointing resolution. In the high-multiplicity environment of heavy ion collisions, the HFT also needs to provide excellent tracking resolution in order to connect tracks identified in the TPC, acting alone, with the corresponding hits in the vertex detector. The resolution of the TPC is not good enough to assign hits in the vertex detector to identified particles with high efficiency. Thus the HFT needs to provide intermediate tracking in the region between the TPC and the vertex detector. We also require redundancy in the design.

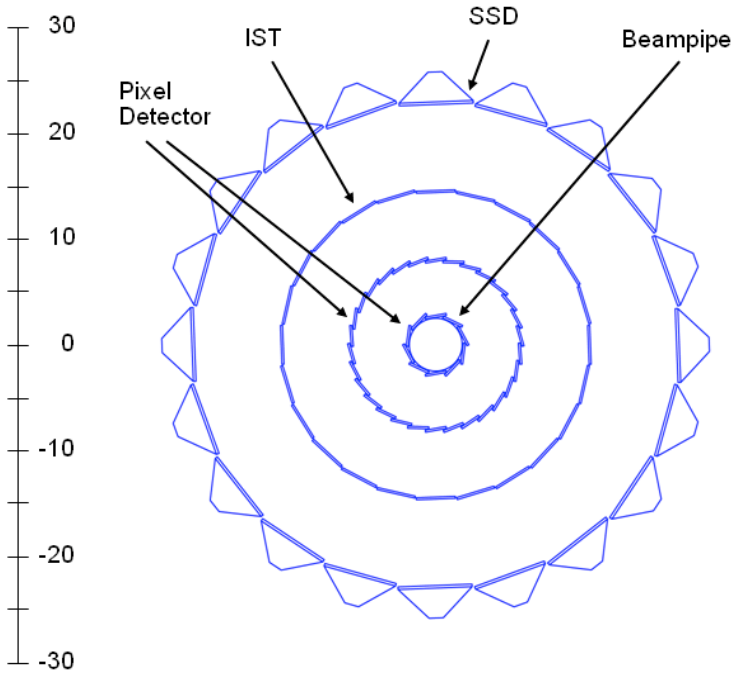


Figure 28: A schematic view of the Si detectors that surround the beam pipe. The SSD is an existing detector and it is the outmost detector shown in the diagram. The IST lies inside the SSD and the PXL lies closest to the beam pipe.

These requirements lead to the HFT design of 4 layers of silicon detectors distributed in radius between the interaction point and the TPC. Figure 28 shows the radial distribution of the four layers. The inner two layers, the PXL, lay at 2.5 and 8 cm, the IST lays at 14 cm and the SSD at 22 cm. A schematic view of the different HFT layers between the beam pipe and the inner field cage of the TPC is shown in Figure 29.

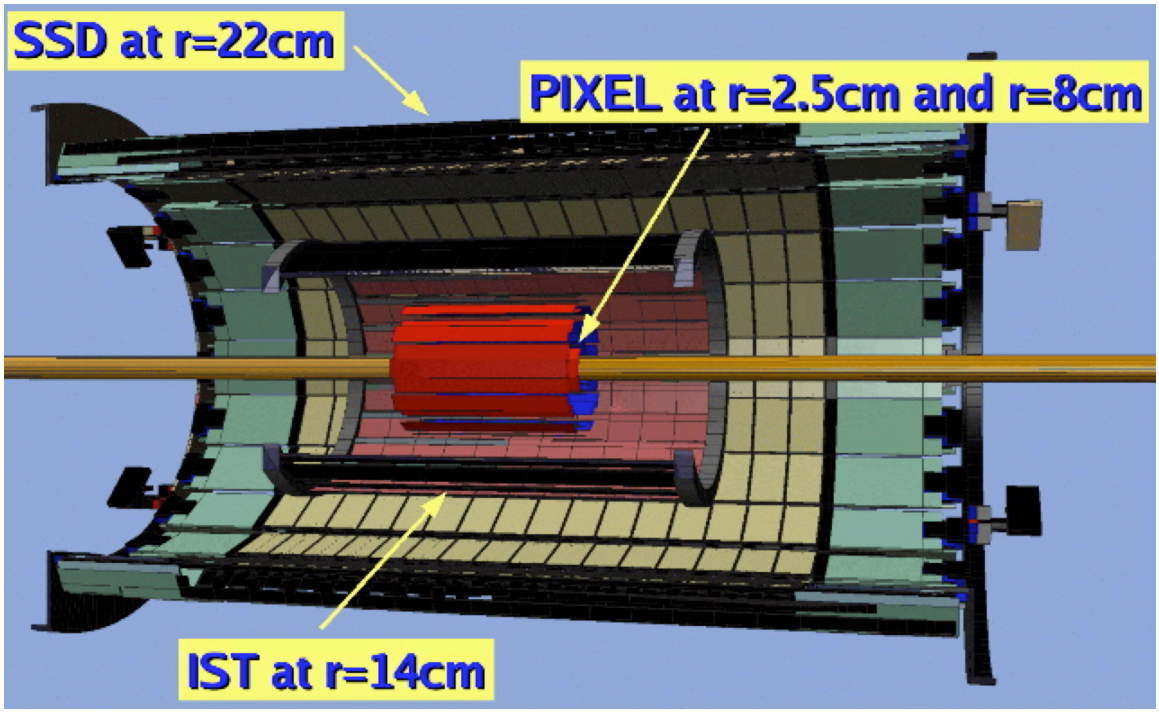


Figure 29: Schematic view of the different layers of the HFT.

The pointing resolution that can be achieved with a given system has two components, a contribution from detector resolution and a contribution from the effects of multiple scattering. Using low radiation length material, in particular between the interaction point and the second layer of the detector can minimize multiple scattering. The HFT requirements are that the PXL and the beam pipe be as thin as technically possible and that the first detector layer be as close to the interaction point as technically feasible.

In order to meet those requirements, STAR needs a new beryllium beam pipe with a radius of 2 cm. The integrated radiation length from the interaction point to the outside of the PXL detector is 1 % of a radiation length.

Table 8 gives an overview of the pointing resolution at intermediate points along the path of a 750 MeV kaon as it is traced back from the TPC to the vertex. Good resolution at the intermediate points is necessary to resolve ambiguous hits on the next layer of the tracking system with high efficiency.

Graded Resolution from the Outside - In		Resolution (σ)
TPC pointing at the SSD	(22 cm radius)	~ 1 mm
SSD pointing at IST	(14 cm radius)	~ 400 μm
IST pointing at PXL-2	(8 cm radius)	~ 400 μm
PXL-2 pointing at PXL-1	(2.5 cm radius)	~ 125 μm
PXL-1 pointing at the vertex		~ 40 μm

Table 8: Pointing resolution of the TPC and HFT detectors at intermediate points along the path of a 750 MeV kaon as it is tracked from the outside – in.

Good pointing resolution can overall only be achieved if the individual detectors guarantee a long-term mechanical stability and reproducibility that is of the order of the resolution of the detector. The numbers for the subsystems of the HFT are:

- PXL 20 μm
- IST 300 μm
- SSD 300 μm

An important requirement is that the HFT be able to be read out with a frequency that is compatible with STAR DAQ, i.e. 1000 Hz. All sub-detectors are read out individually and their readout needs to fulfill this condition. The IST and the SSD are fast detectors and achieving this is trivial. However, the existing readout chain for the SSD is designed for a slower readout speed and thus needs to be redesigned and built to fulfill the readout specification. The sensors of the PXL detector on the other hand have a slow readout time of the order of 100 μs. The individual pixels are always live and the sensors keep a memory of all tracks that pass through it during one readout cycle. This leads to pile-up of tracks that do not belong to the triggered event. Pile-up is unavoidable in this technique. With extensive simulations of the SSD, IST, and PXL detectors, we have shown that even at RHIC II luminosities the effects of pile-up are minimal if the readout time of the PXL sensors is smaller than 200 μs. This leads to the requirement that the readout time of the PXL sensors must be 200 μs or smaller.

The first layer of the HFT lies very close to the interaction vertex in a very high radiation field. The pixel sensors will be built in a technology that is not radiation hard. Thus, we require that the innermost sensors can operate during an entire RHIC year at highest RHIC II luminosities without a noticeable drop in efficiency. The location close to the beam is also prone to potentially catastrophic failure of the silicon in case of unintended and uncontrolled excursions of the beam from its nominal orbit. For the case of catastrophic failure or diminished efficiency due to high radiation, we want to be able to replace the PXL detector with a new, fully functioning copy of the detector and so we require that the PXL detector can be exchanged within one day.

Calibration of a micro-vertex detector is very elaborate and time-consuming. The concept of replacing a detector within the short time span required for the HFT can only work, if the new detector is calibrated internally on the bench and if this calibration can be transferred to the inserted detector. This is a very important requirement for the PXL sub-detector.

The HFT needs to operate under RHIC II conditions and luminosities. The outer layers (IST, SSD) are required to operate for 10 years in this radiation field without degradation of performance in terms of efficiency. The PXL layers of the HFT are retractable and can be replaced in case of damage. The PXL layers need to operate for one year under the highest RHIC II luminosities without appreciable deterioration of the detection efficiency.

4.2. The Pixel Detector (PXL)

The PXL detector is a low mass detector that will be located very close to the beam pipe. It will be built with two layers of silicon pixel detectors, one layer at 2.5 cm average radius and the other at 8.0 cm average radius. The PXL will have a total of 40 ladders, 10 in the inner layer and 30 in the outer layer. Each ladder contains a row of 10 monolithic CMOS detector chips and each ladder has an active area of ~19.2 cm × ~1.92 cm. The CMOS chips contain a ~1000 × ~1000 array of 18.4 μm square pixels and will be thinned down to a thickness of 50 μm to minimize Multiple Coulomb Scattering (MCS) in the detector. The effective thickness of each ladder is

0.37% of a radiation length. The relevant performance parameters for the PXL detector are shown in Table 9.

Pointing resolution	(13 ⊕ 22GeV/p·c) μm
Layers	Layer 1 at 2.5 cm radius Layer 2 at 8 cm radius
Pixel size	18.4 μm × 18.4 μm
Hit resolution	10 μm rms
Position stability	6 μm (20 μm envelope)
Radiation thickness per layer	X/X0 = 0.37%
Number of pixels	~436 M
Integration time (affects pileup)	0.2 ms
Radiation tolerance	300 kRad
Rapid installation and replacement to cover radiation damage and other detector failure	Installation and reproducible positioning in 8 hours

Table 9: Performance parameters for the PXL detector.

4.2.1. Technology Choice

Topological reconstruction of D mesons in the heavy ion STAR environment requires extremely good pointing resolution. In the heavy ion environment with thousands of tracks in a central collision, pointing resolution is critical to reduce the combinatorial background while maintaining good detection efficiency. Four technologies were considered for this task: hybrid pixels as used in LHC detectors, CCDs as were successfully used in the SLD experiment at SLAC, Monolithic Active Pixel Sensors (MAPS) and Depleted P- Channel Field Effect Transistors (DEPFET).

Hybrid pixels were rejected because of cost and performance. They are expensive and difficult to produce because they rely on specialized technology that is not generally available. These devices require high-density bump bonding of the sensor chips to the readout chips. The capability to do the special required bump-bonding is a very limited resource. While in principle hybrid detectors are a developed technology it is not a technology that is readily available. The manufacture of the hybrid devices for LHC was carried out by multiple collaborators rather than by commercial houses. One cannot just order additional copies from a commercial vendor, particularly since the LHC productions have been completed. To produce hybrids requires setting up new manufacturing facilities.

The performance of the hybrid devices is limited for our application by two features, radiation thickness and position resolution. Position resolution is limited by the pixel size, which is limited by the bump-bonding density that can be achieved. The radiation thickness is limited because both the detector silicon and the readout silicon have to be kept fairly thick to successfully bump-bond the two together. Additional radiation thickness is required for cooling. The hybrids designed for LHC applications are fast high power devices since they are required for triggering. They can afford the penalty of radiation thickness and position resolution because LHC events are

comparatively low multiplicity and the particles of interest have significantly higher momentum than in our application.

A comparison of pointing resolution performance between hybrids and MAPS or CCDs is shown in Figure 30 using two detector layers one at 2.5 cm radius and the other at 8 cm radius. The figure shows the ratio of the area resolution for pointing back to the interaction point. The hybrid used for this comparison has 50 µm by 450 µm pixels and has a radiation thickness of 1.2%. The MAPS has 18.5 µm by 18.5 µm pixels. The position resolution of the MAPS is set by the pixel size and the expected mechanical stability window of 20 µm. The radiation thickness for the MAPS is 0.37%. This is what can be achieved for a detector ladder. This includes a thinned silicon detector chip (50 µm), carbon composite support, a flex readout cable and the required bonding adhesives. In this comparison a 0.75 mm beryllium beam pipe has been included at a 2 cm radius.

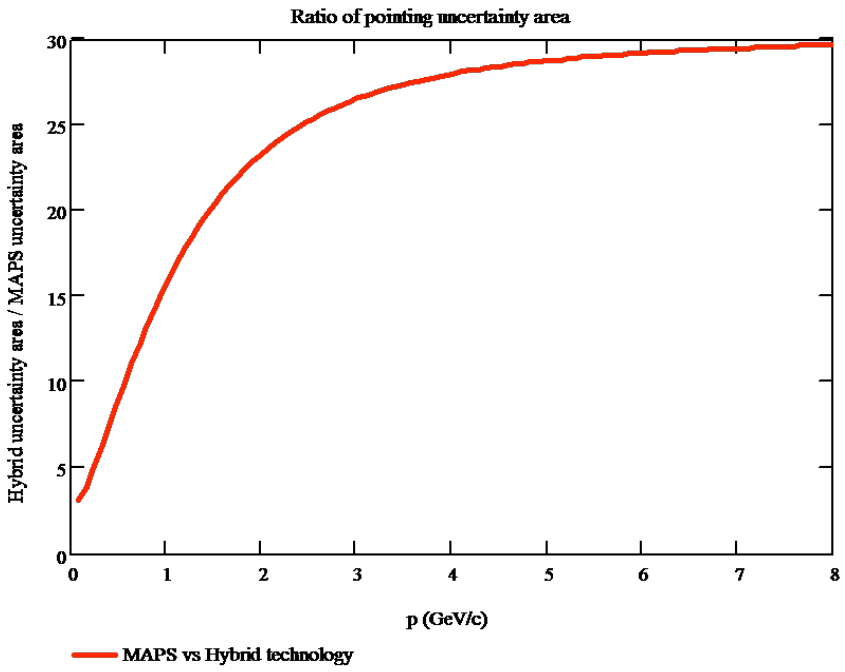


Figure 30: Comparison of pointing accuracy of MAPS and Hybrid technology. The ratio of the pointing area uncertainy of Hybrids divided by MAPS uncertainty is shown as a function of the momentum. At the low momentum end the MAPS have a 3 to 1 advantage. At high momemtum the advantage increases to 30.

From Figure 30 it can be seen that at the low momentum end (p = 100 MeV/c) where multiple coulomb scattering sets the performance limit the MAPS outperform the hybrid by a factor of 3. At p = 1 GeV/c the MAPS have a factor of 15 advantage and at the high end where performance is set by position resolution the MAPS are superior by a factor of 30. Both MAPS and CCDs can achieve the performance shown in Figure 30 because they can be built with small pixels, they can be thinned and they can operate at low power. Their disadvantage is slow readout speed, which results in pileup and their limited radiation hardness.

MAPS have been chosen over CCDs because of cost, accessibility to foundries, simplified cooling requirements, readout speed and radiation tolerance.

The cost of MAPS is expected to be less than CCDs because MAPS use standard CMOS technology available from several foundries. Their relatively low cost has been demonstrated with our shared project development runs and engineering runs. The cost of CCDs has not been explored, but use of these devices would most likely be limited to working with Rutherford Lab and depending on their access to a specialized foundry. In addition to the cost savings of using a standard CMOS process the main cost advantage of MAPS in our case is the result of our collaboration with Marc Winter's group at IPHC in Strasbourg. They have provided all the engineering to develop the MAPS devices.

Readout speed is also an important advantage of MAPS over CCD technology. In MAPS fast parallel hit discrimination and readout can be accomplished because the full suite of CMOS devices is available on the detector chip. This permits fast performance with relatively low power. With CCDs charge transfer requires drivers pulsing large capacitive loads on the chip. This requires significant power if done rapidly. There is an active program at Rutherford Lab improving performance of CCDs, but this relies on increased parallelization, which adds power, and more sophisticated sinusoidal drives which complicate peripheral electronics support.

Radiation hardness is another important advantage of MAPS over CCD technology. Bulk damage to the silicon from radiation increases signal loss due recombination and it increases leakage current. Recombination is less of a problem in MAPS because the electrons are collected in a few nanoseconds since they travel at most 30 μm while in CCDs the electron paths are on the centimeter scale. Likewise the leakage current is a significantly larger problem for CCDs. MAPS have a very limited silicon volume in the pixel that contributes to leakage while in CCDs a much larger volume with possible damage sites is sampled as the charge cluster is passed to the output. Leakage current is an issue when the amount of charge collected is sufficient to contribute shot noise. Shot noise is not an issue for MAPS that are readout rapidly even for devices that have received significant radiation levels. In addition, CCDs must be cooled, even when not damaged, to control leakage current. Cooling to below room temperature adds significant engineering complications and expense to the detector design.

MAPS have the cost benefit of reduced support development. They are digital devices, which do not require specialized electronics for readout. This can be done with standard FPGAs and off the shelf digital drivers. Thinning and dicing is a routine operation done by standard industry services. Detector ladders are built in house using normal wire bond connections.

DEPFET technology was also considered for this project. DEPFET devices have been developed and produced by only one institution, MPI Semiconductor Laboratory in Munich. This is by far the most aggressive technology and has potential for producing the best performance. The support structure and detector system would be fabricated as a single large piece of silicon and could be made exceedingly thin. We visited their laboratory and had discussions with them, but we decided not to go that route due to the remaining development hurdles and the reliance on a single institution with a unique foundry capability.

4.2.2. Design Considerations

Building in the capability for rapid exchange of the HFT PXL detector is an insurance policy. The investment of a relatively small amount of effort and expense makes it much more likely that the system will provide usable data. Insurance in this case is well warranted as history in our field shows that the odds are against a detector producing useful physics on its first deployment. This is an unfortunate situation, but nonetheless it should be recognized and addressed accordingly. Rapid exchange capability will allow mid run fixes which would not otherwise be possible. Replacement capability provides a way to overcome premature radiation damage

problems. It will also allow repairs of other possible failures that could compromise the data quality. The most important time for this capability is during the commissioning period when unanticipated problems are most likely to develop. If detector replacement is not routine, risk free and fast it will always be ruled out even in the event of catastrophic failure due to pressure from other interests in STAR and PHENIX. A fast and proven exchange system lowers the decision threshold for corrective action. Without a lowered threshold the policy decision will always favor proceeding with compromised performance. However, the decision as to whether or not to analyze the data comes from a completely different quarter. Smart students and postdocs are the ones who in the end decide which data and physics to pursue and they wisely choose the most likely path for success. That path does not steer them toward data from a poorly functioning device. This fact determines the success or failure of a detector.

Building a detector system with rapid exchange capability means more careful upfront attention to installation design, which improves chances for successful installation and deployment.

The main cost in manpower for rapid exchange capability is in the design and this cost is either free or contributed. The cost of implementation for both construction and operation could well be a money saver compared to a more casual approach to installation design. The main added construction costs for fast exchange capability are an installation platform and a new BBC support.

Returning to the insurance analogy, we routinely insure houses and cars where the cost of loss and the probability of loss are much smaller than in our case with the PXL detector. The insurance provided by rapid exchange capability provides excellent protection for low cost. It should not be neglected.

4.2.3. Mechanical Design of the PXL Detector

The mechanical design has been driven by the following design goals:

- Minimize multiple coulomb scattering, particularly at the inner most layer
- Locate the inner layer as close to the interaction region as possible
- Allow rapid detector replacement
- Provide complete spatial mapping of the PXL from the beginning

The first two goals, multiple coulomb scattering and minimum radius, set the limit on pointing accuracy to the vertex. This defines the efficiency of D and B meson detection.

The third goal, rapid detector replacement, is motivated by recognition of difficulties encountered in previous experiments with unexpected detector failures. This third goal is also motivated by the need to replace detectors that may be radiation damaged by operating so close to the beam.

The fourth goal, complete spatial mapping, is important to achieve physics results in a timely fashion. The plan is to know, at installation, where each pixel is located with respect to each other to within 20 microns and to maintain the positions throughout the lifetime of the detector.

An overview of the pixel detector is shown in Figure 31. PXL consists of two concentric barrels of detector ladders, which are 20 cm long. The inner barrel has a radius of 2.5 cm and the outer barrel has an 8 cm radius. The barrels separate into two halves for assembly and removal. In the installed location both barrel halves are supported with their own three-point precision kinematic mounts located at one end. During installation, the support for the detector is provided by the hinge structures mounted on a railed carriage. Cooling is provided by air flowing in from one end between the two barrel surfaces and returning in the opposite direction over the outer barrel surface and along the inner barrel surface next to the beam pipe.

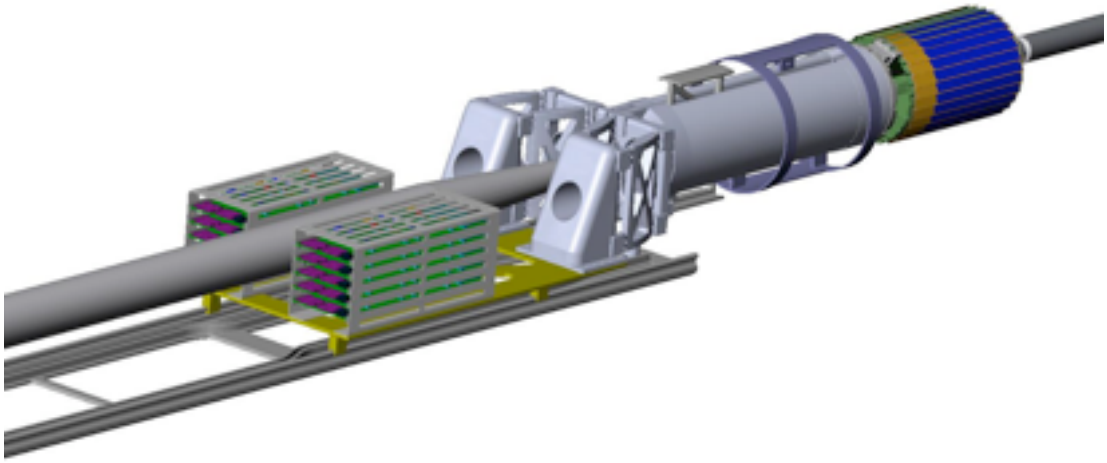


Figure 31: Overview of the PXL detector mechanics showing detector barrel, support structures and insertion parts plus interface electronics boards.

The design of the mechanical components is presented in the following sections. Related structural and cooling analysis is covered in Appendix 1.

Detector Ladder Design

The mechanical support for the detector chips is arranged in ladders. 10 chips in a row form a ladder. An exploded view of the mechanical components is shown in Figure 32. The thinned silicon chips are bonded to a flex aluminum Kapton cable which is in turn bonded to a thin carbon composite structure. All electrical connections from the chips to the cable are done with a single row of wire bonds along one edge of the ladder. The carbon composite sheet, which is quite thin, will only be sufficient for handling the chips and for heat conduction. Stiffness and support of the ladder is provided by the support beam. This particular ladder structure has been optimized based on our previous prototype designs which included gull wing and foam laminate designs. The assembly of the ladder and the attachment of ladders to the sectors is done with specialized vacuum tooling developed for this project. Parts are aligned and held in place with vacuum chuck tooling for bonding. Fifty micron soft, pressure sensitive acrylic adhesive 200MP by 3M is used to make the bonds. A method has been developed which uses a 4 bar pressure vacuum bag and the pressure of an autoclave to remove bond voids and to stabilize the bond. The low elastic modulus of the adhesive is an important component in the design as it greatly reduces bi-metal type deformations stemming from differential expansion caused by thermal changes and humidity changes. This is discussed in more detail in Appendix 1.

The next step in the ladder development will be to build additional mechanical prototypes to verify the mechanical design both structurally and thermally.

Ladder Support System

A critical part of the ladder support is the thin carbon composite beam which carries one inner ladder and three outer ladders as shown in Figure 33. The beam, which is an adaptation of the ALICE pixel detector design, provides a very stiff support while minimizing the radiation length budget. Significant stiffness is required to control deformations from gravity, cooling air forces and differential expansion forces from both thermal and humidity variations. The composite beam carries a single inner ladder and three outer ladders. Ten of these modules form the two

barrel layers. The beam, in addition to its support function, provides a duct for cooling air and adds cooling surface area to increase the heat transferred from the silicon chips. By making the beam from high strength and high thermal conductivity carbon fiber the wall thickness can be as thin as 200 microns and still satisfy the strength and heat transfer requirements. The final thickness however, will probably be limited by fabrication challenges. Forming methods under consideration are a single male mandrel with vacuum bagging or alternatively nested male and female mandrels. To date, we have constructed seven-layer, 244 micron thick, carbon composite beams using a female mandrel which satisfy our requirements.

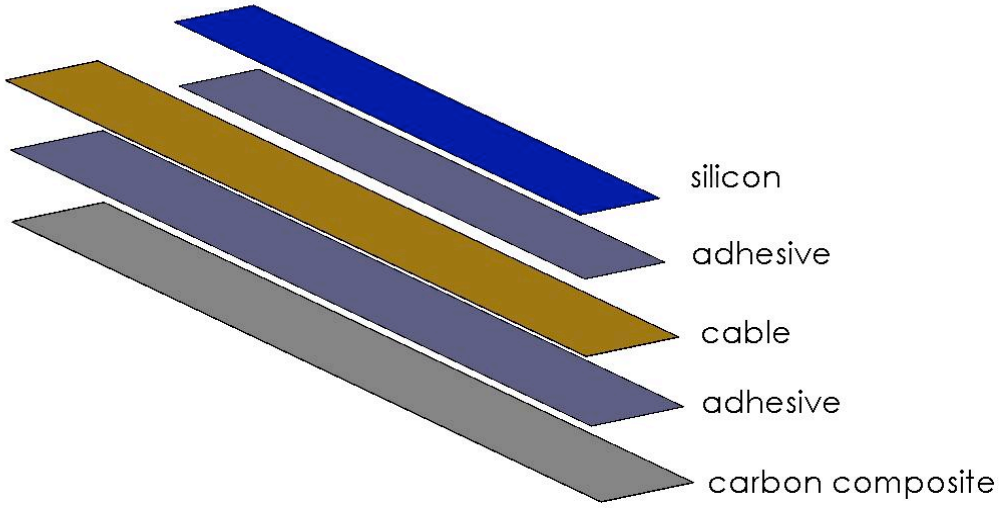


Figure 32: Exploded view of the ladder showing components. The silicon is composed of 10 square chips. It is shown here as a continuous piece of silicon, the way it has been modeled for analysis.

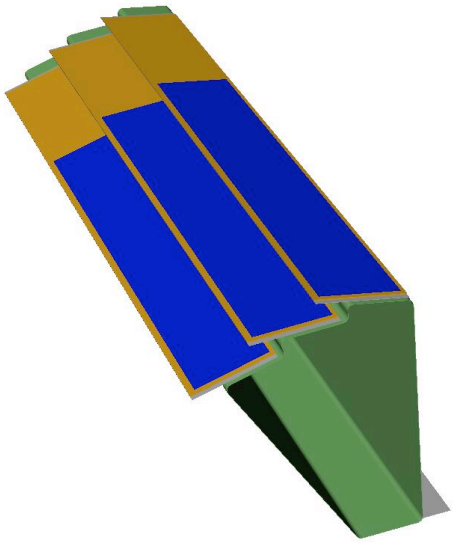


Figure 33: Thin wall carbon support beam (green) carrying a single inner barrel ladder and three outer barrel ladders. The beam in addition to supporting the ladders provides a duct for conducting cooling air and added surface area to improve heat transfer to the cooling air.

The ladders will be glued to the beam using low strength silicon adhesive as was done in the ATLAS pixel design. This adhesive permits rework replacement of single ladders.

Support of the sectors (beam with ladders) is done in two halves with 5 sector beams per half module (see Figure 34). The sector beams are attached to a carbon composite D-tube with precision dove tail mounts for easy assembly and replacement. The D-tube supports the 5 sector beams and conducts cooling air to the sectors.

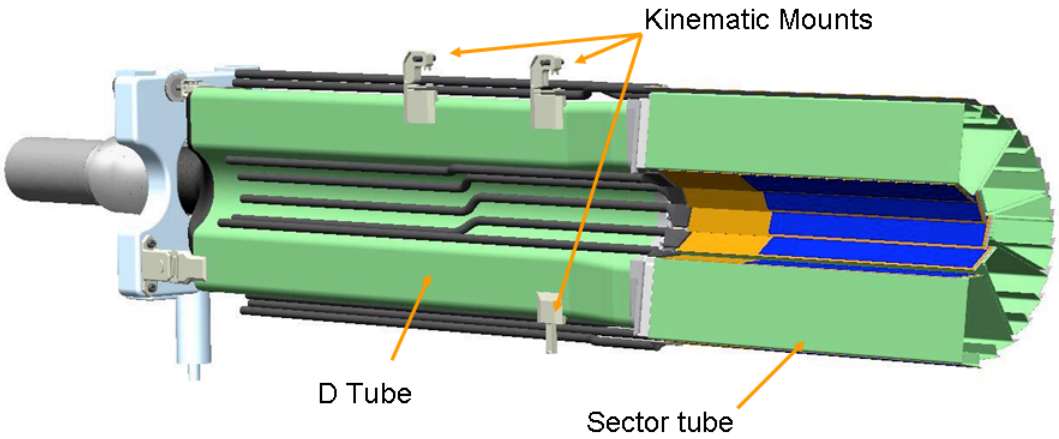


Figure 34: Half module consisting of 5 sector beam modules. The sector beam modules are secured to a carbon composite D tube using a dovetail structure, which permits easy replacement of sector modules. Carbon composite parts are shown in green for greater visibility.

Kinematic Support and Docking Mechanism

When the pixel detector is in its final operating position it is secured at 3 points with precision reproducible kinematic mounts to the Inner Support Cylinder (ISC) as shown in Figure 35.

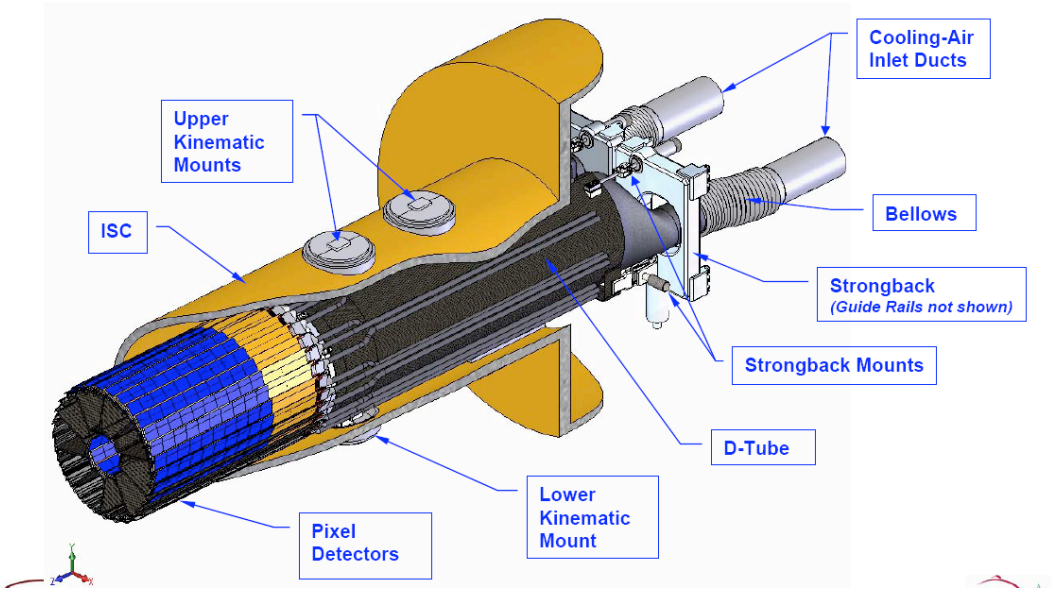


Figure 35: Detector assembly in the installed position supported with three kinematic mounts.

A more detailed view of the kinematic mounts is shown in Figure 36. The mounts provide a 3-2-1 constraint system which should allow repeatable installation to within a few microns.

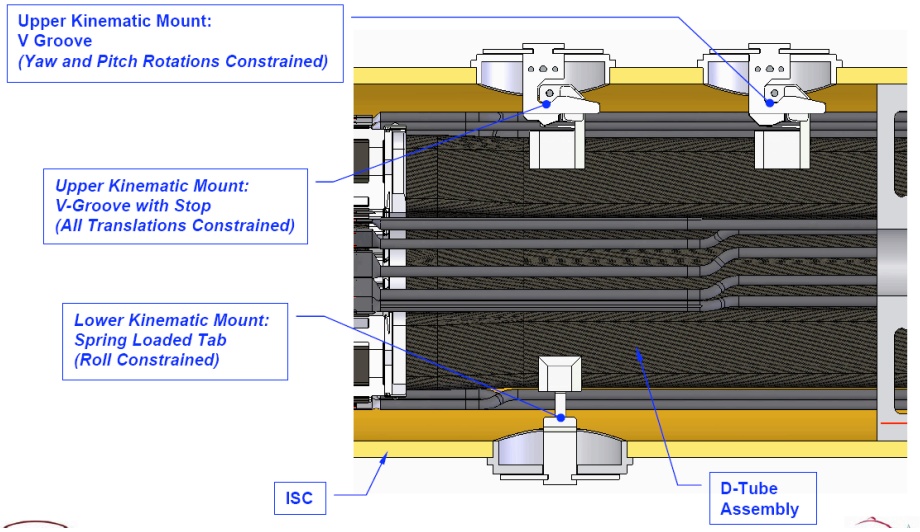


Figure 36: Detailed view of the kinematic docking mounts for the PXL detector. The mounts provide a fully constrained support and operate with a spring loaded over center lock down.

Insertion Mechanism and Installation

The mechanics have been designed for rapid installation and replacement. Installation and removal of the pixel detector will be done from outside of the main STAR detector with minimum disruption to other detectors systems. This will be done by assembling the two halves of the detector on either side of the beam pipe on rails outside of the STAR magnet iron. The detector carriage will be pushed into the center of STAR along the rails until it docks on the kinematic mounts. As shown in Figure 37 and Figure 38, the hinged support structure is guided by cam followers to track around the large diameter part of the beam pipe and close down at the center into the final operating position. Once the detector is docked in the kinematic mounts the hinged support from the carriage is decoupled allowing the kinematic mounts to carry the light-weight detector system with a minimum of external forces affecting the position of the detector barrels. The external loads will be limited to the cables and the air cooling ducts. The cables are loosely bundled twisted pairs with 160 micron conductor plus insulation, so this load should be minimal. The two inch cooling ducts will be the greater load and may require additional design effort to isolate their effect so that the 20 micron position stability for the pixels can be maintained.

Cooling system

Cooling of the detector ladders with pixel chips and drivers is done with forced air. The pixel chips dissipate a total of 160 watts or 100 mW/cm^2 and an additional 80 watts is required for the drivers. In addition to the ladder total of 240 watts some fraction of this is required for voltage regulators and latch up electronics that are off the ladder but reside in the air cooled volume. The temperature of operation is still under consideration. An optimum temperature for the detectors is around 0 deg C, but they can be operated at 34 deg C without too much noise degradation. The cooling system design is simplified if we can operate at 24 deg C, slightly above the STAR hall temperature; however if a cooler temperature is required, the cooling system will be equipped

with thermal isolation and condensation control when the system is shut down. In any case the design will include humidity and temperature control as well as filtration. Cooling studies (see Appendix 1) show that air velocities of 8 m/s are required over the detector surfaces and a total flow rate of 200 cfpm is sufficient to maintain silicon temperatures of less than 12 deg C above the air temperature.

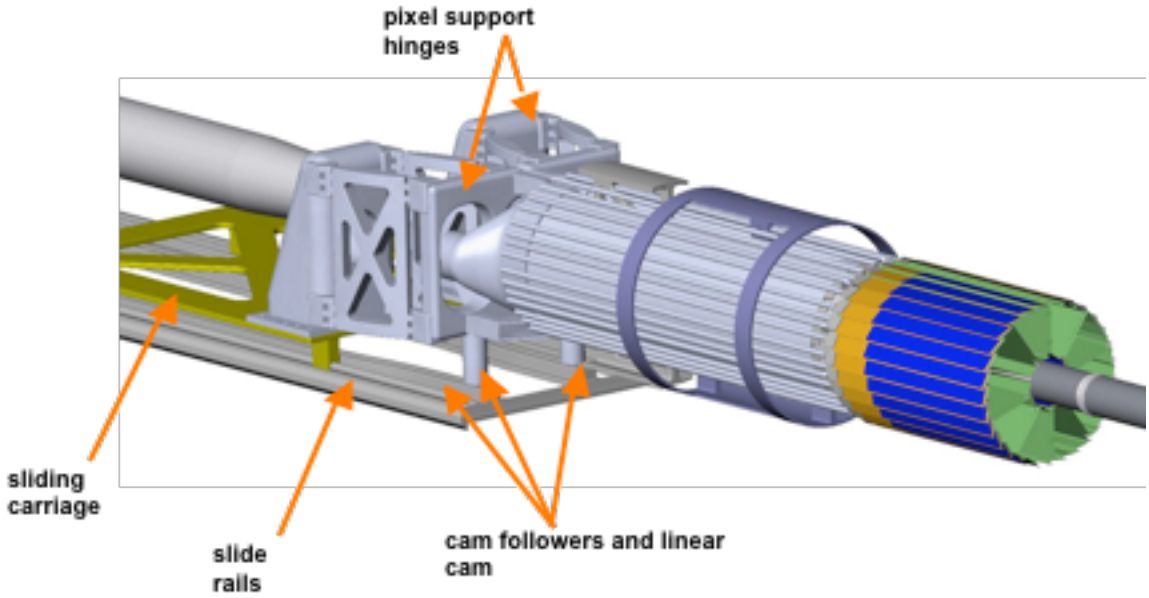


Figure 37: Track and cam guide system for inserting the detector.

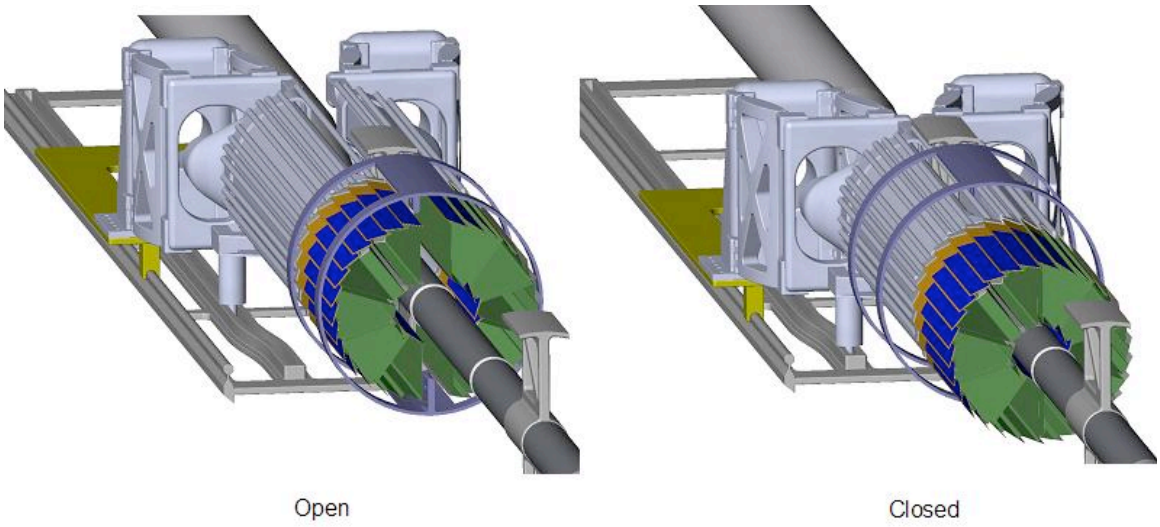


Figure 38: Initially the detector halves have to be sufficiently open to clear the large diameter portion of the beam pipe. It then closes down sufficiently to fit inside the Inner Field Cage (IFC) while clearing the beam pipe supports and then finally it closes down to the final position with complete overlapping coverage of the barrels.

The detector cooling path is shown in Figure 39. Air is pumped in through the support beam. A baffle in the ISC forces the air to return back over the detector surfaces both along the beam pipe and along the ISC.

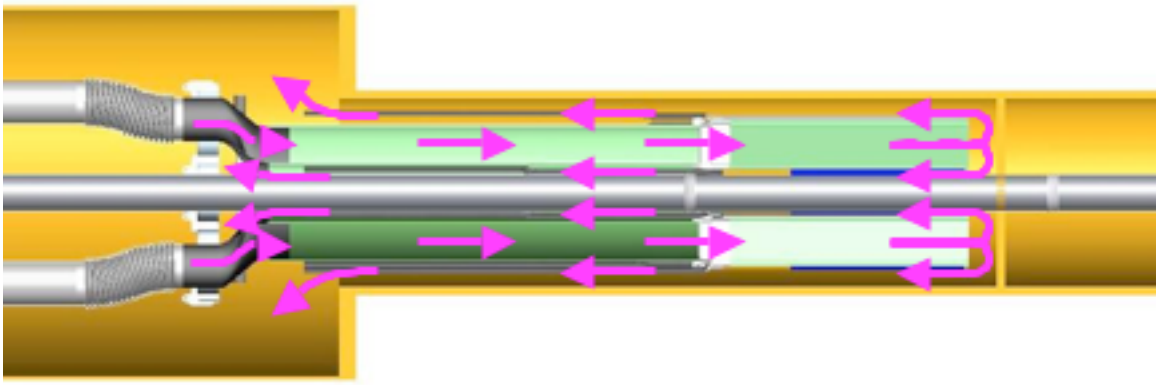


Figure 39: PXL detector cooling air path. The air flows down the center of the sector modules and returns back over the detector ladders on the sector modules and into the larger ISC volume where it is ducted back to the air cooling unit.

The air chiller system providing the cooling air circulating through the PXL detector has not been completely specified yet, but sizing and ducting have been investigated for a system (see Figure 40) with 400 cfpm capacity (twice the currently expected requirement). A commercially available centrifugal pump with a 5 horsepower motor is sufficient for this system. It is expected that the chiller will be located in the Wide-angle Hall within 50 ft of the pixel enclosure and will be connected with 6 inch flexible ducts. An estimate of the required chiller heat capacity is given in Table 10.

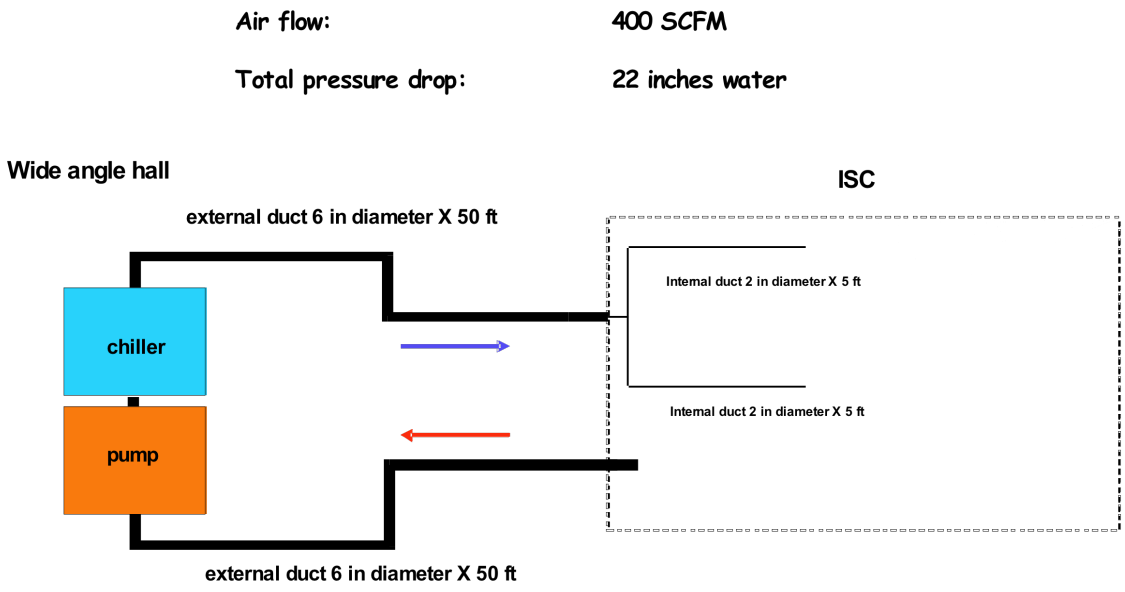


Figure 40: Schematic outline of air cooling system for the PXL detector.

Cabling and Service System

The required wiring connections are identified in Figure 44. The 2 m fine wire twisted pair (pair diameter .32 mm) bundles leading from the ladders to the interface cards are designed to minimize mass, space and mechanical coupling forces that could disturb the pixel positions. The space envelope required for these bundles is illustrated in Figure 41.

Heat source	Power (watts)
Detector silicon	160
On-ladder signal drivers	80
Voltage regulators in ISC	24
Heat influx through ducting and ISC if 35 deg C below ambient	600 - 2000
Pumping	1000
Total load on chiller	1900 - 3300

Table 10: Preliminary estimate of heat load on the chiller for the PXL air cooling system.

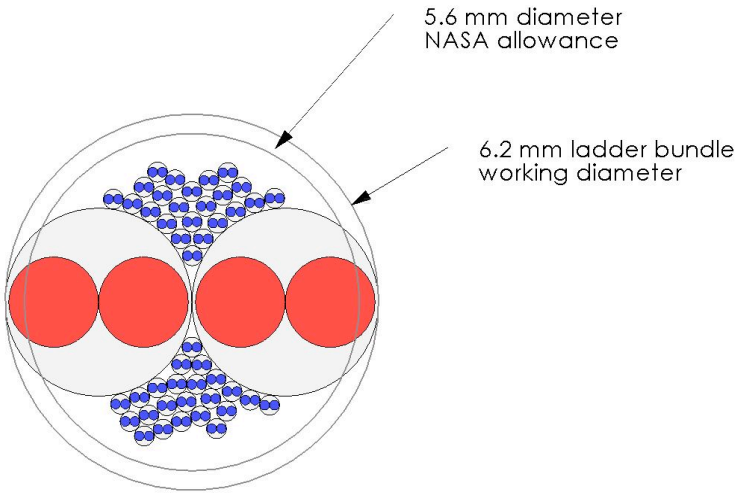


Figure 41: Cable bundle envelope for the ladder connections. The blue pairs include 40 signal pairs, clock and trigger lines and JTAG communication. The red conductors are for power.

There will be a 2'x2'x3' crate for the readout boards. This must be located outside of the main magnetic field and outside of the highest particle flux region. To achieve the required data transfer rates the LVDS signal cables running between this crate and the drivers inside the ISC are limited to 6 meters. To meet these constraints the readout crate will be located on the floor of the hall at the end of the magnet (there is no space on the magnet end ring for mounting the readout box). This will allow for the operation of the PXL system both with and without the pole tip in place. The crate will be portable on wheels to accommodate end cap access requirements. Compared to the cables running to the detector, the power and fiber optic cables from the readout crate to the outside world are relatively small and provide little handling burden.

Alignment and Spatial Mapping

The PXL system is being designed to have full pixel-to-pixel spatial mapping at installation with a 3D tolerance envelope of 20 microns. This will eliminate the need for spatial calibration with tracking other than to determine the 6 parameters defining the PXL detector unit location relative

to the outer tracking detectors. Tracking, on the other hand, can use the PXL detector to spatially map the outer detectors, if required.

Using a vision coordinate machine to determine the detector locations on the fully constructed ladder half modules will do the mapping and alignment. A full 3D map of the ladders is necessary since the manufactured ladder flatness will exceed the 20 micron envelope. After mapping, the half modules will be installed in STAR without disturbing the relative positions of the pixels.

Addressing this in more detail, a support fixture for the half modules will be used in the vision coordinate machine, which has kinematic mounts identical to the kinematic mounts in the ISC for securing the half module. The pixel chips will be manufactured with reference targets in the top metal layer that can be picked up by the vision coordinate machine and the ladders will be mounted such that there is an unobstructed view. The fixture will be rotated for each ladder measurement. Full 3D measurements of the chips on the ladder are required since the ladder flatness will lie outside of the 20 micron envelope. The fixture will have precision reference targets on each ladder plane so that the ladder points can be tied together into a single coordinate frame. The map of the fixture targets can be measured once with a touch probe measuring machine and thus avoid extreme machining tolerance requirements for the fixture. Precision machining, however, will be required, for the kinematic mounts and their placement tool.

For this approach to work the ladders must hold to their mapped position within 20 microns independent of changes in temperature, humidity and gravity direction. Since the detector ladders have 1 mm overlapping active regions with their neighbors, a check of the mapping accuracy will be done with tracking.

Detailed information on mechanical design simulation and prototyping may be found in Appendix 1.

4.2.4. Sensors and Readout

Sensor Development

We approach the design of the electronics for the PXL detector as a two stage development process with the readout system requirements tied to the stages of the sensor development effort. The sensor development is taking place at the Institut Pluridisciplinaire Hubert Curien (IPHC) in Strasbourg, France, where we are working in collaboration with Marc Winter's group. In the current development path, the first set of prototype sensors to be used at STAR will have digital outputs and a 640 μs integration time. We will use these sensor prototypes to construct a prototype sector for deployment in the STAR detector. This prototype system will employ the mechanical design to be used for the final PXL detector as well as a readout system that is designed to be a prototype for the expected final system. We will also test the final PXL sensors with a full scale prototype.

Monolithic Active Pixel Sensor Development at IPHC

The sensor development path for the PXL detector sensors is tailored to follow the development path of the technology as it was set by the IPHC group. In this path, the Monolithic Active Pixel Sensors (MAPS) with analog multiplexed serial analog outputs in a rolling shutter configuration are envisioned as the first generation of sensors followed by a more advanced final or Ultimate sensor that has digital outputs. The analog MAPS have been produced and tested and our sensor

development path will soon move to digital binary readout from MAPS with fine-grained threshold discrimination, on-chip correlated double sampling (CDS) and a fast serial LVDS readout. A diagram showing the current development path, with the attendant evolution of the processing and readout requirements, is shown in Figure 42.

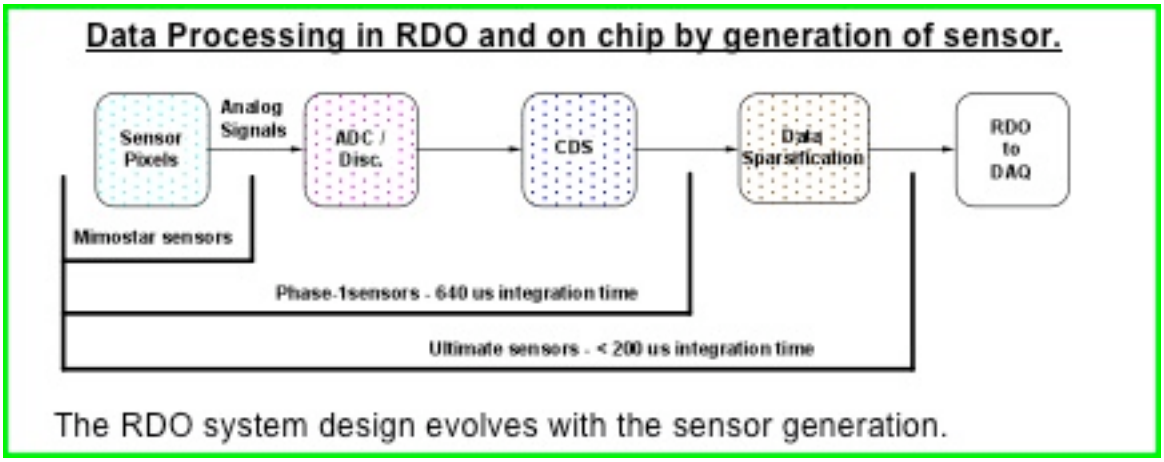


Figure 42: Diagram showing the sensor development path of sensors for the STAR PXL detector at IPHC in Strasbourg. The readout data processing required is shown as a function of sensor generation.

The Mimostar series sensors are the first generation of sensors that have been fabricated and tested. These are 50 MHz multiplexed analog readout sensors with 30 μm × 30 μm pixels in variously sized arrays depending on generation. This generation has been tested and characterized and, with the exception of some yield issues, appears to be well understood. Testing with these sensors is described in Reference [43].

The next generation sensor has been named “Phase-1”. This sensor is based on the Mimosa-8 and Mimosa-16 sensor technology and contains on-chip correlated double sampling and column level discriminators providing digital outputs in a rolling shutter configuration. The Phase-1 sensors are full sized 640 × 640 arrays resulting in a full 2 cm × 2 cm sensor. In order to achieve a 640 μs integration time, the Phase-1 sensor is equipped with four LVDS outputs running at 160 MHz.

The final sensor is named “Ultimate”. The Ultimate sensor includes all of the attributes of the Phase-1 sensor with the pixel sub-arrays clocked faster to give a < 200 μs integration time. The pixel size has been reduced to 18.4 μm × 18.4 μm to increase the sensor radiation tolerance in the higher luminosity RHIC II environment. The Ultimate sensor also includes run length encoding based on a data sparsification and zero suppression circuit. There are two data output lines from the sensor and the data rates are low thanks to the newly included data sparsification circuitry. The first prototype sensors of this design are expected to be ready in the 2010 time frame.

Sensor Series Specifications

The specifications of the sensors under development are shown in Table 11. The Phase-1 sensor is a fully functional design prototype for the Ultimate sensor, which results in the Phase-1 and Ultimate sensors having very similar physical characteristics. After successful development and testing of the Phase-1 sensors, a data sparsification system currently under development at IPHC will be integrated with the Phase-1 design. Finally, the Ultimate sensor will include an enhancement allowing for faster clocking of the sub-arrays.

	Phase -1	Ultimate
Pixel Size	30 μm × 30 μm	18.4 μm × 18.4 μm
Array size	640 × 640	1024 × 1088
Active area	~ 2 × 2 cm	~ 2 × 2 cm
Frame integration time	640 μs	100 – 200 μs
Noise after CDS	10 e^-	10 e^-
Readout time / sensor	640 μs	100 – 200 μs
Outputs / sensor	4	2
Operating mode	Column parallel readout with all pixels read out serially.	Column parallel readout with integrated serial data sparsification.
Output type	Digital binary pixel based on threshold crossing.	Digital addresses of hit pixels with run length encoding and zero suppression. Frame boundary marker is also included.

Table 11: Specifications of the Phase-1 and Ultimate sensors.

In addition to the specifications listed above, both sensors will have the following additional characteristics:

- Marker for the first pixel in an array.
- Register based test output pattern JTAG selectable for binary readout and troubleshooting.
- JTAG selectable automated testing mode that provides for testing pixels in automatically incremented masked window to allow for testing within the overflow limits of the zero suppression system.
- Independent JTAG settable thresholds.
- Radiation tolerant pixel design.
- Minimum of 3 fiducial marks per sensor for optical survey purposes.
- All bonding pads located along one side of the sensor.
- Two bonding pads per I/O of the sensor to facilitate probe testing before sensor mounting.

Architecture for the Phase-1 Sensor System

We have designed the prototype data acquisition system to read out the large body of data from the Phase-1 sensors at high speed, to perform data compression, and to deliver the sparsified data to an event building and storage device.

The requirements for the Phase-1 prototype and final readout systems are very similar. They include:

- Triggered detector system fitting into the existing STAR infrastructure and to interface to the existing Trigger and DAQ systems.
- Deliver full frame events to STAR DAQ for event building at approximately the same rate as the TPC (~ 1 KHz for the STAR DAQ1000 upgrade).
- Reduce the total data rate of the detector to a manageable level (< TPC rate).

The proposed architecture for the readout of the Phase-1 prototype system is shown in Figure 43 with the physical location and separation of the system blocks shown in Figure 44.

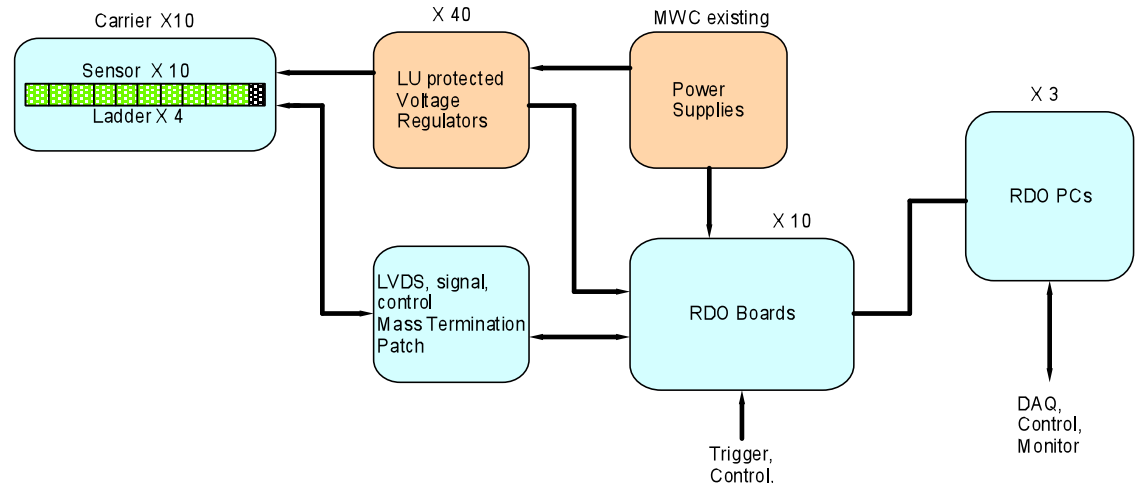


Figure 43: Functional block schematic for the readout for the Phase-1 prototype system. The detector ladders and accompanying readout system have a highly parallel architecture. One system unit of sensor array / readout chain is shown. There are ten parallel sensor array / readout chain units in the full system.

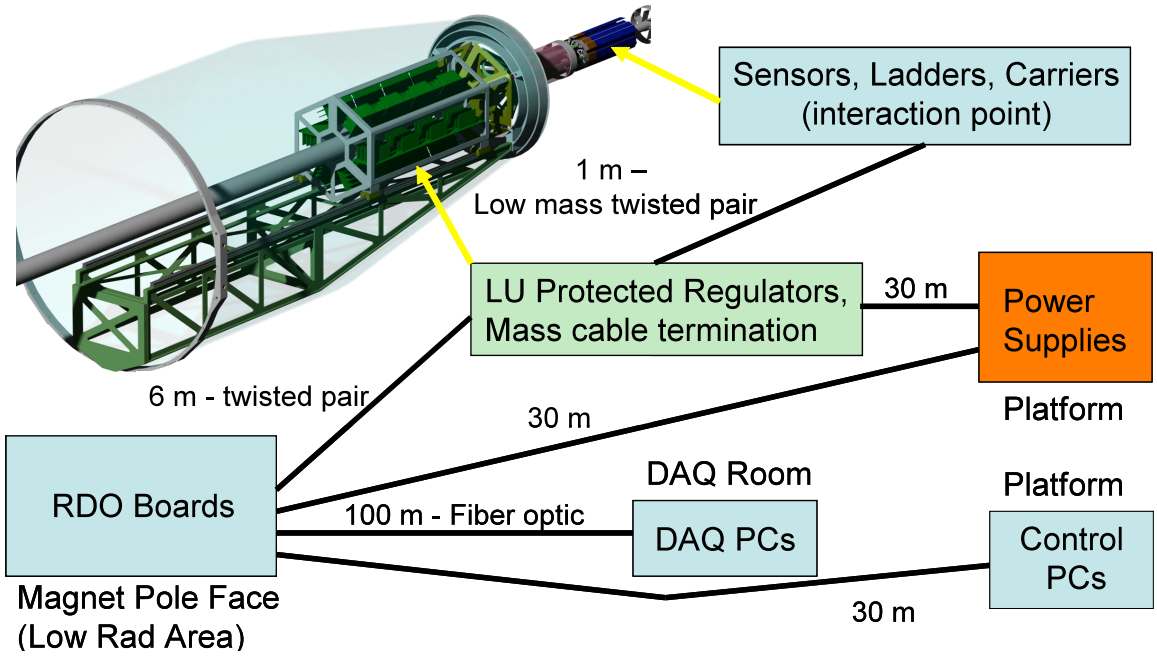


Figure 44: Physical layout of the readout system blocks. This layout will be the same for both the Phase-1 based patch and the final PXL detector system.

The architecture of the readout system is highly parallel. Each independent readout chain consists of a four ladder mechanical carrier unit (a sector) with each ladder containing ten Phase-1 sensors. The current plan is to install a patch of Phase-1 sensors consisting of at least two sectors mounted with the final mechanical positioning device and located 120 degree apart.

The basic flow of a ladder data path starts with the MAPS sensors. A PXL ladder contains 10 Phase-1 MAPS sensors, each with a 640 × 640 pixel array. Each sensor contains four separate digital LVDS outputs. The sensors are clocked continuously at 160 MHz and the digital data containing the pixel threshold crossing information is read out, running serially through all the pixels in the sub-array. This operation is continuous during the operation of the Phase-1 detectors on the PXL ladder. The LVDS digital data is carried from the four 160 MHz outputs in each sensor in parallel on a low mass flex printed circuit board to discrete LVDS buffers located at the end of the ladder and out of the low mass detector region. This portion of the ladder also contains the buffers and drivers for the clocks and other control signals needed for ladder operation.

Each Phase-1 sensor requires a JTAG connection for register-based configuration, power, ground, a 160 MHz readout clock and a synchronization signal to start the readout. These signals, the latch-up protected power, as well as the LVDS outputs and synchronization and marker signals from the detectors are carried via low mass twisted pair cables from the discrete electronics at the end of the ladder to a power / mass termination board located approximately one meter from the PXL ladders. There is one readout board per PXL sector (40 sensors). A diagram of a ladder is shown in Figure 45.

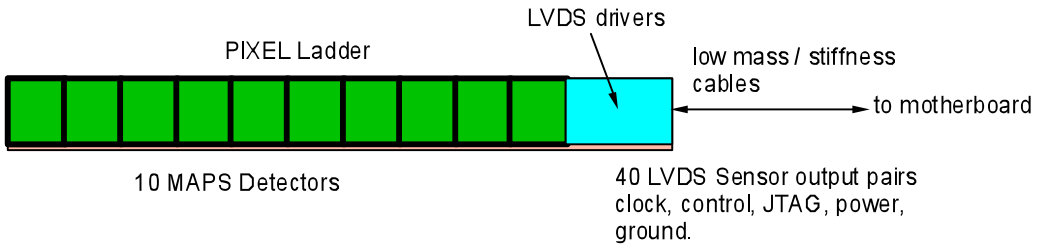


Figure 45: Assembly of sensors on a low radiation length Kapton flex cable with aluminum conductors. The sensors are connected to the cable with bond wires along one edge of the ladder.

The flex cable parameters are:

- 4 layer - 150 micron thickness
- Aluminum Conductors
- Radiation Length ~ 0.1 %
- 40 LVDS pair signal traces
- Clock, JTAG, sync, marker traces.

The connection to the driver end of the ladders will be made with a very fine 150 μm diameter twisted pair wire. These wires will have very low stiffness to avoid introducing stresses and distortions into the mechanical structure. The other ends of these fine twisted pair wires will be mass terminated to allow connection to the Power & Mass-termination (PM) board located approximately one meter away.

Latch-up protected power is provided to the sensors from the PM boards. Each ladder has independently regulated power with latch up detection circuitry provided by a daughter card that plugs into the PM board. There are four regulation and latch-up daughter cards per PM board and a total of 10 PM boards are needed for the complete detector system readout. A block diagram for the PM board is shown in Figure 46.

The digital sensor output signals will be routed, along with a 160 MHz clock signal, to the PM board and then to the readout boards (RDO). The RDOs will be mounted in a movable electronics rack located on the cave floor. Each location is approximately 6 meters away from the PM boards and Si sensors. A diagram describing the attributes of the two circuit boards that

make up the RDO system can be seen in Figure 47. A functional block diagram of the RDO can be seen in Figure 48.

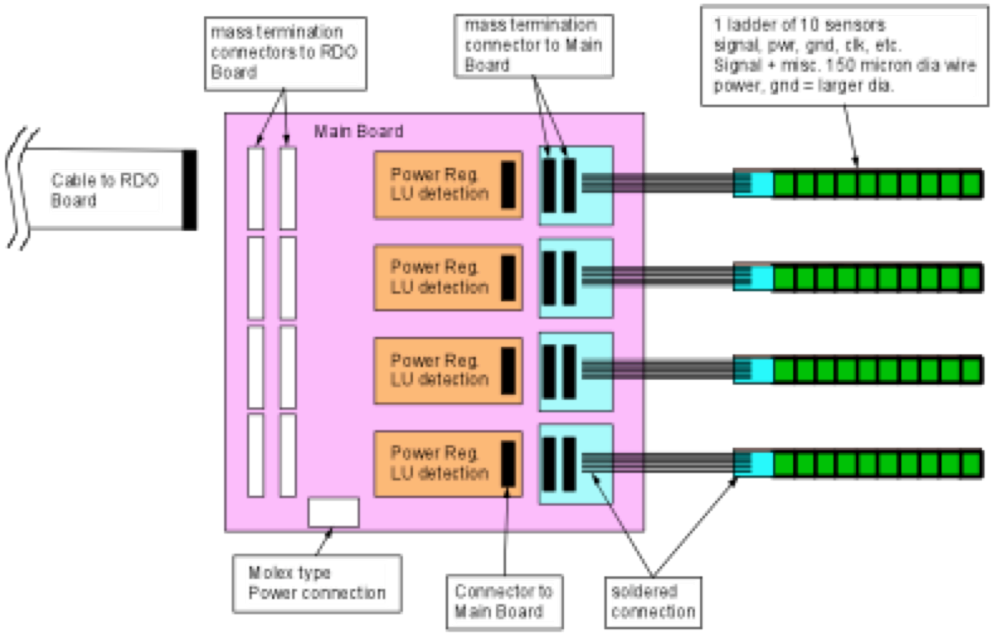


Figure 46: Power and mass-termination board block diagram. The digital signals to and from the sensors are routed through the main board and are connected to the readout boards via the mass termination connectors on the main board. Latch-up protected power regulation is provided to each ladder by a daughter card mounted to the main board. The main power supplies will be located far from the detector (in the STAR racks).

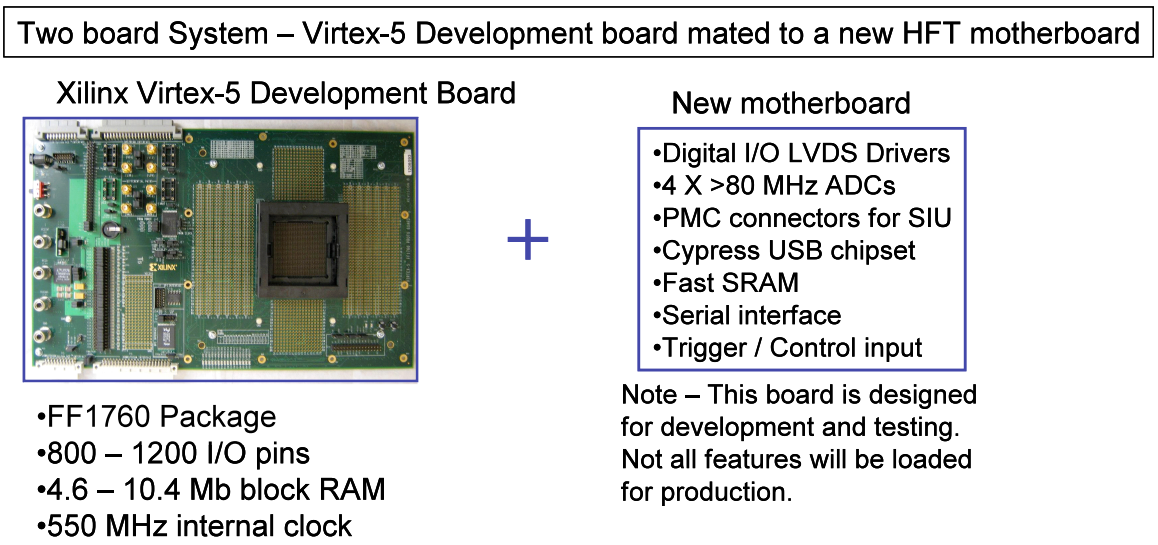


Figure 47: Readout board. The readout system consists of two boards per sector of 40 sensors. A commercial Xilinx Virtex-5 development board is mated to a custom motherboard that provides all of the I/O functions including receiving and buffering the sensor data outputs, receiving the trigger from STAR, and sending the built events to a STAR DAQ receiver PC via a fiber optic connection.

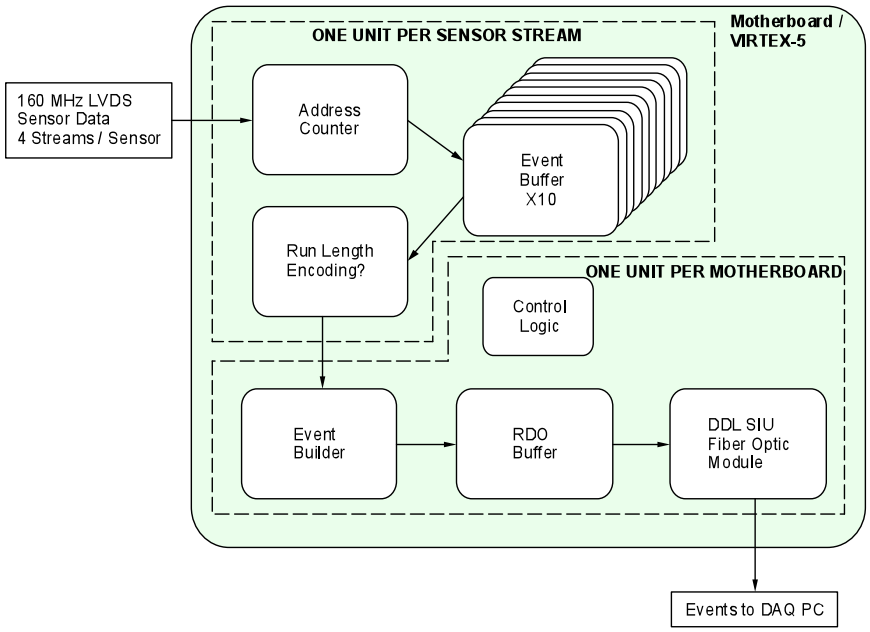


Figure 48: Functional block diagram of the data flow on the RDO boards.

The RDO boards are based on a fast Xilinx Virtex-5 FPGA development board, which is mated to a custom motherboard. The motherboard provides several functions, including LVDS buffering into the FPGA, a STAR trigger input, PMC connectors for mounting a fiber optic Detector Data Link (DDL), SRAM, and various ADCs and I/O connectors to be used in testing the board.

The data processing path takes several steps. First, the sensor output signals are buffered and then fed into the FPGA. In the FPGA the data is re-sorted to give a raster scan, after which the location of pixels with hits are converted to pixel addresses using an address counter. Zero suppression is achieved by the conversion of hits to addresses in a relatively low multiplicity environment and this is the main mechanism for data reduction used in the readout system. The efficiency and accidentals rate for a simple threshold circuit on each pixel is shown in Figure 49.

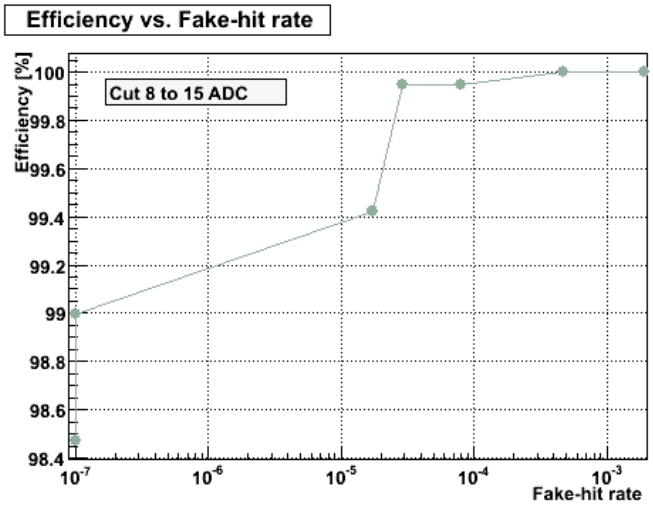


Figure 49: Efficiency versus fake hit rate for a simple threshold cut on signal level. The figure is obtained from live-beam data taken with the Mimostar-2 sensors.

When a trigger is received, one of a bank of event buffers is enabled for one frame of data (409,600 pixels). After the frame has been recorded in the event buffer, the results of that frame are sent to an event builder. The event builder gathers all of the addresses on the RDO and builds them into an event, which is then passed via fiber optic links to the STAR DAQ receiver PCs.

We intend to use the Source Interface Unit (SIU) and Readout Receiver Cards (RORC) developed for ALICE as our optical link hardware to transfer data to and from the STAR DAQ system. These links have been chosen as the primary readout connections for the new STAR TPC FEE. Leveraging existing hardware and expertise in STAR allows for a faster and more reliable design than developing our own custom solution.

The complete readout system consists of a parallel set of sector readouts (4 ladders per sector) with ten separate readout chains. A system level functionality block diagram is shown in Figure 50.

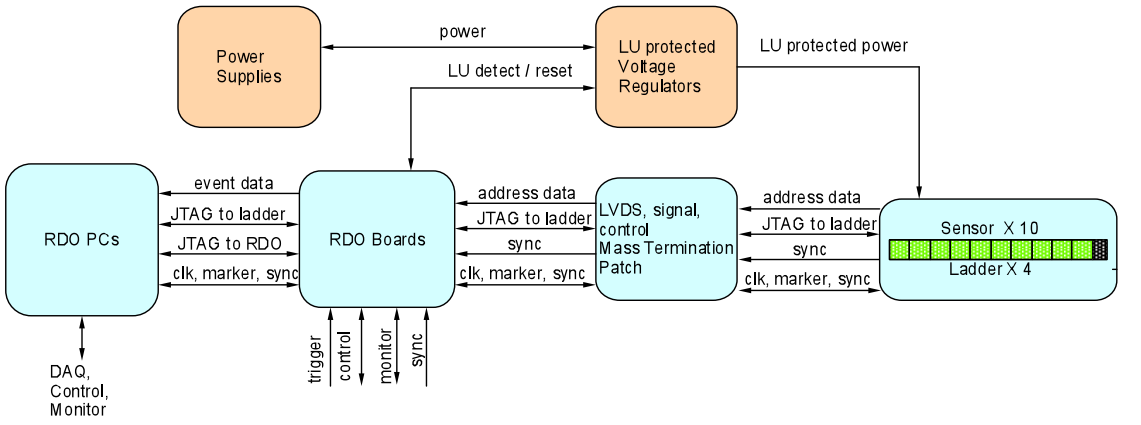


Figure 50: System level functionality diagram of the readout of the PXL sensors. One of the ten parallel readout chains is shown.

Data Synchronization, Readout, and Latency

The Phase-1 PXL sensors are read out continuously. Hit-to-address processing is always running during the normal operation of the detector. The PXL will receive triggers and the STAR clock via the standard STAR Trigger and Clock Distribution module (TCD). The receipt of a trigger initiates the saving of the found hit-addresses into an event buffer for one frame (409,600 pixels). The PXL detector as a whole will be triggered via the standard STAR Trigger Clock Distribution (TCD) module. Since 640 μs is required to read out a complete frame of interest, the data will be passed to DAQ for event building about 640 μs after the trigger is received. We will provide for multiple buffers that will allow us to capture temporally overlapping frames of data. This will allow us to service multiple triggers within the 640 μs readout time of the sensor. In this system, the hit address data is fanned out to ten event buffers. A separate event buffer is enabled for the duration of one frame upon the receipt of a trigger from the TCD. Subsequent triggers enable additional event buffering until all of the event buffers are full and the system goes busy. The resulting complete frames are then passed to the event builder as they are completed in the event buffers. This multiple stream buffering gives a system that can be triggered at a rate above the expected average rate of the STAR TPC (approximately 1 kHz). Furthermore, since the addition of buffers is external to the sensors, the capability for the addition of large amounts of fast SRAM will be included in the RDO board design allowing for flexibility in our readout system configuration. This multiple event buffer architecture will result in the duplication of some data

in frames that overlap in time. However, our data rate is low and the duplication of some data allows for contiguous event building in the STAR DAQ, which greatly eases the offline analysis. In addition, synchronization between the ladders/boards must be maintained. We will provide functionality to allow the motherboards to be synchronized at startup and any point thereafter.

Triggering Considerations

The primary tracking detector of the STAR experiment is the TPC with the Heavy Flavor Tracker upgrade designed to add high-resolution vertex information. The PXL detector is part of a larger group of detectors that make up the HFT upgrade at STAR. The other tracking detector components of the HFT include the Silicon Strip Detector (SSD) and the Intermediate Silicon Tracker (IST). Since the HFT is a system of detectors, in order to maximize efficiency, the trigger response and dead time characteristics of each detector in the HFT system should be matched, as much as possible, to the others. As the main detector, the post DAQ-1000 TPC sets the effective standard for the other detectors in the system. In the current understanding of the system, the PXL detector information is only useful in conjunction with the external tracking detectors and thus the PXL detector will only be triggered when the TPC is triggered.

The triggers in STAR are produced randomly with a 107 ns crossing clock spacing. The behavior of the TPC is to go dead for 50 μs following the receipt of a trigger. This means that the TPC, and by extension the PXL detector, will receive random triggers spaced by a minimum of 50 μs. An additional constraint is imposed by the fact that the TPC data acquisition system contains 8 buffers at the front end. This allows for the capability of the TPC to take a quick succession of 8 triggers (separated by 50 μs) but then the TPC will go busy until the data has been transferred and buffers cleared. The time required for this depends on the event size. Some of these numbers can be found at http://drupal.star.bnl.gov/STAR/daq1000-capabilities. Other statistics about DAQ1000 are private communication with the STAR DAQ group (Tonko Ljubicic). This behavior provides the basis for the assessment of the trigger response characteristics of the detectors in the HFT system. In general, the HFT detector readout system will provide for the acquisition of up to 8 successive triggers separated by 50 μs with some, as yet uncharacterized, clearing time. The goal is to have the HFT detectors "live" whenever the TPC is "live". In Appendix 2 we show an analysis of the trigger response characteristics of the PXL detector.

System Performance for the Phase-1 Prototype Sensor System

The raw binary data rate from each Phase-1 sensor is 80 MB/s. For the 400 sensors that make up the PXL detector this corresponds to 32 GB/s. The raw rate must clearly be reduced to allow integration of the PXL data stream into the overall STAR data flow. Zero suppression by saving only addresses of hit pixels is the main mechanism for data volume reduction. The parameters used to calculate the data rates are shown in Table 12.

Based on the parameters given above, the average data rate (address only) from the sensors in the prototype Phase-1 detector is 237 kB per event which give an average data rate of 237 MB/s. It is possible to reduce the data rate further using a run length encoding scheme on the addresses as they are passed from the event buffer to the event builder as indicated in Table 12. We are currently investigating this option, though the data rate reduction from this approach is expected to be moderate. The raw data rate reduction from the hit-pixel to address conversion is shown graphically in Figure 51.

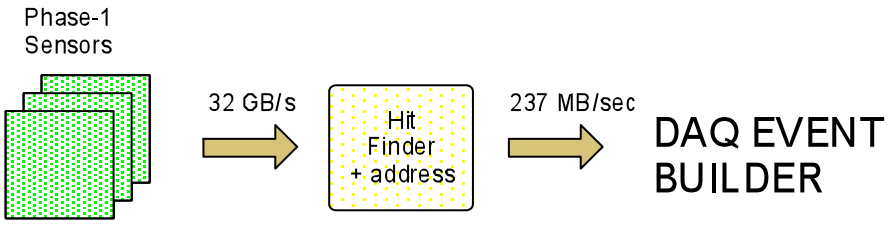


Figure 51: Data rate reduction in the Phase-1 readout system.

Bits per address	20
Integration time	640 μs
Luminosity	3×10^{27}
Hits per frame on inner sensors (r = 2.5cm)	295
Hits per frame on outer sensors (r = 8.0cm)	29
Sensors inner ladders	100
Sensors outer ladders	300
Average pixels per cluster	2.5
Average trigger rate	1 kHz

Table 12: Parameters used to calculate data rates from a Phase-1 based system.

Architecture for the Ultimate Sensor System

The most significant difference between the Phase-1 and Ultimate sensors is the inclusion of zero suppression circuitry onboard the sensor. The ultimate sensors provide zero suppressed sparsified data with two LVDS output lines per sensor. Another difference between the Phase-1 and Ultimate sensors is that the pixel size for this final production sensor is reduced to 18.4 μm. This is useful because a smaller pixel has a shorter charge collection time making it more radiation tolerant. In addition, the sub-frame arrays are clocked faster to give a < 200 μs integration time and a frame boundary marker is added to the data stream to allow for the demarcation of frame boundaries in the absence of hits in the sensor and to allow for synchronization with the RDO system. The upgrade from the Phase-1 to the Ultimate sensors in the system is expected to involve the fabrication of new sensor ladders using the same mechanical design used in Phase-1 but using the new Ultimate series sensors and a redesign of the Kapton readout cable. The Kapton cable for the Ultimate sensor will require significantly fewer traces (20 LVDS pairs instead of 40) for readout and the new cable design should have a lower radiation length. The task of reading out the Ultimate series sensors is actually less challenging than the readout of the Phase-1 sensors since the data reduction functionality is included in the sensor.

The readout hardware described above for the Phase-1 readout system remains the same for the Ultimate readout system. Some reconfiguration of the functionality in the FPGA is required for readout of the Ultimate sensor PXL detector but that is all done in the software. A functional block diagram for the RDO boards is shown in Figure 52.

The Ultimate sensor operates in the same rolling shutter readout mode as the PHASE-1 sensor. The address data, which is clocked out of the Ultimate chip has well defined latencies that we will use to keep track of triggered frame boundaries and which can be verified using synchronization markers from the sensors. For example, the first pixel marker from the sensor corresponds to the actual scan of pixels through the sensor and the frame boundary marker delineates frame

boundaries in the sparsification system on the sensor. Using this information and knowing the internal latencies in the sensor, we can generate the internal logic in the FPGA to implement the same multiple buffering technique that was previously described.

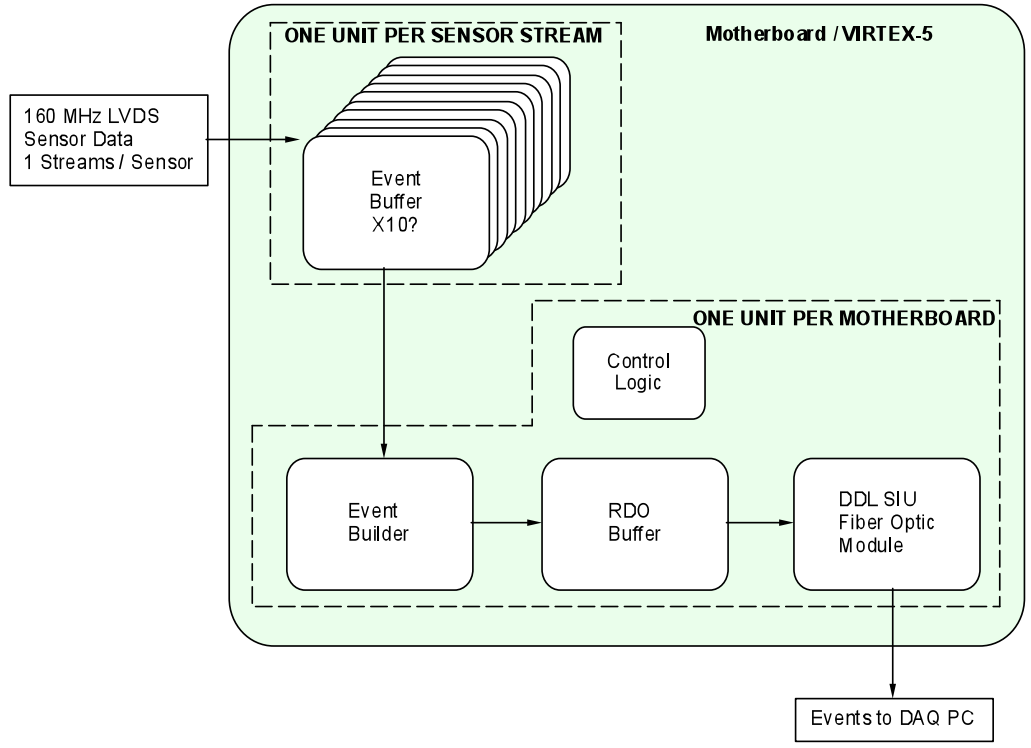


Figure 52: Functional block diagram of the RDO boards for the readout of the Ultimate detector based PXL detector.

System Performance for the Ultimate Sensor System

The parameters used to calculate the data rates for the system are shown in Table 13. From these parameters, we calculate an average event size of 209 kB giving an address data rate of 209 MB/s from the Ultimate sensor based PXL detector. A more detailed analysis of the readout chain including parameters for the size of buffers and a discussion of the internal FPGA functions are included in Appendix 2.

Bits per address	20
Integration time	200 μs
Luminosity	8×10^{27}
Hits per frame on inner sensors (r=2.5cm)	246
Hits per frame on outer sensors (r=8.0cm)	24
Sensors inner ladders	100
Sensors outer ladders	300
Average pixels per cluster	2.5
Average trigger rate	1 kHz

Table 13: Parameters used to calculate data rates from an Ultimate sensor based system.

4.2.5. Sensors and Readout Simulation and Prototyping

Mimostar-2 based Telescope Test at STAR

Using a preliminary system design for the analog readout, we have taken data with a set of Mimostar-2 sensors at STAR. This system is an early prototype whose performance is evaluated as part of the overall vertex detector development effort. We have successfully implemented a continuous readout using a 50 MHz data acquisition system with on-the-fly data sparsification that gives nearly three orders of magnitude data reduction compared to the raw ADC rates. The readout system was mated with a prototype Mimostar2 sensor and configured in a telescope geometry to measure the charged particle environment in the STAR environment near the PXL detector position. The detector telescope is shown in Figure 53.

Figure 53: Three Mimostar-2 sensors in the telescope configuration used in the beam test at STAR.

We found that the system worked well, gave reasonable efficiency and accidental hit rates, and measured an angular distribution of tracks consistent with imaging the interaction diamond and with imaging a beam-gas interaction type background. The prototype readout system integrated well into the existing STAR electronics and trigger infrastructure and functioned successfully as any another STAR detector subsystem. The prototype readout system and the results have been published in NIM.[43]

LVDS Data Path Readout Test

The readout system architecture for the Phase-1 and Ultimate sensors contains a high-speed digital data path that is required to read out the sensor hits during the sensor integration time. The RDO sensor data interface path requires that LVDS data move over a total distance of 6 to 8 meters at a rate of 160 MHz for Phase-1 and 125 MHz for Ultimate. 1 to 2 meters of this distance is over high impedance fine twisted pair wire. Since the design is challenging, though it works on paper, we though it would be prudent to make a prototype set of test boards and check the performance of our design as a precursor to starting a production design for the final set of

readout boards. We have completed making a complete set of test boards for one basic block of the highly parallel RDO system consisting of a functional ladder mockup, mass termination board prototype and a limited functionality RDO motherboard coupled to a Xilinx Virtex-5 Development board. The test was successful with bit error rates of approximately 10^{-15} for the configuration and clock speed needed for the detector. A report on this test may be found in Appendix 3.

4.2.6. Engineering Prototype

As an important milestone in the HFT construction we have scheduled an engineering prototype run with the PXL configuration shown in Figure 54. An engineering run with the HFT PXL detector serves a number of important functions that are required in the development of a robust detector system capable of producing useful physics in a timely fashion. Some functions address resolution of questions that could affect or require modification of the final design. Other functions address the need to get an early start on hardware and software commissioning.

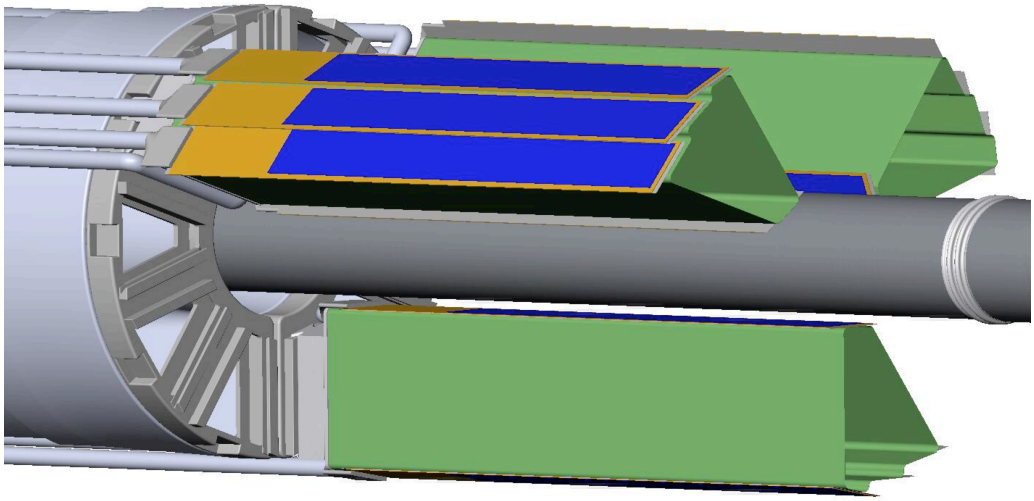


Figure 54: Proposed PXL configuration for the engineering prototype.

The engineering run will be the first opportunity to run a detector at such a small radius and verify our estimates of the electron background generated in ultra-peripheral collisions. The background levels affect the optimum operation of the final detector chip, namely the tradeoff between read out speed (integration time) and power dissipation. The outcome of this issue could result in modification of cooling and mechanical support rigidity. This is not something that could be addressed on the fly. The time between the engineering run and the final installation would be sufficient to take corrective actions if required.

The engineering run will provide a test for vulnerability to wakefield generated noise or other unanticipated noise sources. We don't expect this to be an issue with our detector design, but if the engineering run exposes a problem then RF shielding would be implemented.

Every effort is being made to insure that the HFT PXL detector will meet the requirements of mechanical stability while operating in the STAR environment. However, if the engineering run reveals difficulties resulting from unanticipated issues with the STAR environment then they can be addressed before operation with the completed HFT detector.

The PXL detector electronics system, detector plus read out, will be tested with the STAR DAQ and trigger system prior to the engineering run so integration complications are not expected, but the engineering run could reveal unexpected issues with pickup or grounding associated with DAQ connections that would require correction prior to the complete HFT operation.

The engineering run will test software for detector alignment through tracking so that good working software is available at the start of operation of the complete HFT detector system. The engineering run will be an important time for commissioning this software as well as other software systems such as slow controls and various diagnostic software tools. There are many such functions that will require testing and correction that can be accomplished only through actual operation. Experience has repeatedly and painfully shown that bringing up a new detector system in a collider environment is a daunting task with many time conflicting activities which are still all essential to proper operation. It is important to recognize this and design an engineering run to provide an ordered approach to commissioning the detector.

The limited detector coverage designed for the engineering run is being configured to provide some capability for D meson detection so there is some hope that some physics can be accomplished, but the overriding goal of the engineering run will be system verification and correction.

4.3. The Intermediate STAR Tracker

The Intermediate Silicon Tracker (IST) consists of a barrel of silicon pad sensors at a radius of 14 cm. The sensors are supported by 24 carbon fiber ladders, which are tiled for maximum hermiticity. Figure 55 shows a SolidWorks model of the IST. Table 14 gives the most relevant specifications.

Radius	14 cm
Length	50 cm
Number of ladders	24
Number of hybrids	72
Number of sensors	144
Number of readout chips	864
Number of channels	110592
R-ϕ resolution	172 μm
Z resolution	1811 μm

Table 14: Specifications for the IST.

The best figure-of-merit for the tracking capabilities is the final D^0 reconstruction efficiency. Determining this efficiency involves extensive GEANT simulations and analysis. A fast simulation code was used to determine the optimum radius of the IST barrel and the internal geometry of the silicon pad sensors.

4.3.1. Requirements

The most relevant experimental constraints are data taking rate capabilities, radiation levels and the material budget. The data rate and radiation levels are constrained by the RHIC environment

and have to be taken into account in the sensor and readout chip choice. The material budget is connected to the tracking capabilities of the inner tracking system, but has also a large impact on the capabilities of more outward located detectors and their associated physics programs. The requirement to design a low mass IST with sufficient mechanical rigidity has led to the choice of state-of-the-art materials.

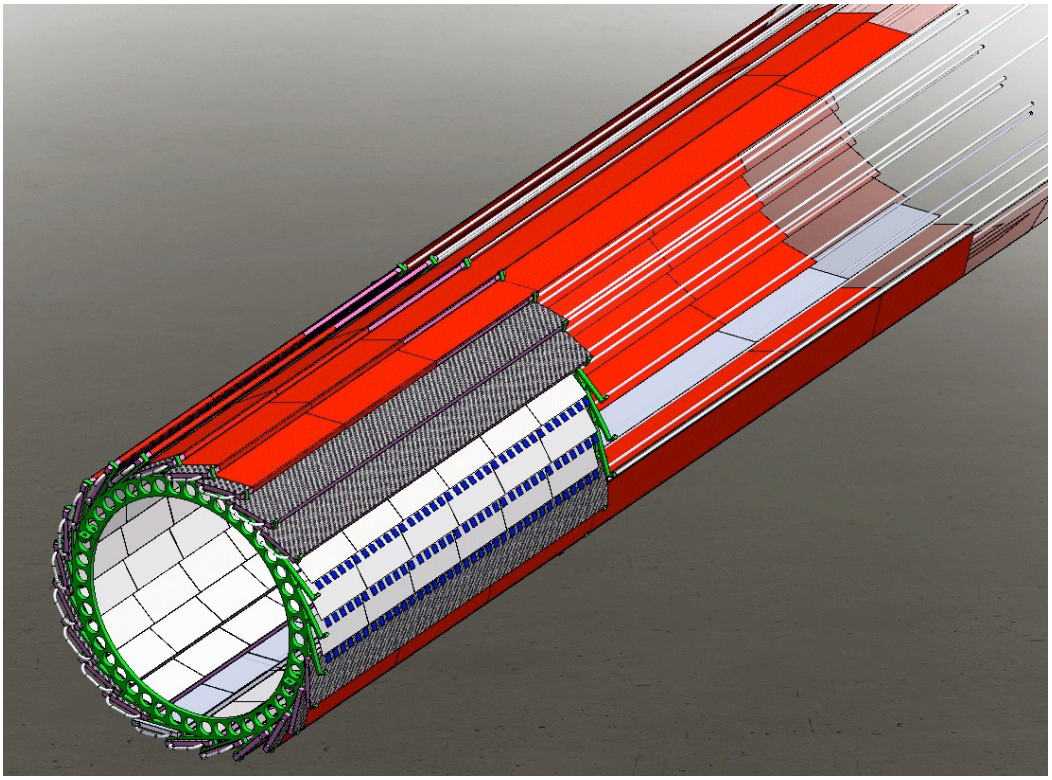


Figure 55: SolidWorks model of the IST.

The IST should be able to operate without significant event pile-up for 200 GeV Au+Au collisions. Therefore, the IST has to be able to resolve interactions from each beam bunch crossing which are occurring every 107 ns. The spin program at RHIC relies on individual beam bunch crossings to set and determine the relative spin orientations in the proton beams. Also here the IST has to be able to resolve individual beam bunches.

The intrinsic resolution of the IST is required to provide sufficient pointing accuracy for the PXL layers. This is more critical in R-ϕ compared to the Z direction. A resolution at the level of 200 μm in the R-ϕ plane will provide the needed pointing accuracy as discussed earlier.

Extrapolating the radiation doses received by the RHIC experiments during the past RHIC operations, it is expected that the total radiation dose for the IST barrel will not exceed 30 kRad per year. Both the silicon sensors and the readout chips on the hybrids are required to be fully operational after 10 years of operation.

The mass requirements for the IST are defined by the heavy ion physics requirements in the mid-rapidity region and by the W–boson spin physics program for more forward rapidities. To make the multiple Coulomb scattering comparable to the detector resolution the thickness of the IST layer has to be less than or equal to 1.5% of a radiation length.

4.3.2. Design Choices

IST Radius and Sensor Geometry

The Intermediate Silicon Tracker is located between the outer layer of the PXL detector and the SSD. Taking mechanical constraints into account a possible radius range is from 12 to 20 cm. This radius has to be optimized for reconstruction efficiency while keeping the SSD and IST redundancy in mind. The IST barrel will cover the full acceptance of the STAR TPC, i.e. 2π coverage for $-1 < \eta < +1$.

At the highest RHIC energy of 200 GeV for Au+Au collisions the charged particle density at a radius of 12 cm can easily exceed one per cm^2. The silicon sensors need to be divided into pads such that the occupancy of the individual pads do not exceed a few percent. The occupancy is fully determined by the number of active elements and can be reached by different sensor geometries. What has to be taken into account is the double-hit probability within the search area on the IST sensors resulting from the pointing resolution of the TPC and SSD. Figure 56 shows the occupancy of a sensor with 768 active elements and the fraction of hits that are accompanied by one or more hits in the search area. In the case of a silicon strip detector the search area is defined by the width of the search area and the length of the strips. At the proposed radius of 14 cm more than 10% of the tracks would result in ambiguous IST hits. For the proposed silicon pad sensors this drops to about 1%. The number of active elements is determined by the density with which the readout chips can be packed on the hybrids.

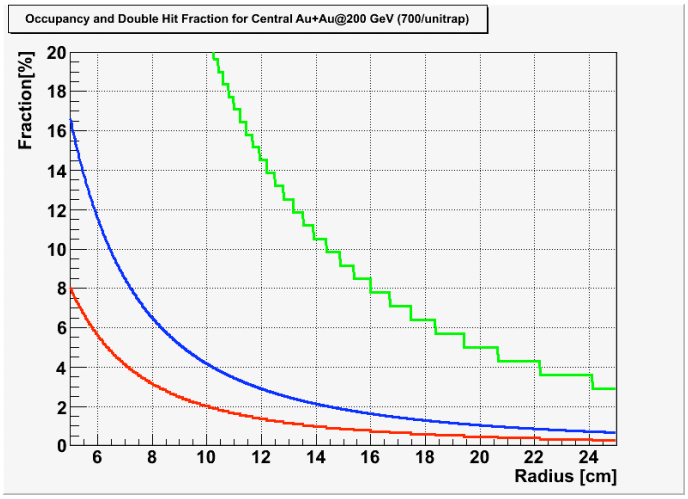


Figure 56: Occupancy [blue curve] and double-hit fraction for a silicon strip detector [green curve] and a silicon pad sensor [red curve].

Silicon pad sensors are well suited to the RHIC environment and proved their suitability in the PHOBOS experiment. Figure 57 shows a study of the single track finding efficiency of the HFT as a function of the pad layout of the IST sensors. The better resolution (the size of the pads on the y-axis) is in R-ϕ, the bending plane. From these studies it was determined that 768 channels arranged in strips of roughly 600 μm x 6000 μm provide an efficiency of about 83%. Going to more channels could give a slightly better efficiency but would lead to space problems when trying to mount more readout chips on the hybrids. The right plot shows the efficiency when hits from the SSD are not included in the tracking. In this case the single track finding efficiency decreases to 73%. This has to be compared to 50% if the IST would not be there and only the

TPC would provide tracking to the PXL. Thus, the IST adds in an essential way to the efficiency and redundancy of the HFT.

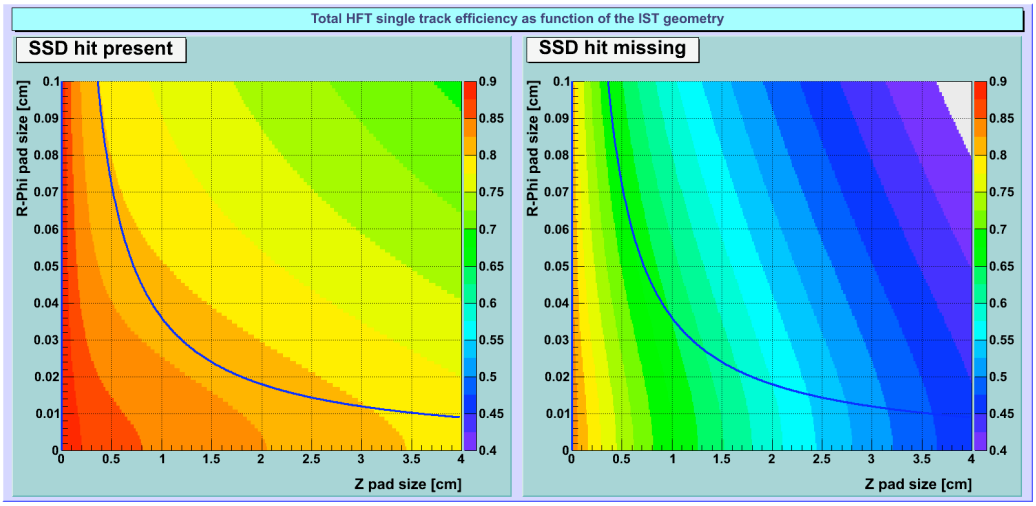


Figure 57: Single track finding efficiency for different R-ϕ and Z pad sizes of the IST. The solid line shows an iso-line for 768 readout channels. The left panel shows the efficiency when hits from the SSD are included. In the right panel the SSD hits are not included in the track. Particles tracked are kaons at 750 MeV/c.

The efficiency of the whole inner tracking system is determined by an intricate interplay of the detector layer radii, resolutions and thicknesses. Since these characteristics are mostly fixed for PXL and SSD, varying the radius of the IST barrel for a certain internal sensor geometry makes it possible to optimize the radius with respect to the single track efficiency quickly. Figure 58 shows a calculation of the single-track efficiency as a function of the IST barrel radius. Although the dependence is rather weak it is clear that 14 cm will give the best efficiency. This can be understood from the fact that IST is located roughly halfway between the outer layer of the PXL and the SSD.

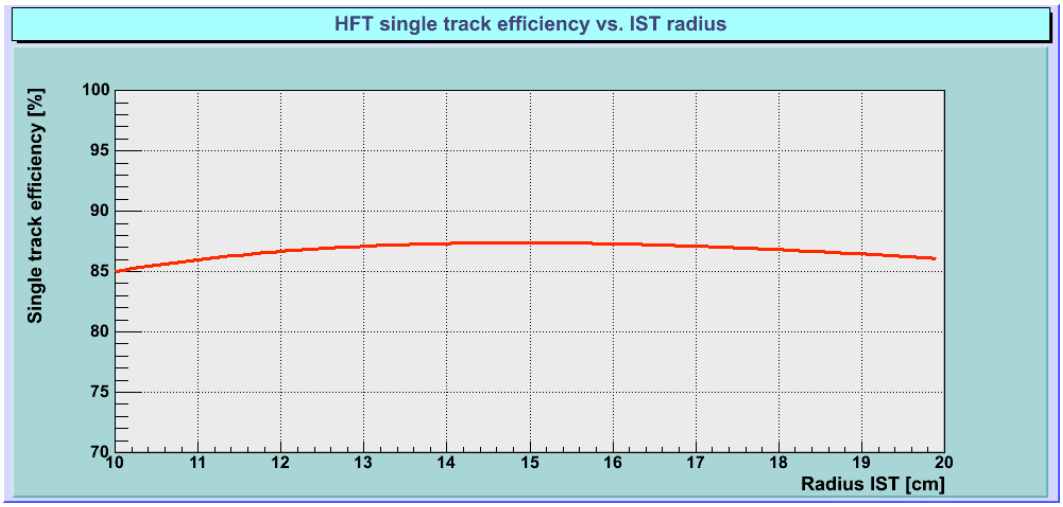


Figure 58: Single-track efficiency as a function of the IST barrel radius. The assumed internal sensor geometry was 600 µm in R-ϕ and 6000 µm in Z.

Readout Chips

The APV25-S1 chip was chosen for reading out the IST sensors because it met the requirements and is readily available. This readout chip was developed for the CMS silicon tracker, which is using about 75,000 of these chips. The radiation hard production process of the APV25-S1 will enable to withstand at least 2 orders of magnitude more in radiation load compared to what is expected to be accumulated during the lifetime of the IST. The chip is fast enough to handle the RHIC interaction clock, even with multiple interactions during p+p running. Moreover, the chip is already used successfully for reading out the COMPASS triple-GEM detectors and will also be used to read out the STAR Forward GEM Tracker (FGT).

Hybrids and Ladders

To meet the requirement of the IST to have on average a thickness of less than 1.5% X_0, special attention has to be paid to the choice of materials for the hybrids, cables and ladders. For the cables Kapton with copper conductors was chosen. Although aluminum conductors would make the cables even lighter, they also would make them more difficult to produce and much more fragile. The radiation length requirement makes it not desirable to use a ceramic substrate, like AlN, for the hybrid. A 500 µm thick AlN substrate would already contribute 0.6% X_0 while being extremely fragile. A 250 µm thick G10 substrate would only add 0.13% X_0, but still the Kapton cable would have to be connected to this hybrid. Manufacturing the hybrid and cable out of one piece of Kapton circumvents connection problems and was chosen as the most elegant solution. Since the 50 μm thick Kapton is not self-supporting a proper supporting material is required. Using 250 μm thick carbon fiber leads to a thickness of 0.11% X_0 while providing the required mechanical rigidity.

A honeycomb carbon fiber structure with carbon fiber skins was chosen for the IST ladders. These use the same construction techniques and facilities as used for the ATLAS silicon tracker upgrade and add about 0.4% X_0 to the IST layer, including liquid cooling. Copying the ATLAS design in the same facility greatly reduces the engineering effort and cost of the ladders. Also, since the IST ladders are only half the length (50 cm) of the ATLAS ladders, the design is conservative with respect to strength and gravitational sag.

Cooling

The expected heat dissipation for the IST is 11 W per ladder, 264 W for the whole system. Although an air cooling system probably will be able to cool the IST, it is felt that a liquid cooling system will be able to perform this function in a more consistent way. A liquid cooling system will add at most 0.2% X_0 to the system.

Readout System

The Forward GEM Tracker is also using APV25-S1 readout chips. This system will be operational 2 years before the IST. In order to reduce the electronic engineering effort and to unify as many STAR readout systems as possible, the IST will use as much as possible of the FGT readout system. An effort is being made to design the FGT readout system such that it can be used also for the IST with as few alterations as possible.

4.3.3. The Silicon Pad Sensors

The manufacturing techniques for silicon sensors are well established and are mastered by several manufacturers. The preference is to produce single sided devices with p-implants on n-bulk silicon using poly-silicon resistors. Such sensors are relatively easy to produce with high yield and can also be handled without much difficulty in a standard semiconductor lab. In contrast, double-sided devices have a lower yield (thus more expensive) and need special equipment to handle them.

Figure 59 shows the internal layout of the IST silicon pad sensors. The active elements are arranged in such a way that the best resolution is in the bending direction, i.e. R-ϕ. Along the beam direction, the resolution will be ten times larger. The sensors will be roughly 7.7 cm x 4 cm with 768 channels. All channels are AC coupled and connected through a second metal layer to bonding pads on one long edge of the sensor. From the manufacturing point of view this design is reasonably standard. Preliminary discussions with Hamamatsu showed that they are able to produce such sensors within the proposed budget.

Hamamatsu is the preferred vendor because of their excellent track record with respect to the quality of their produced sensors. This will greatly reduce the amount of quality control that has to be performed for these sensors. It will be sufficient to fully measure the characteristics of one or two samples per produced batch of about 20 sensors. Moreover, Hamamatsu uses design rules, which make their sensors radiation hard. Therefore, we foresee no performance degradation during the expected IST lifetime.

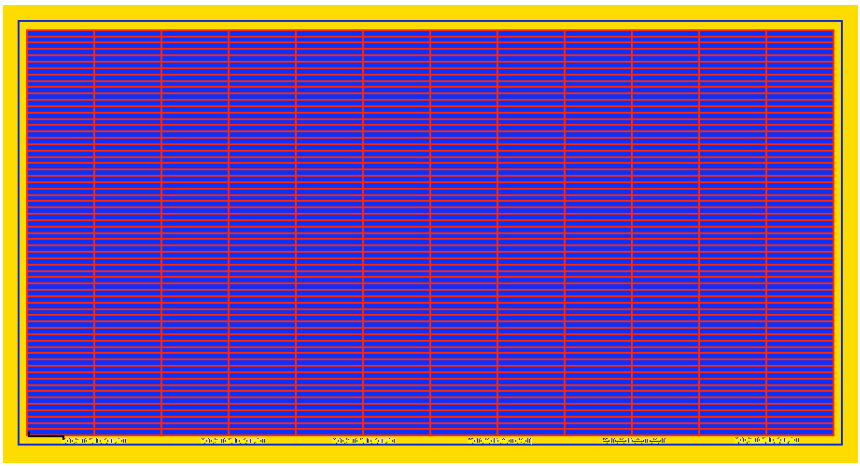


Figure 59: The silicon pad sensor internal layout.

4.3.4. The Readout Chips

About 100k channels will be read out in the IST. Readout chips with the necessary requirements for this system are already being used for similar purposes by other experiments. We chose the APV25-S1 readout chip.[44] Each channel of the APV25-S1 chip consists of a charge sensitive amplifier and shaper whose output signal is periodically sampled at up to 40 MHz (the LHC interaction rate). The samples are stored in a 4 μs deep analog pipeline. Following the trigger, the data in the pipeline can be processed by an analog circuit, mainly de-convoluting the amplifier response from the actual signal and associating the signal with a specific bunch crossing. The resulting analog data can then be multiplexed and sent to digitizer boards. Although the analog

data lead to higher data volumes at the front-end, it is an advantage that charge-sharing between strips and common mode noise can be studied in detail, which greatly improves the understanding and performance of the detector. The equivalent noise charge (ENC) of the APV25-S1 depends on the capacitance of the strips and the de-convolution algorithm used. For our purposes, the noise is better than 2000 electrons. With 300 μm thick silicon sensors this will give a signal-to-noise ratio of better than 11:1 based on the most probable energy deposition by a minimum ionizing particle (MIP). The nominal power consumption of the APV25-S1 chip is 2.39 mW per channel, i.e. about 0.3 W per chip. The chips have been fabricated in a radiation hard deep sub-micron (0.25 µm) process.

4.3.5. Hybrids and Modules

The layout of an IST module can be seen in Figure 60. The hybrid carries 2 sensors and 12 readout chips. There will be a gap of 400 µm between the sensors. Overlapping the sensors would lead to complications in the assembly process. These acceptance gaps will be compensated because of the redundancy between SSD and IST. An interesting feature, which is not visible in this picture, is that the cable will be folded over to the backside of the ladder on which this module will be mounted. In this way the cables do not obscure visual access to the modules, which is needed for spatial survey purposes and inspection.

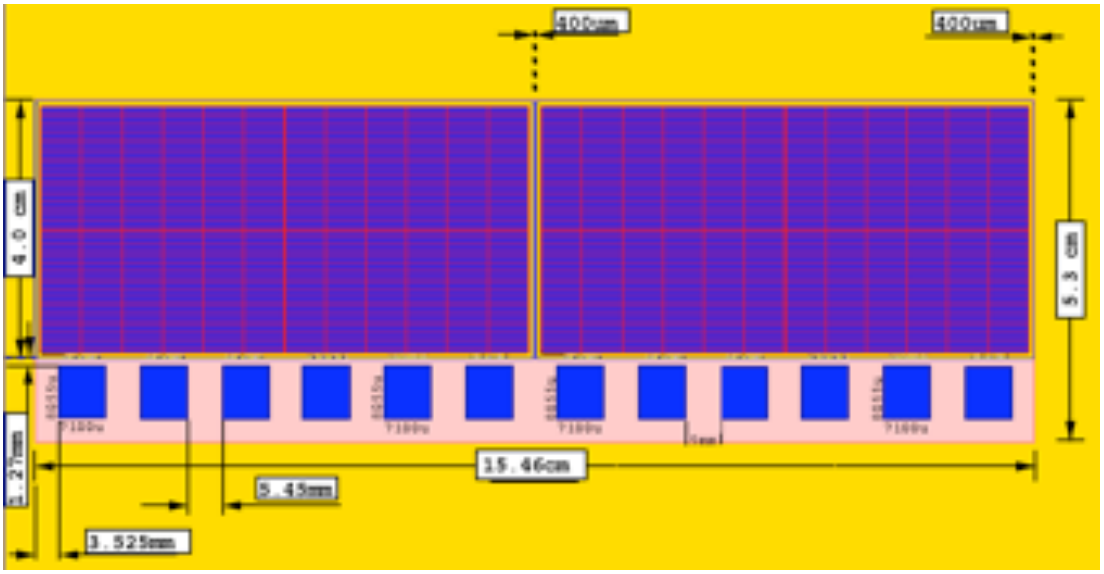


Figure 60: Layout of an IST module.

To keep the material budget low the IST hybrids and modules have to be constructed from low mass materials. Figure 61 shows a promising prototype Kapton hybrid design with an integrated long Kapton cable. Both hybrid and cable are about 70 μm thick. The hybrid will have to be laminated onto a proper substrate material to achieve enough mechanical rigidity. Carbon-carbon and carbon fiber are being prototyped to study their mechanical and thermal properties. In the final design the flexible cable will be long enough to be connected to more standard cables outside the active area.

For this prototype four PHOBOS Inner Vertex sensors were used because there were no IST prototype sensors produced yet and because the PHOBOS sensors are very close to the sensors used in the IST. The PHOBOS sensors are silicon pad sensors with 512 active elements per

sensor, the elements are AC coupled to the 2nd metal signal traces that connect to the bonding pads. The Kapton hybrid was laminated to a 500 µm thick carbon-carbon substrate. Power, control and readout connections were wire bonded to the hybrid. As a first test only ¼ of the sensor elements were wire bonded to the readout chips. First tests show that the chips are functional and that the sensors are being read out as expected.

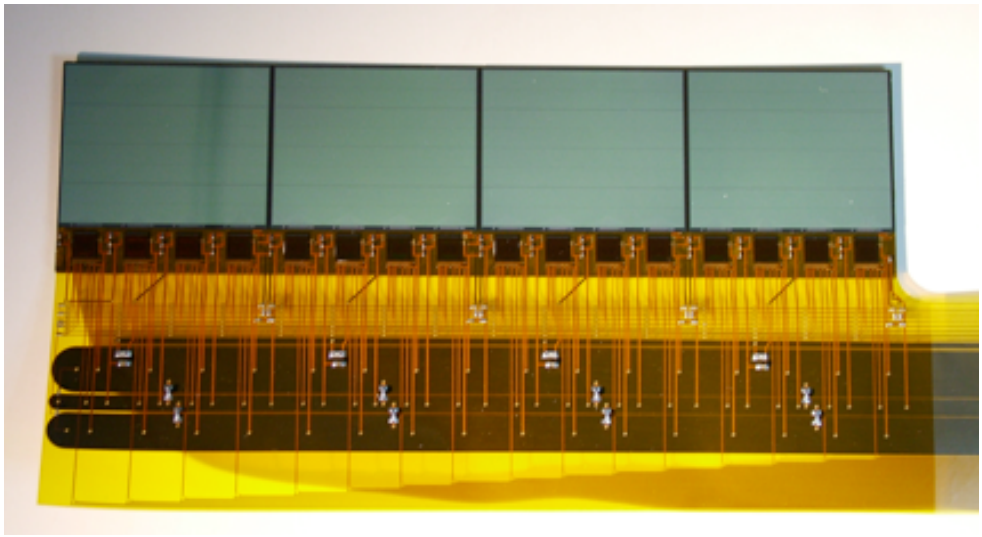


Figure 61: IST prototype with 4 PHOBOS IV sensors and 16 APV25-S1 readout chips.

4.3.6. Mechanical Support Structure

The IST barrel will consist of 24 ladders, which are mounted on a carbon fiber support cylinder. This Middle Support Cylinder (MSC) is described in Section 4.5.1.

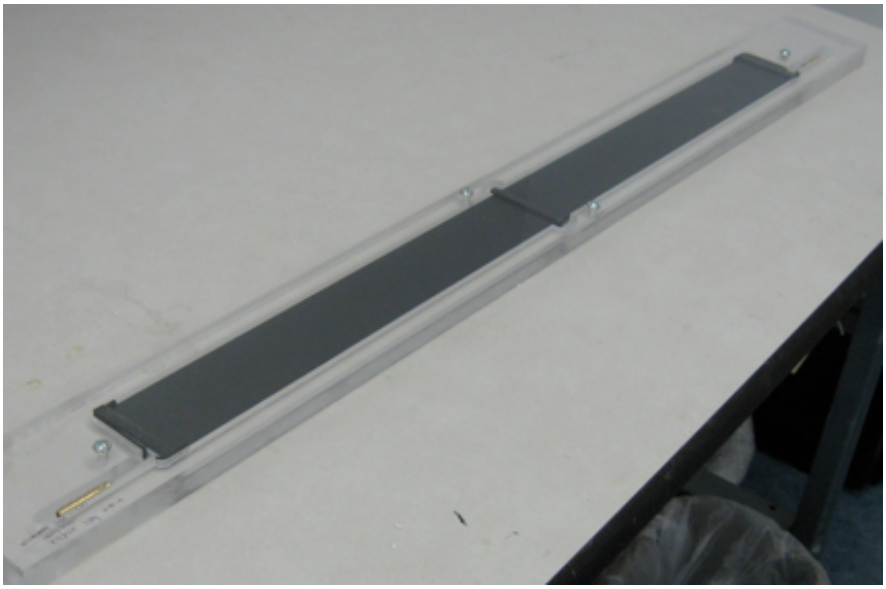


Figure 62: Long IST prototype ladder made out of carbon fiber honeycomb and carbon fiber skins. This prototype has one cooling channel.

This ladder is a shorter version of the staves under development for the ATLAS tracking upgrade. Because they are shorter they are even more rigid than the ATLAS staves and it is expected that their midpoint sag will be less than 100 µm when only end supports are used. A prototype ladder has been produced, as shown in Figure 62, and is being tested.

A more detailed cross-section of the ladder and mounted modules can be found in Figure 63. This design shows the 300 µm thick silicon sensor, the 300 µm thick APV25-S1 readout chip, the 100 µm thick Kapton hybrid-cable, the 500 µm thick carbon-carbon substrate and the 5 mm thick carbon fiber ladder with cooling tube. It also shows nicely how the Kapton hybrid folds over to the backside of the ladder where it is routed out to the readout system. The carbon-carbon substrate not only gives mechanical rigidity to the module, but also acts as a heat sink to transport heat from the readout chips to the cooling tube in the ladder.

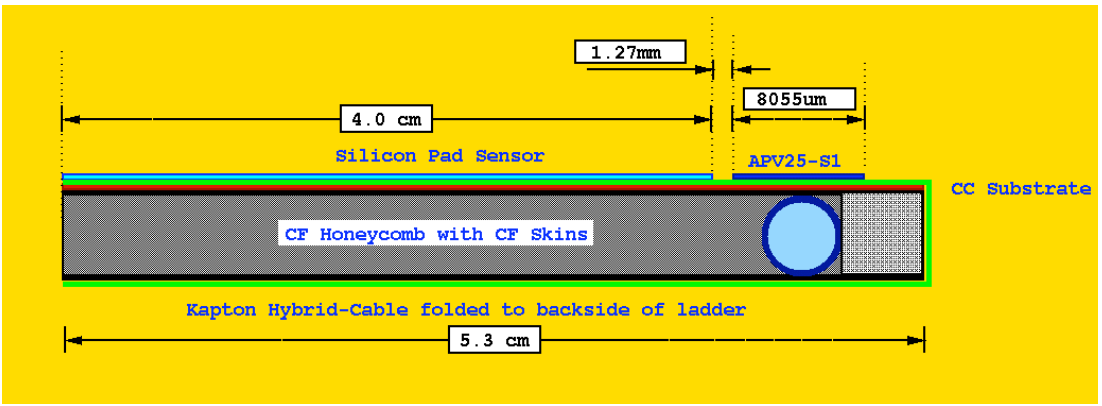


Figure 63: Cross-section of the ladder and modules. The Kapton hybrid shown in green is folded over to the back side.

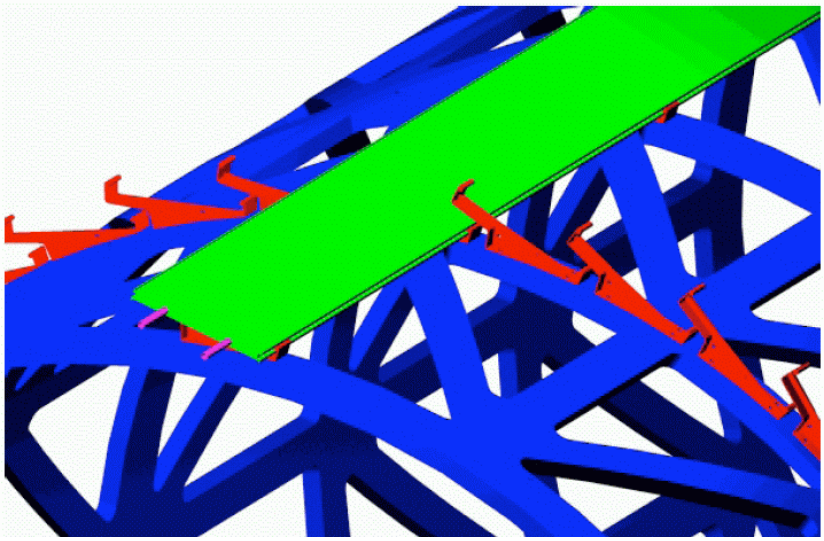


Figure 64: Ladder 'clip' mounting of the IST ladders onto the supporting cylinder (ISC).

It is expected that the ladder mounting scheme will follow the ATLAS upgrade design efforts. Figure 64 shows a schematic impression of the ATLAS mounting scheme. Here the ladders are mounted with clips on the MSC. Because of the shorter length of the IST ladders it is sufficient to use endpoint supports only. One end of the ladder would be kept fixed while the other end

allows thermal expansion. A clamshell interface is required on which the ladders are mounted first. This clamshell can then be optically surveyed to determine the sensor positions before it is being mounted on the ISC.

A prototype of this clip-on design has been prepared, as shown in Figure 65, and is currently under investigation.

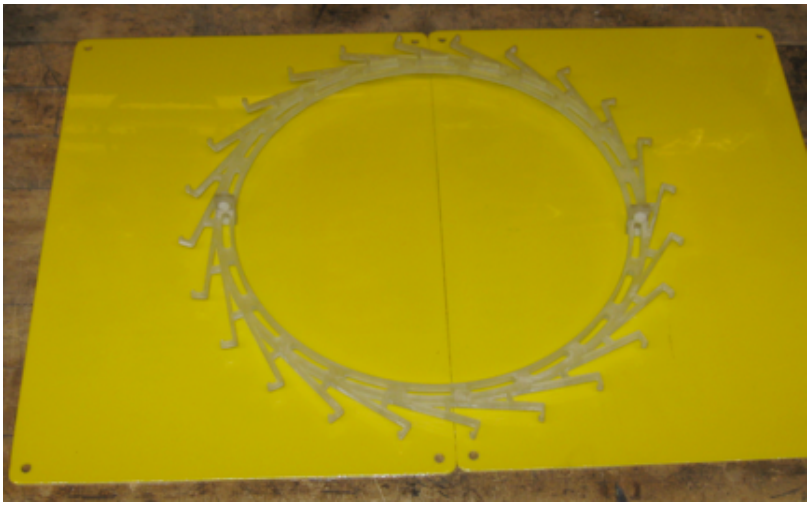


Figure 65: Rapid prototype of the IST ladder mounting structure.

The mechanical support structure will be manufactured with an overall accuracy of 100 µm. Locally, the structure supporting the IST requires an accuracy of less than 100 µm. For instance, the mounting surfaces of the sensor modules will have to be flat to within 50 µm to avoid stress on the sensors.

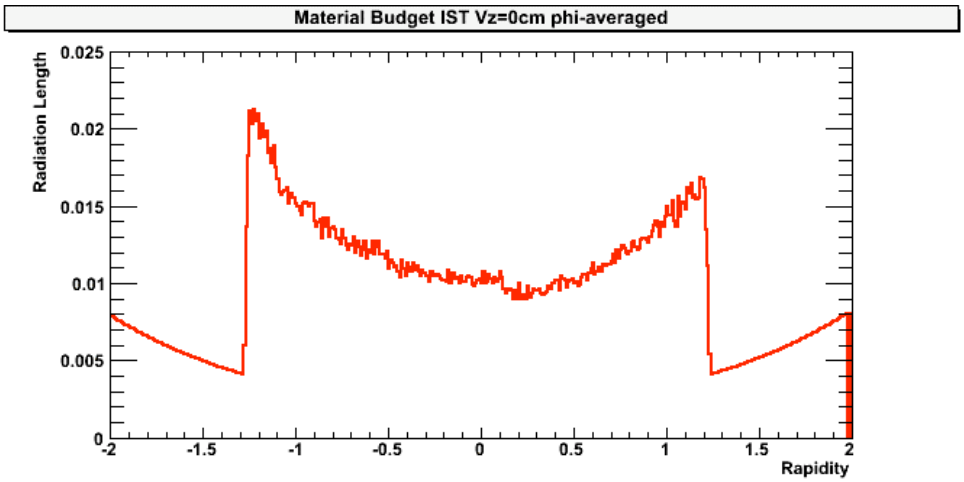


Figure 66: Phi averaged material budget for the IST as a function of rapidity.

Figure 66 provides a realistic estimate of the IST material budget by describing ladder and module designs in a GEANT geometry. These results were obtained by propagating 100,000 geantino events through the IST geometry using GEANT 3.21/08. The material budget at mid-rapidity is well below the required 1.5% X_0. The MSC and support clips where not included in

this calculation. The Kapton readout cables only running in the negative rapidity direction causes the asymmetry in the material budget.

4.3.7. Cooling

The only source of dissipation on the ladders is the 36 APV25-S1 readout chips. Although the nominal power consumption is about 300 mW per chip, the final power consumption depends on the capacitance of the attached sensor channels and consequently the optimal settings of the chip parameters. For safety margin a maximum dissipation of 400 mW per chip is assumed. This leads to a dissipation of about 15 watt per ladder, 360 watt for the whole IST barrel. Trying to cool this with air only was considered too daunting and liquid cooling channels were incorporated in the ladder design. The power dissipation of 15 Watts per ladder leads to about 0.6 mW per mm^2 dissipation if the heat would spread out isotropically. The placement of the cooling tube directly under the readout chips and the use of high thermal conductive material like carbon foam will make the cooling of the ladders manageable with a room temperature cooling system. Calculations making use of FloWorks and SolidWorks are underway to determine the optimal cooling configuration. Figure 67 shows a simulation for a Freon cooled IST ladder incorporating a flattened cooling tube. In this picture the color coded temperature is displayed, showing that the APV25-S1 readout chips heat up to about 89° F (32° C). Most of the ladder remains at about 25°C.

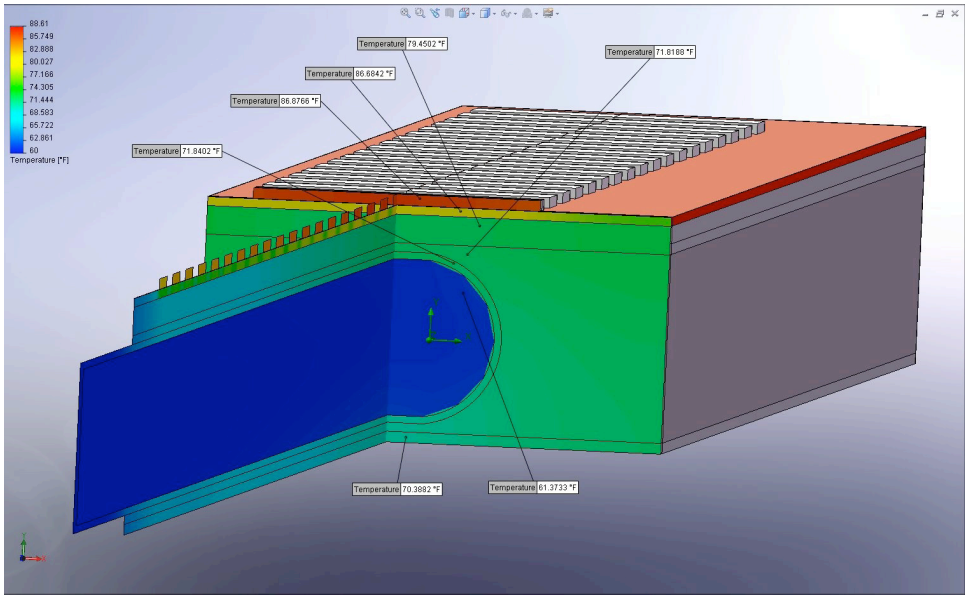


Figure 67: FloWorks simulation of a liquid cooled IST ladder.

4.3.8. Readout System and DAQ Interfacing

Two customized Wiener VME readout crates will house the 36 readout boards (ARM) and 6 crate controller boards (ARC). The boards are of standard 6U x 220 mm size; the crate interconnects these boards with standard 7-slot passive CPCI backplanes and provides integrated low noise 5 V power supplies. The crate will be mounted on the south electronics platform next to the STAR detector. Each ARM handles two detector cables (24 APV chips), providing an ADC, data

buffering and control of APV chip triggering and readout sequencing. The APV chip sample clock is 37.532 MHz, phase-locked to the RHIC bunch crossing (9.383 MHz). This stable timing ensures stable effective gain without the necessity of a timing correction. The ARM also provides the I^2C slow controls interface and isolated low-voltage power supplies to the detector. The ARC interfaces to the STAR trigger and to STAR DAQ via the ALICE Detector Data Link (DDL) Source Interface Units (SIU), the standard for all new STAR DAQ-connected developments for the DAQ1000, Time of Flight (TOF), Barrel (BTOW), Forward GEM Tracker (FGT) and Endcap (ETOW) tower level 2 upgrade. The readout system can buffer up to 4096 events (the maximum number of outstanding events in STAR) and therefore decouples the IST dead time from the data acquisition system, providing a simple fixed dead time. The dead time depends on operating configuration but will typically be 11 μs, with a maximum of 26 μs. A Linux box will be located in the STAR DAQ room and fitted with the ALICE DDL receiver boards and a Myrinet interface to the event builder computer. A schematic detailing these connections is shown in Figure 68.

4.3.9. Slow Controls System

The slow controls system will serve as the primary means for controlling and monitoring the working parameters of the IST. These parameters, such as the hybrid temperature, component currents and voltages will be interfaced with the standard STAR alarm system. The alarm system logs the parameter history and alerts the shift crew if operating limits are exceeded. The black dashed lines in Figure 69 show the communication flow between the slow controls computer and the hardware being controlled. The red solid lines represent the actual hardware connections, which allow this communication. The slow controls for the IST detector and readout crates will be handled exclusively by Ethernet traffic to the IST Linux box, through the ALICE DDL link to the readout crates, and then finally through the RDOs to the APV's via the local I^2C link. There will be no other hardware needed for slow controls. All power supplies will be fitted with an Ethernet controls interface.

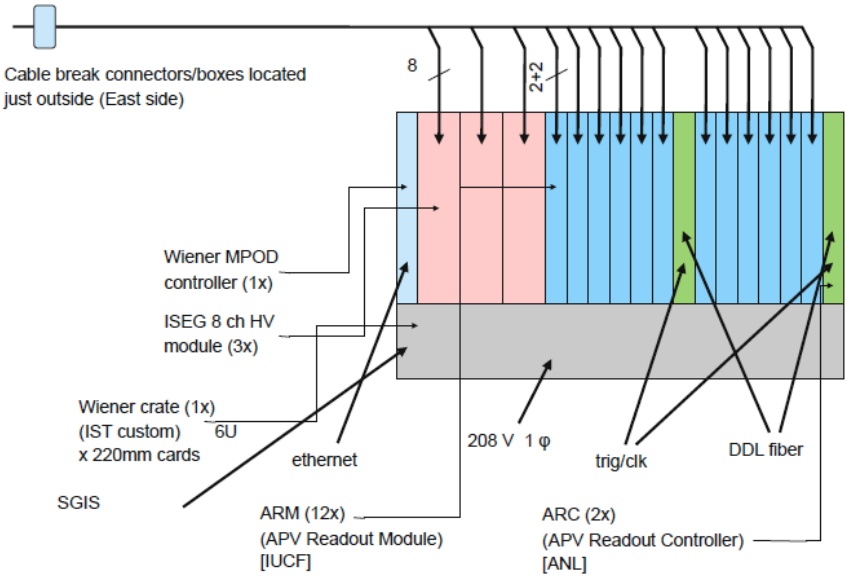


Figure 68: IST DAQ block diagram.

Although STAR is using EPICS as its standard slow control system there is a slight preference to use LabVIEW instead. LabVIEW provides the user with virtually any instrument driver and a very convenient user interface. LabVIEW runs on both Windows and Linux. It is relatively simple to interface LabVIEW and EPICS. At the moment, both options are still open.

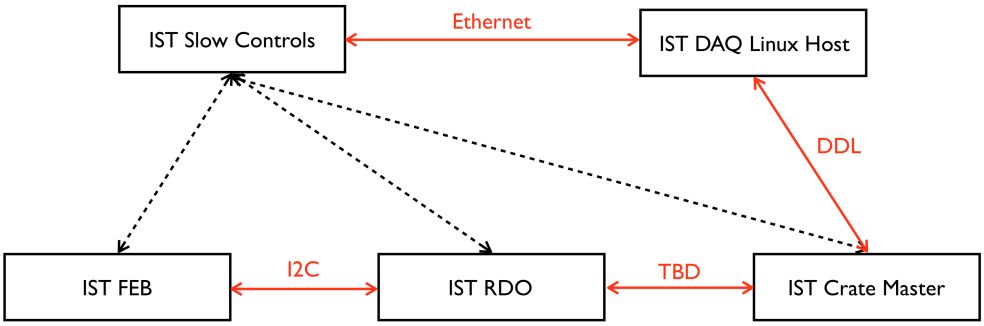


Figure 69: IST slow controls flow diagram.

4.3.10. Spatial Survey and Alignment

The IST will have to be aligned with respect to other detector subsystems of the inner tracking upgrade, PXL and SSD. The final alignment will be done with tracks through an iterative residual method. However, for this method to be successful it is important that the positions of the active elements are known in advance with an accuracy comparable to the resolution of the detectors. A 5-step plan can achieve this.

The positions of the sensors on the module have to be determined. Internally the structure of the sensors will be known with an accuracy of about 1 to 2 µm. This information is obtained through the production mask drawings of the sensors and accessed through alignment marks on the sensors. The modules will be built on an assembly machine under control of an operator checking the process under a microscope. The expected placing accuracy is 5 µm. After the modules have been assembled they can be surveyed with an optical survey machine at MIT. The accuracy of this machine is about 10 µm in-plane. An out-of-plane contrast measurement leads to an accuracy of 50 to 100 µm.

The same methods will be used for the ladders. Three modules will be glued to one ladder with an accuracy of about 5 µm. Then the ladder will be optically surveyed with an in-plane accuracy of 10 μm and an out-of-plane accuracy of 50 to 100 µm. After the ladder is approved it will be shipped to BNL where an additional survey will take place.

At BNL the ladders will be put together in 2 clamshell cylinders that can be measured on a coordinate measuring machine. After the clamshells have been put together on the ISC to form the IST barrel another survey needs to take place. Up to this point it should be possible to survey the silicon sensors themselves. The sensors have the highest internal accuracy (1 to 2 µm) and in the end it is their position, which should be known with the best accuracy. However, after the clamshell has been closed visual access to the sensors will become impossible, especially after the ISC gets integrated with the rest of the inner tracking system. It is important to have survey points on the ladders, the clamshell structure and the ISC, which are visible to the BNL survey group. These survey points then 'anchor' the IST inside the inner tracking system and finally to the whole STAR detector.

4.4. The Silicon Strip Detector

The SSD[45] is a high-resolution silicon strip detector that is mounted at a radius of 22 cm. Its radial location puts it midway between the event vertex and the first active row of the TPC. Thus, it is ideally suited for the purpose of improving the TPC's pointing and momentum resolution.

The SSD was designed to work with the TPC and the STAR Silicon Vertex Tracker (SVT). The design readout frequency of the existing SSD is 300 Hz. This does not meet the HFT readout frequency requirement of at least 1 kHz. Therefore, the readout electronics needs to be upgraded. To achieve the new speed requirement, the existing silicon detector wafers and the ladder structure is kept and a significant amount of the electronics are replaced. The upgrade also requires new cabling, cooling, and mounts. Table 15 shows the relevant parameters of the SSD.

4.4.1. The SSD Barrel

The SSD barrel is composed of 20 individual ladders. The ladders are made of carbon fibre and each ladder supports 16 detector modules. An overview of the assembly is shown in Figure 70. Each of the modules is composed of one double-sided silicon strip detector and two hybrid circuits equipped with analog readout electronics. On both ends of a ladder, two electronics boards are used to control the detector modules and convert the analog signal from the Si wafers into a digital signal, which is then sent to readout boards that are located on the STAR south platform.

SSD Radius	22 cm
SSD Length	106 cm
$\|\eta\|$ coverage	< 1.2
Number of ladders	20
Number of wafers per ladder	16
Total Number of wafers	320
Number of strips per wafer side	768
Number of sides per wafer	2
Total number of channels	491520
Silicon wafer size	75 × 42 mm
Silicon wafer sensitive size	73 × 40 mm
Silicon thickness	300 μm
Strip pitch	95 μm
Stereo Angle	35 mrad
R-ϕ resolution	20 μm
Z resolution	740 μm

Table 15: Summary of SSD characteristics and performances.

One ladder is shown, in detail, in Figure 71. In the new electronics, two cable busses (one per side of the Si wafers) transport the analog signals along the ladder to a pair of ADC boards, where the signals from the 16 wafers are digitized concurrently. After digitization, the signals are sent via optical fiber links to the Readout Boards, which are in turn linked to the DAQ system through optical fibers.

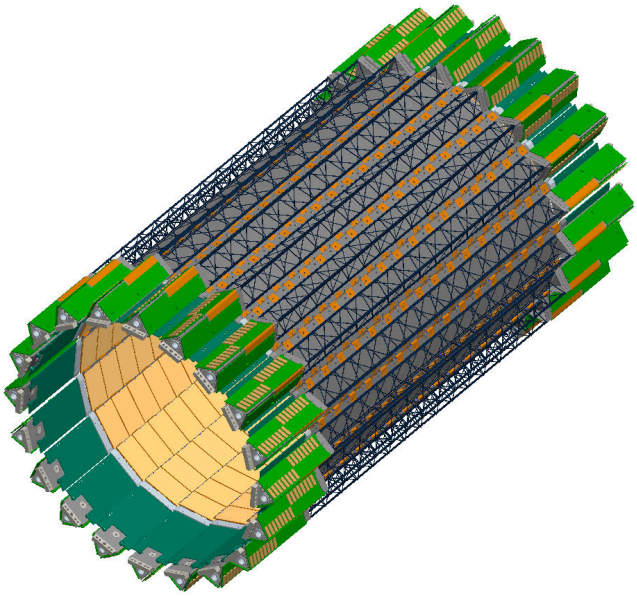


Figure 70: A CAD model of the SSD. The rectangular gold objects in the inside of the cylinder represent the silicon. The triangular structure in the center is the ladder support. The green objects at the end represent the readout electronics (Ladder Board).

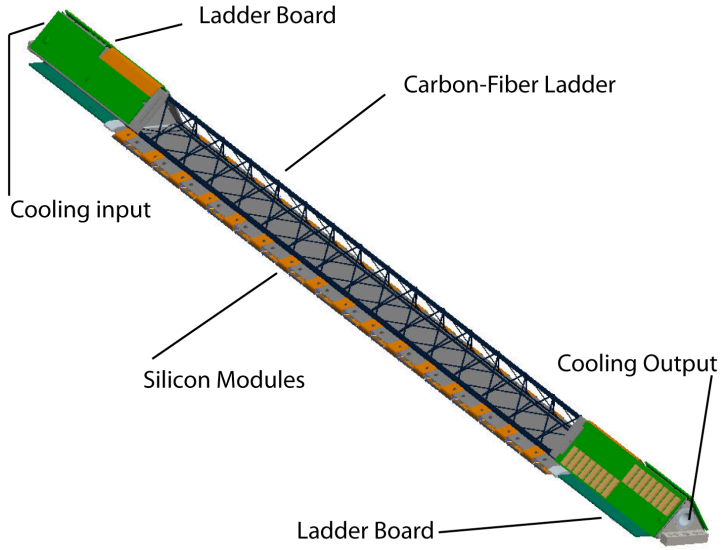


Figure 71: An SSD ladder showing its various components. The Ladder Board contains the electronics that reads out the silicon modules.

A detector module is the basic element of the SSD and it integrates a silicon wafer with its front-end electronics. One detector module is shown in Figure 72. Each module is composed of a silicon detector and two hybrid circuits. A silicon strip detector measures 42 mm by 75 mm. It is double-sided with 768 strips on each side of the detector. The strips have a pitch of 95 μm, and are crossed with a 35 mrad stereo angle between the strips on the P and N side of the silicon. It takes 16 modules to fill a ladder. A Ladder Board reads out the module at each end.

The two hybrid circuits are built on top of a flexible circuit made of Kapton and copper, which are, in turn, glued to a carbon fiber stiffener. The circuitry includes 6 analog readout chips (the ALICE 128C) and approximately 50 components (resistors and capacitors).

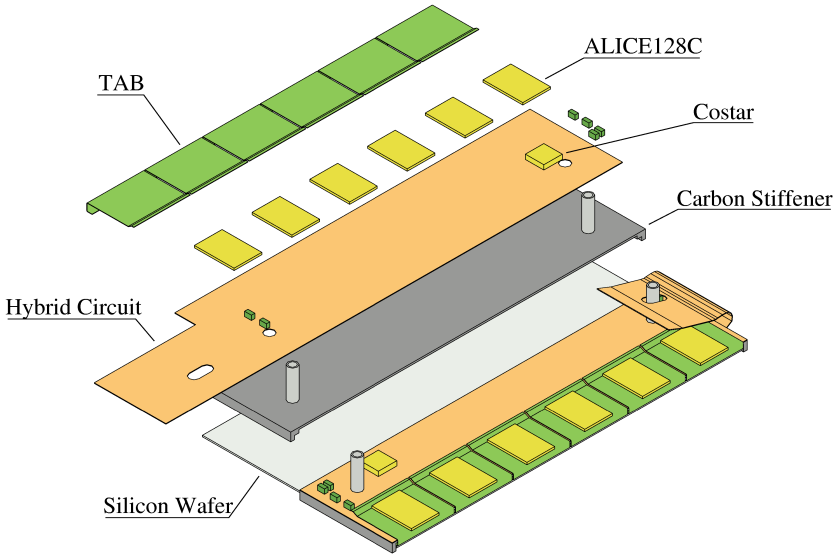


Figure 72: Exploded view of one detector module.

4.4.2. Electronic Upgrade

A Ladder Board reads each detector module in parallel. Figure 73 shows the block diagram of the ladder board and the RDO Board. The optical connection is bidirectional; the second fiber provides trigger and slow control information to the FPGA on the ladder board, which manages the analog circuitry on the ladder.

Ladder Board

Every module on the SSD ladder has its own ADC, thus 16 ADC channels are needed. We use 8 Analog Devices AD7356 dual ADC chips. Each chip contains two independent ADCs with 5 MHz sampling rate and a bit-serial output. The serial output produces a 14-bit pulse train, of which only 10 bits are used in this application. The outputs of these 16 ADC channels are sent to the inputs of a parallel-serial converter, along with the slow control output of the FPGA. The parallel signals are clocked in to the serial converter at a 40 MHz rate, resulting in a 1.4 Gb/s pulse train, which is converted to optical signals and transmitted to one of the 5 inputs of the RDO board. The optical nature of this connection allows the RDO crate to be located outside the STAR magnet.

RDO Board

Each readout card accepts the fiber link from five ladders. A readout card is connected to the DAQ SSD PC by a DDL fiber link (50 MHz × 32 bit = 1.6 Gb/s or 40 MHz × 32 bit = 1.28 Gb/s) identical to those in reading out the TPC. Eight readout cards (four for each SSD side) reside in a 6U VME crate; there are, therefore, 8 fibers connecting the readout crates to the DAQ computers.

The DDL links, together with their source interface to the SSD RDO (SIU board) and the PCI-X card residing in the SSD DAQ PC (D-RORC board), are readily available for purchase.

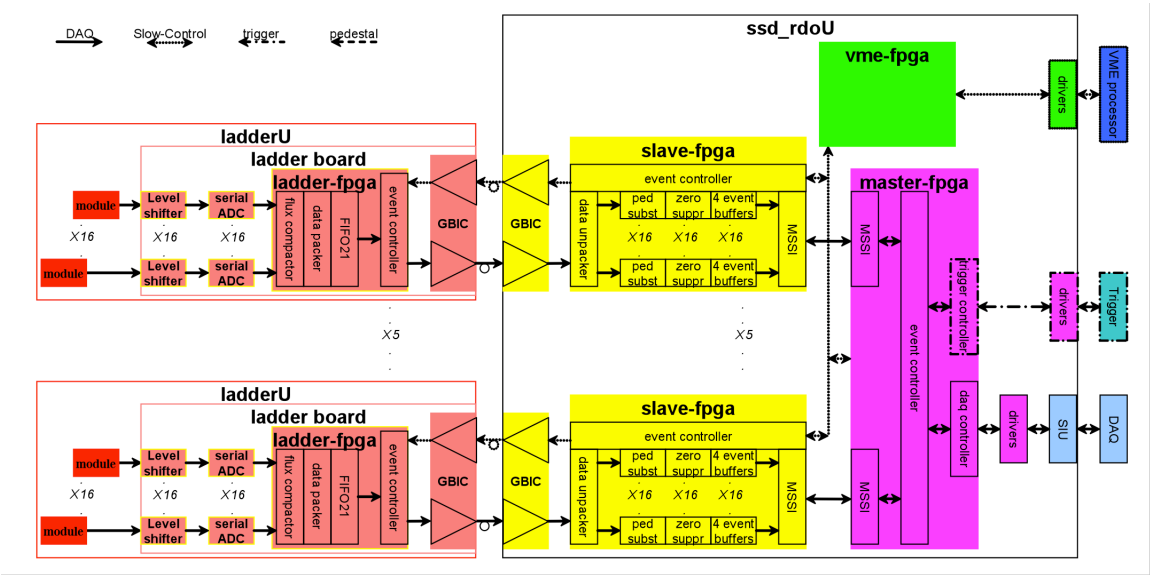


Figure 73: A schematic of the interconnection between the ladder electronics and the RDO card, Each RDO handles 5 ladders. The connection between the ladder electronics and the corresponding RDO card is a dual optical fiber.

At the RDO card, the 1.4 Gb/s bit train is converted by a deserializer to a 20-bit wide data path, which is updated at a 40 MHz rate. Twenty of the 24 bits produced by the deserializer are reshaped into a 50 MHz stream of 16 bits width and delivered to a second bank of 16 1:10 deserializers, resulting in 16 10-bit wide replicas of the original ADC values produced on the ADC card. (The remaining 4 bits are used for the slow control function.) This second bank of deserializers is contained in an array of 5 FPGAs, each one dedicated to the data delivered by the fiber from a single ADC card. These FE-FPGAs perform zero suppression and multi-event buffering on the 16 data streams produced in the last bank of deserializers.

The multi-event buffers and zero suppression both provide a means to reduce dead time due to data burden on the DDL optical fiber. Zero suppression is carried out in the simplest possible way – the ADC value for each strip is compared with a stored pedestal value corresponding to that strip. If the ADC value exceeds the pedestal, the strip number and ADC value are encoded into a 32-bit word and entered into the multi-event buffer.

The multi-event buffers are provided as a second means of reducing dead time. Simulation has shown that for randomly spaced triggers 4 buffers can keep the dead time to about 7 per cent for a trigger rate of 1 kHz. We expect about 3% of the strips to be hit in a central Au+Au event.

There is sufficient on-chip RAM storage in the FE-FPGAs to implement buffers for 4 events that have not been zero-suppressed. In zero-suppressed mode, these buffers can be coalesced into a single event buffer large enough to handle the largest zero-suppressed event. During data taking, it is expected that the operator will monitor ladder occupancy. When a ladder is observed to be producing large zero-suppressed events, the offending module will be masked off.

The ladders are read out by passing a token to the chain of 6 ALICE128 analog multiplexers handling the analog signals corresponding to the 768 strips of a single module. Once this process has started, it must continue until the token reappears, at the end of 768 clock cycles. In the event

of an abort arrival, the clock speed is doubled in order to minimize the time consumed by this process.

Services

The electronics are located on the South platform, where space is readily available. A VME crate contains both the RDO cards and the Slow Control communication interface.

The 8 SSD readout cards require 8 DDL fiber links to DAQ PCs. Each DDL receiver card (DRORC) handles two fibers; thus, 4 DRORC cards are required to provide the necessary interface. This is best implemented in 2 PCs, each with 2 DRORCs. Each PC is responsible for one-half of the SSD.

The Slow-Control information to and from the ladders travels over the optical fibers to the readout cards The SSD Slow-Control interface consists of two independent JTAG chains: the Slow-Control chain and the FPGA configuration chain. Slow control communicates with the RDO board through the VME backplane. The transport on optical fiber between RDO and ADC boards is completely transparent to all the components that have to decode and answer to the JTAG orders.

Each of the 8 readout cards has its interface to the STAR trigger.

4.4.3. Mechanical Mounting

The SSD is mounted on the OSC via a small bracket that is show in Figure 74. This design eliminates an end ring that creates significant backgrounds for the FGT. To assemble and repair the ladders, each ladder can be removed separately. Figure 75 shows the mechanical dimension of each ladder and that there is sufficient clearance to take out each ladder.

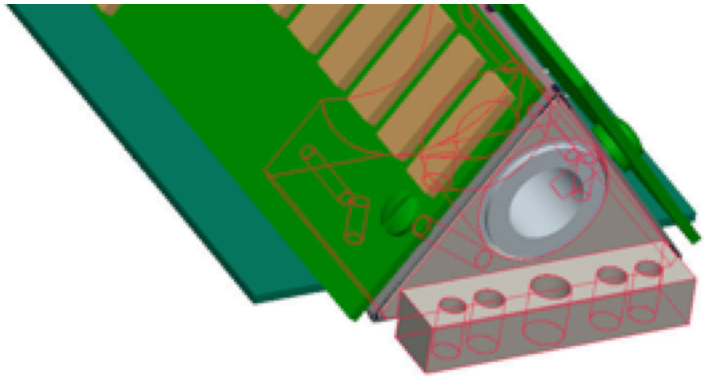


Figure 74: End bracket for the SSD that mounts to the OSC. The holes are used for alignment and to fix the detector.

4.4.4. Cooling System

The evacuation of heat produced by the electronics in the SSD is critical in order to establish stable behavior with the sensors and the associated electronics. The power consumption of the different components of the SSD ladders can be separated into two independent parts: The first part is due to the Front End Electronics (Alice 128C) chips, and the second part to the Ladder

Boards. The Si detector modules do not contribute substantially to the power consumption budget.

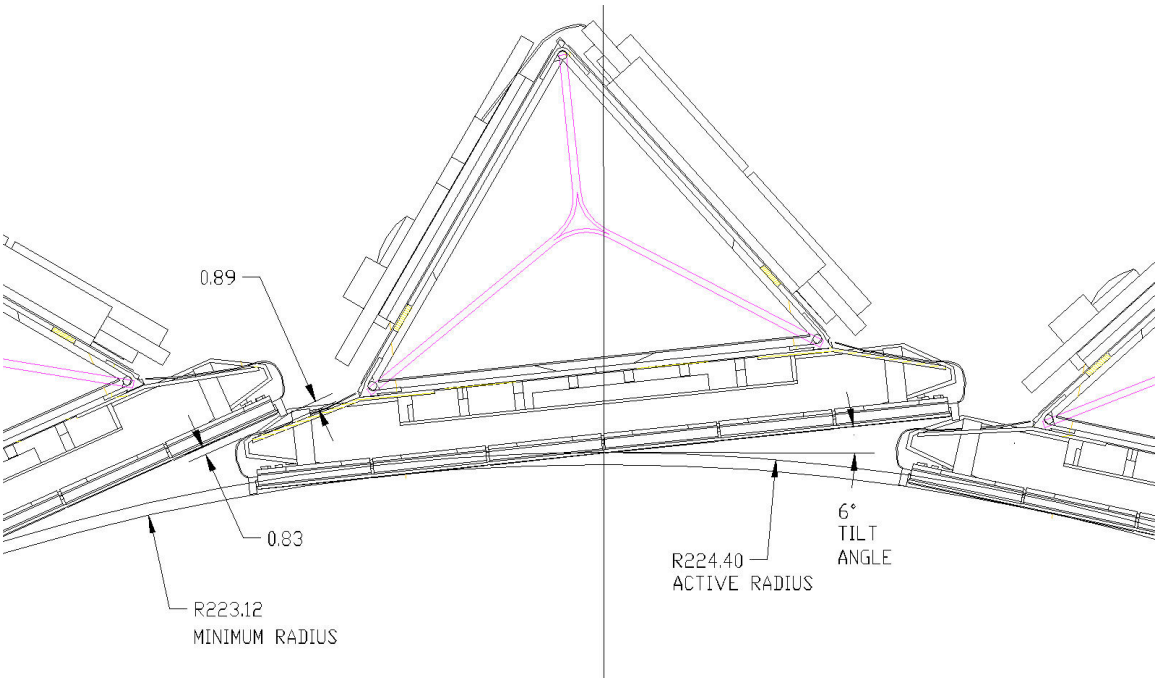


Figure 75: Physical location of each ladder. The length dimension is in mm. The tilt angle has recently been increased to 7° to provide clearance for a post on the modules. This results in a slightly smaller radius.

The ADC chips selected for the ladders consume very little power (20 mA @ 2.5 V). Taking into account all of the remaining components, the electronics at the end of each ladder are expected to consume 6.7 W. Thus, the estimated dissipation for a full ladder is expected to be 23.4 W compared with 20 W for the existing system.

Table 16 compares the power consumed by the FEE electronics and the electronics boards on both ends of each ladder for the old and the new design.

	Old	**New**
Total FEE	10 W	10 W
Total Electronic Boards	10 W	13.4 W
Total per ladder	**20 W**	**23.4 W**

Table 16: Estimated power consumption for a ladder

The Air Path in the Ladders

Each ladder is cooled by air circulating throughout the carbon fiber structure and, in effect, the ladder functions as an air pipe. So each ladder is wrapped in a thin Mylar film to guide the air. The electronic boards are installed on the ladder ends with the components pointing inwards and 'seeing' the inside of the triangular section. Deflectors inserted inside the ladder help guide the air to the warmest components.

The flow of air is driven by an external vacuum system so that air is pulled through the ladders and the heated air is removed from the central part of the STAR detector. The input air comes from the TPC Inner Field Cage (IFC). The warm air is then evacuated to the outside of STAR through a flexible hose of approximately 10-mm diameter.

Requirements and Functionality Tests

Cooling the electronics is an essential task to maintain the performance of the detector. The Si detectors and the ADC boards become unstable when they get too hot. For example, during RHIC Runs 6 and 7, the SSD ladders routinely tripped when they reached a temperature between 45°C and 50°C. The exact temperature that the modules tripped depended on the location and ladder number. The temperature rise produced an increase in leakage current, which resulted in lower bias voltage at the silicon due to IR loss in the bias resistor. In order to regain depletion, the voltage had to be raised. This cycle continued until the power supply tripped off. So experience has shown that the SSD electronics should be maintained at 35°C to 40°C; and pushing the temperature above 40°C reduces the efficiency of the detector.

The SSD design team has done a series of thermal tests on a ladder to see how it performs under various conditions. Table 17 shows the temperature inside the ladder at a few critical points when the cooling system is off. The maximum temperature measured was 46.5°C. These tests were done at an ambient temperature of 19°C whereas the average temperature inside the IFC of the TPC during Runs 6 and 7 was 24°C.

	SIDE P (°C)	**SIDE N (°C)**
ADC	42.8	46.5
Control Board FPGA	34.8	36.5
Connection Board	45.2	45.4

Table 17: Mean electronics temperatures measured on the test ladders with cooling off. The ambient air temperature was 19°C.

Table 18 shows the temperature distribution at the critical points with the cooling 'on'. Once again, it is worth noting that these temperatures were recorded using input air at 19°C. In the actual STAR environment, the input air is drawn from the IFC and the air in this region typically has a temperature of 24°C.

	SIDE P (°C)	**SIDE N (°C)**
ADC	33.1	33.2
Control Board FPGA	33.7	30.7
Connection Board	27.6	24.5

Table 18: Mean electronics temperatures measured on the test ladder with cooling on. The ambient air temperature and input air temperature was 19°C.

Additional temperature measurements were performed at various points along the ladder and these results are shown in Table 19. Between modules 8 and 11 (in the middle of the ladder), the temperature goes above 37°C, even when the cooling system is on.

Module	Si Temperature (°C)	COSTAR Temperature (°C)
3P	27.8	35.3
5P	32.9	32.5
8P	30.9	37
11P	30.2	37.5
14P	28.7	34.9
16P	25.1	32.3

Table 19: Mean Temperatures measured at various points along the test ladder with the cooling system turned on. The column on the left identifies the wafer number (1-16).

Results from Run-7 show that when the SVT was turned on, the leakage current increased. Thus, it appears that the SVT produced an additional heat load on the SSD. The SSD cooling system is designed so that it uses the air from the IFC, no other detector can provide heat to it, and the ladders are kept to a range between 32°C and 37°C.

Vacuum Source

The SSD vacuum system also needs an upgrade because the existing Vortex system is complex, prone to failure, and expensive. It consumes 76 kW of power. A cheaper and more reliable system is available from a commercial manufacturer. A three-phase system is highly desirable because a 3-phase motor does not require brushes and so is capable of continuous operation over a very long period of time. The location of the vacuum system is on the North Platform (dirty power side). It provides vacuum to the SSD via non-conducting plastic pipes. The precise details on how to route the pipe, and divide the airflow so that it reaches each ladder are still to be determined.

4.4.5. SSD Ladder Status

The SSD detector was used last during Run-7. At the beginning of the run, several ladders were known to be inoperable. Due to hardware issues, two ladders did not provide useful data and were turned off at the beginning of the run. Four other ladders were not stable when they were operated at the nominal HV configuration. They needed to be operated at a lower voltage and therefore were less efficient. During the run, it was determined that there was inadequate cooling to several ladders. Upon inspection after the run, several bent cooling hoses were found and are the probable cause of the ladder's overheating and instabilities. After Run-7, the SSD was removed and returned to Subatech Laboratory in Nantes. There the engineers tested each ladder and made a few repairs.

Among the 22 ladders (the 20 ladders that compose the SSD and 2 spare ladders), there are 6 perfect ladders; the others have flaws of various kinds. Eleven ladders have a few hybrid circuits that cannot be fully tested with the Subatech test bench. However the data acquired with these hybrid circuits may be completely usable. It was observed during the last data taking at STAR, that most of them produce good data. Nevertheless, due to some cooling failures and to reduce the heat load, a few of the hybrid circuits were turned off.

At this time, it is not possible to give a definitive status of these hybrid circuits. However, a software upgrade is planned to enable testing of these circuits. For a conservative estimate, we assume these hybrid circuits are bad. Using these assumptions, we obtain:

- 7 ladders with one hybrid circuit (out of 32 per ladder) not fully tested,

- 1 ladder with 2 hybrid circuits not fully tested,
- 2 ladders with 3 hybrid circuits not fully tested, and
- 1 ladder with 8 hybrid circuits not fully tested. (This was the first ladder produced so assembly techniques evolved during its assembly.)

In addition, a few inoperable hybrid circuits have been identified in five ladders. During data acquisition, these hybrid circuits had to be bypassed and thus did not provide data.

- One ladder had two partially damaged hybrids. One hybrid circuit had one group out of a total 6 dead., while another hybrid circuit had 5 groups damaged. This results in an effective inactive area of one hybrid.
- One ladder with 1 dead hybrid circuit and 2 not fully tested hybrid circuits. If the 2 not fully tested hybrids are considered as bad, this leads to an electronic coverage of 91% and for STAR data use 81%. The value is less for STAR data use as the current STAR tracking algorithms require that both the N and P side to functional. It is worthwhile to mention that the two hybrids could provide good data but have not been checked yet.
- Three ladders, known to have frequent HV trips during data taking, have been diagnosed to have some of the modules/hybrid circuits that cause a high leakage current. In that state, the culprit hybrid circuits are disconnected. This means we can use 1 ladder with 2 hybrid circuits off, another ladder can also be used with 4 hybrid circuits turned off, and the last ladder is operational with 2 modules turned off. In addition, some chips are missing (5 in total) and 1 hybrid circuit is not operational.

A repair of the four ladders with needed excessive HV was studied. Thermal images of a hybrid circuit with high leakage current found one of the capacitors hotter than the others. The capacitor was then carefully removed from the circuit. When the ladders was retested, the leakage current returned to their nominal current. After the success of the first repair, this procedure was repeated with the other three high current ladders. All of the repairs were a success and now all of these ladders are working.

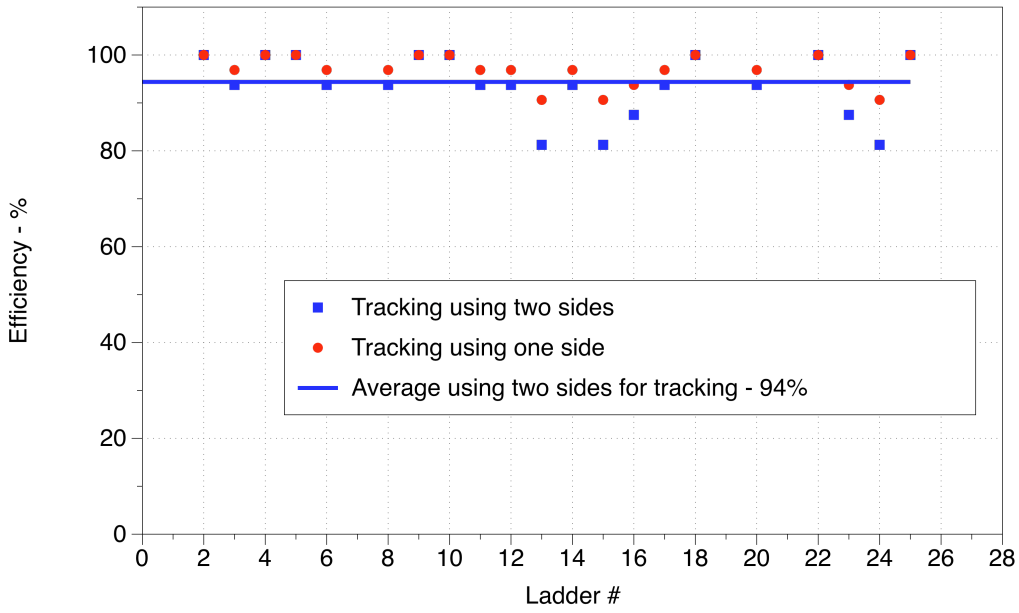


Figure 76: A plot of the efficiency for the existing 21 ladders. The blue points assume that both the n and p side are needed in tracking. The red points are for the case when either side is used.

Figure 76 shows a summary of the current status of the best twenty-one ladders. It assumes that the hybrid circuits that cannot be fully tested are bad. This figure shows the *lower limit of the active coverage*. The red marker represents the electronic coverage for each ladder. Since the SSD tracking software has been designed to use both the p and n side to determine a particle's position, one single side hybrid failure can result in the whole module being declared unusable. The blue triangle marker in Figure 76 shows the active area taking into account this effect. The average coverage, 94%, is represented by the blue dotted line.

It is worthwhile to note that only one side of the module can detect a particle when the hybrid serving the other face of the module is not operational. This change would degrade the spatial resolution, but it would increase the spatial coverage to 99%. Preliminary studies indicate it is possible only to use one side of module for STAR tracking.

4.4.6. Rack Space

The SSD currently occupies one rack on the South Platform. This rack contains a VME crate, two CAEN power supply crates, and two distributions boxes for the HV and power cables. This space is maintained for the present CAEN supply or a replacement. The power supplies provides, 100 V, +2 V, -2 V, and +5 V to the ladder.

4.4.7. Services

The SSD services must pass through the integration constraints of the WSC and FGT on the west end, and the MSC and ESC on the east side. Therefore, we make a preliminary estimate of the space needed. This is based on consideration of the current draw and allowable voltage drop for the ladder power connections, and the count of other conductors and optical fibers needed to service the ladder. All conductors will be standard commercial CCAW wire (10% by volume copper-clad aluminum). The cable is a custom construction with an aluminum foil shield and silicone insulation and jacket materials, which have excellent performance with regard to flammability, radiation tolerance, and mass. The cable diameter estimate accounts for fill factor and for insulation and jacket thicknesses to meet the required voltage and flammability ratings.

Function	Type	#	Diameter mm	Area Rectangular cm^2	Total Area Rectangular cm^2
DAQ and Slow Control	Optical Fiber (dual)	20	3.0	0.1	1.8
Ladder power / bias	Sense (×6 AWG 26)	20	5.5	0.3	6.1
	LV (×8 AWG 22)				
	HV Bias (×2 AWG 26)				
Air Cooling	Air cooling to end of cone	20	12.7	1.6	32.3

Table 20: SSD services parameters. The total area is calculated in square centimeters, not accounting for packing fraction. The diameter of the air-cooling is taken from the size of the original SSD design.

The SSD is readout separately on each side of STAR. Each ladder is a separate detector. Therefore there will be 20 cables and 20 dual fibers on both the East and West end. As each ladder requires only one HV bias connection, these wires are simply unused in the west cables where space is more constrained. An estimate of the size needed for these cables is given in Table 20. These cables will connect directly to the ladder board on one end and then be terminated on a block so that that cabling to the platform can easily be reconnected. Two flat areas on the FGT have been allocated to these cables. The values specified in that table with some contingency with fit in that location.

There will be a direct connect from the cone to the SSD racks on the South Platform. If the existing power cables are acceptable, then they will be used. If not, then new cables they will be replaced. The Optical Fibers are new. The air-cooling will come from the North Platform.

4.5. Global Support

The HFT is a highly integrated project. In addition to two new detectors, IST and PXL, the HFT project deliverables share supports with the FGT, and directly support the SSD and a new beam pipe for STAR. Additionally, HFT must be compatible, thus 'integrated' with all future STAR physics programs, which might interface to or be impacted by it.

The supports for HFT and FGT will replace the current support cone structure in its entirety. This new structure, called the Inner Detector Support (IDS), shares deliverables with FGT, but nominally replicates the current mechanical interface of the current cone system to the STAR TPC. This will be described in more detail below. Installation of this structure is nominally identical to the insertion and removal of the current support cone so will follow existing procedures and use current tooling.

HFT also requires a new beam pipe for STAR. The PXL detector has a smaller aperture than the current beam pipe therefore a necked beam pipe is required on the same timeframe as first insertion of the PXL. The HFT PXL Detector is intended to be easily installed and removed, especially during RHIC operations. PXL installation is explicitly not included here, rather in the PXL mechanics section (Section 4.2.3) of this document.

The various support structures for SSD, FGT, IST, PXL, and the beam pipe also support all internal service routing, and must be compatible with IFC (Inner Field Cage) E-field requirements. The services for the SSD will impact the design of the FGT as they will share space with FGT services. Adequate routing space and strain relief for services is a requirement across all integrated detectors and here we will include requirements placed on the FGT project (to allow space).

The integration of the HFT project is probably best described in terms of the Assembly Break Down Structure (ABS). An ABS rather than a WBS is better at capturing discrete interfaces which must be controlled – even within a given WBS task. The sections below will roughly follow an ABS.

Following is an overview of the primary integrating structures, their interfaces to each other and the detectors, which they support. This will be presented in an ABS format, and followed by a summary of services both internal and external (inventory and requirements). A brief description of the new beam pipe for STAR will also be provided.

The assembly and installation is described in a specific scenario, where integration with FGT and beam pipe is in summer 2011, before Run-12, and the final assembly in the summer 2013 shutdown, before Run-14. The schedule of the upgrade may not in fact happen in those specific years. The preliminary project execution plan in fact has milestones that corresponds to these shifted by one year. Take the term Run-12 and Run-14 as generic in this section and not indicative of a firm year.

4.5.1. Mechanical Supports and Structures

The HFT and FGT projects will replace what STAR calls the 'Cones' within the IFC of the TPC. The 'Cones' currently support the beam pipe, and formerly the SVT and SSD detectors. The current cone structure is incompatible with the FGT. The FGT requires a 'cylindrical' replacement of the West Support Cone (WSC), to accommodate the cylindrical shape of the GEM disks and their positions for required pseudo-rapidity coverage.

The current, soon former, cone structure is monolithic – it is bonded together: two identical cones, attached to each other via two elliptical beams. These are bonded together via large aluminum inserts at the ends of each beam and the small ends of the cones. The SSD and beam pipe are currently supported via these large inserts (see Figure 77).

The IDS, will replicate the support interface of the current cone structures to the TPC wheels. Several options have been investigated for this replacement; choice between the various options was optimized via cost and schedule to arrive at the current baseline. The options are not presented in this document.

The baseline plan for support of the HFT detectors and the new small diameter beam pipe involves a new support structure, the IDS. The SSD and FGT will be directly supported on this structure and the PXL and IST will be integrated on a separate structure the MSC (Middle Support Cylinder), which will be inserted into the IDS from the east end. The MSC will also provide the inner supports for the new beam pipe.

The goal of the structural layout is to enable as much as possible the parallel integration of sub detectors prior to a STAR opening. For the first iteration, the PXL engineering run for Run-12, the mechanics will be a direct replacement of the entire cone/beam pipe system. Later installation of the IST and SSD in Run-14 will require recovery of at least the beam pipe from the installed system. Some duplicate structures (production versus prototype) will allow pre-assembly of the IST and SSD before the opening of STAR for Run-14, removing these activities from the critical path of the shutdown. A description of the structures, followed by assembly sequences required for Run-12 and Run-14 follows. Note that most figures shown will be indicative of the configuration for Run-14 as all structures must be compatible with this configuration.

Inner Detector Support (IDS)

The Inner Detector Support is composed of 3 main structures, the East and West Support Cylinders (ESC, WSC), and the Outer Support Cylinder (OSC), which spans the gap between the ESC and WSC. The OSC also will eventually support the SSD in Run-14. The three cylinders, ESC, OSC, and WSC are the primary supporting structure for both HFT and FGT and these structures together are the IDS. The ESC and WSC are nominally copies of each other using common fabrication and assembly tooling. The SSD will eventually be supported on an OSC, but is not intended for Run-12. The MSC which will support PXL, and the beam pipe for Run-12 is supported at both ends of the ESC, and potentially by the west end of the OSC (TBD).

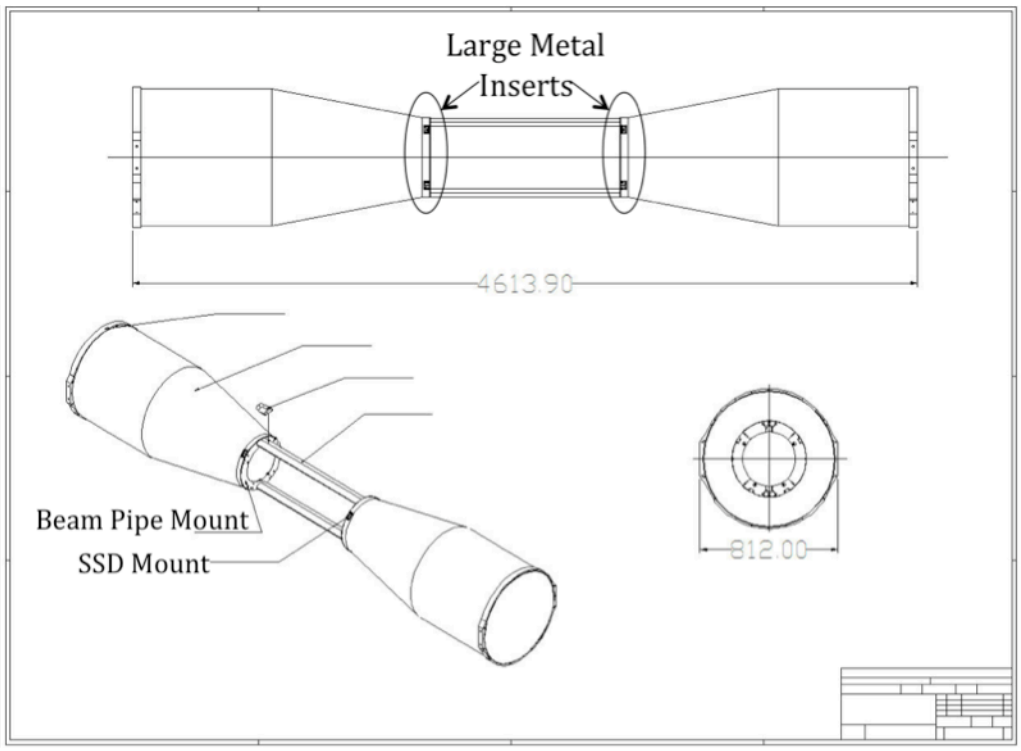


Figure 77: Old detector and beam pipe support.

Mechanical Requirements

The structural performance and interface requirements of the IDS are driven by both HFT and FGT requirements. As it is impossible to have separate supports within the Inner Field Cage for these detectors, some shared design responsibility is inevitable. The HFT requires global stability on the order of the pointing resolution of the TPC, about 1 mm, however the FGT uses the beam constraint for tracking so requires stability on the order of the beam diameter of about 100 μm, so drives the global stability of the IDS. The stability performance of the current design of the IDS is presented in Appendix 1.

The mechanical interfaces, e.g. envelopes and supports are also driven by both FGT and HFT. The length and diameter of the OSC is set by mechanical interface of the SSD layout and its services. The length and diameter of the WSC (thus ESC), is set by the FGT acceptance. The structural elements (material) of the IDS which traverses these envelopes is driven by the structural performance requirements. Additionally, support elements for the SSD, FGT and MSC (Middle Support Cylinder) must be included in the interfaces of the IDS. Routing space for services of the SSD and FGT also impact the IDS.

Electrical Requirements

The IDS is inserted into the Inner Field Cage of the STAR TPC, thus it must be compatible with the bias voltages applied within this environment. The ESC and WSC (large diameters) will protrude into the IFC. A large radius shroud will be provided (see Figure 78) to ameliorate the potential for surface breakdown or coronas at the abrupt changes in radii of the structures. The shroud will also support an EMI foil over the SSD. This shroud, and perhaps a portion of the outer skins of the ESC/WSC will need to be biased. Standoff, both surface and thru-thickness of

any applied bias voltage (some few kV) of the base material of the ESC and WSC structures is required, detail design remains.

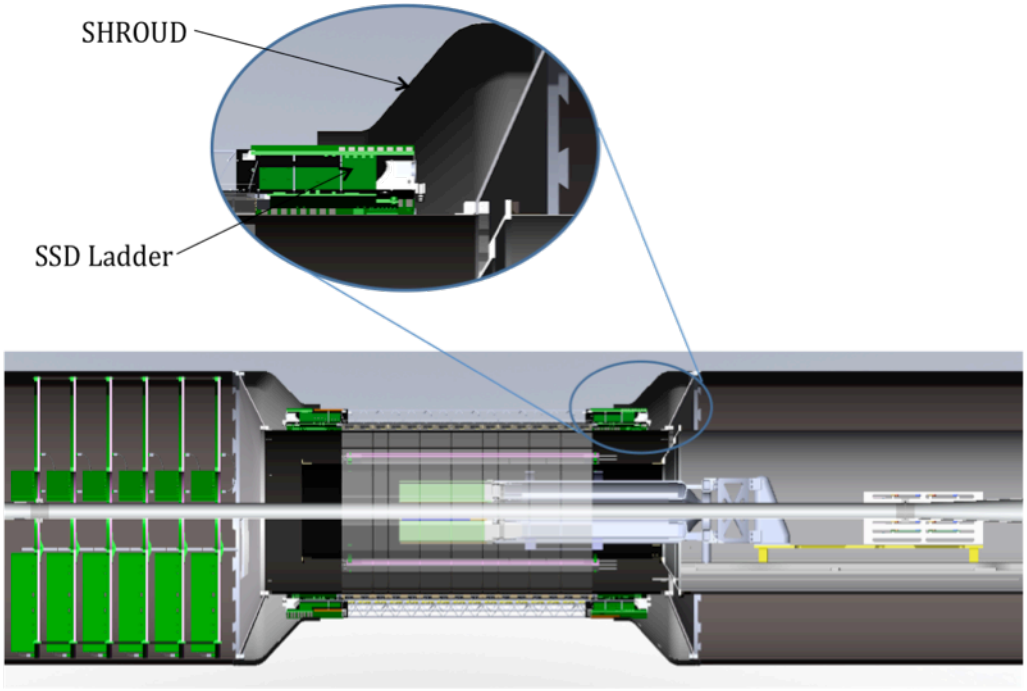


Figure 78: E-field shroud.

West and East Support Cylinders

The intention is to share tooling and thus geometry between these two structures. They are each composed of 3 main elements, each with some sub-structure appropriate to their side (e.g. FGT support on the WSC). These elements are the primary shell (with a flat to avoid the Inner Field Cage resistor chain), a transition cone which spans the radial gap between the shell and the OSC, and a termination ring which is the primary interface to the TPC — essentially replicating the current mechanical support (with brief modifications to improve upon the old adjustment interface).

These structures are the dominant part of the 'simply supported beam' which is the IDS. Each component plays its part in transferring the static loads between TPC supports; these are the primary moment loads from the eccentrically applied detector/service masses, and the reactive point loads from the supports. The transition cones dominate the moment load transfer, and the termination rings will hold the roundness of the shells, both contribute to the overall stability of the IDS.

The electrical Shrouds are not considered part of this deliverable, but are obviously required to meet electrical performance of the IDS system — they will be discussed later.

Structural Shell Assembly

The main component of the structural shell is a thin carbon fiber laminate, potentially with an integral outer layer applied during manufacture to allow for bias voltage to be applied. The inner diameter will be common to both WSC and ESC as it will be set by common tooling. Lamina

may differ between the two structures based on differing structural requirements to support the FGT.

The large sectional inertia of the shell implies that the global performance of the IDS is not dominated by the laminate properties as born out in Appendix 1. It was shown that thickening this laminate simply increased the mass, increasing the deformation implying that this is not an avenue for decreased deflection.

The geometry of these shells is driven primarily by the FGT acceptance. The laminates may need to include provision for bias, thus include some length of conductive surface and sufficient insulated surface to stand off surface creep, and thru-thickness resistance.

Mechanical flanges at the 'middle' (low |Z|) ends are required for mechanical (bolted) interface to the transition cones. A bolted interface is desired to reduce overall risk. The shell is a large part with potentially high fabrication cost; secondary bonding of orthogonal features rather than integrating them into the tooling reduces likelihood of engaging contingency at the expense of an additional assembly step. This is amortized over the risk involved in fabricating the cone structure. Should the transition cone prove inadequate after prototyping, it will allow easier replacement with another iteration of the transition cone.

Transition Cone

The transition cone transfers the primary moment load of the simply supported IDS from the structural shell to the OSC. It was initially envisioned as a flat 'plate' perhaps a honeycomb panel, but studies showed that a conical laminate was more efficient in terms of material (see Appendix 1). Maximizing the cone depth (frustum) maximizes performance of the entire IDS. The frustum is limited by the length of the SSD and the position of the first disk of the FGT. Currently this is limited to 7 cm. With the depth of the cone limited to what is acceptable from active detector layout, the overall stability performance of the IDS is most sensitive to the thickness of the transition cone. The transition cone is currently 4 mm thick, with 5 mm flanges at both inner and outer diameters to allow bolted interface to the structural shells and the OSC. Note that the total flange thicknesses are 10 mm, 5 mm for each side of the flange.

Transfer of stresses into the cone via the flanges has yet to be investigated — they are currently idealized in the analyses, i.e. perfectly coupled. The flanges are currently envisioned to be CFRP with either Aluminum or Titanium fasteners. Fastener stresses will dictate whether these are Al or Ti fasteners, and contact stress may dictate that these flanges may need to be metallic. Albemet (aluminum-beryllium alloy) is an option, which would maintain the same X_0 as CFRP. Cost versus X_0 needs to be studied.

Termination Ring

The Termination Ring is intended to replicate the mechanical interfaces of the current cone system, i.e. the mounts to the TPC and to the existing installation rails used to insert the cone system. It is most likely a machined aluminum ring that will be bonded to the structural shell.

As does the transition cone, the termination ring also contributes to holding the ESC/WSC round. As its radial extent is limited to be the same as that of the current cone's termination rings, an auxiliary radial stiffening plate will be required at each end to help resolve the point loads into the shells of the ESC/WSC. The interface to this stiffening plate is intended to be compatible with all service exits and independent removal of the stiffening plate for various service scenarios, in the case of the FGT, also removal/installation of FGT disks. Due to a desire for shared interfaces, this will be true for both sides. The implication is that the interface must 'force' the transition

ring to be round via tapered pins or some absolute reference/interface to maintain the global shape/deflection of the IDS should one of the stiffening plates need to be removed and re-installed.

Support of the IDS to the STAR TPC is a functional part of the termination ring. As mentioned above, this will be modified to allow for more independent adjustment of the IDS position. Currently, all motions are coupled, i.e. are not independently orthogonal, and the current cone is over constrained in more than 1 DOF. The new support will be '4-2-1' i.e. 4 vertical, 2 horizontal and 1 "Z" constraint, so only over-constrained in the 'vertical' dimension.

E-Field Shroud

Initial field calculations indicate that a 4 cm or greater radius is required at the |Z| extent of the ESC/WSC to meet field requirements if the surface is at ground potential. The goal of the shroud design will be to exceed this radius and project down to just outside the SSD radius to support an EMI/field cover for the SSD.

The structure of the shroud will be fiberglass with a high dielectric matrix (Cyanate Ester), which is also common to all of the other structures (it also has high radiation tolerance). The outer conductive layer is undetermined, but proposed to be metalized fiber rather than conductive paint to reduce chance of contaminating debris within the IFC. The need for bias will likely require some development of this laminate in addition to its interface to the structural shells of the ESC/WSC.

OSC (Outer Support Cylinder)

The OSC replaces the elliptical beams of the current cone structure. It spans the gap between the ESC and WSC and carries the moment load between them. It is designed to have the same amount of material as the current beams, but spread over a cylindrical region of volume. Its stiffness will match the current beams for vertical deflection, with the added benefit of also providing the same stiffness horizontally.

The OSC will (eventually) include the supports for the SSD, as well as any strain reliefs for its services. A benefit of the OSC being a cylinder as opposed to the previous elliptical beams is it allows the SSD ladders to be directly mounted to the outer surface of the OSC. This presents several benefits for the SSD, and generally the STAR inner tracking performance. The relatively massive aluminum support rings for the SSD can be eliminated, saving mass in front of the FGT, and near the edges of the TPC. The SSD ladders can now be independently mounted or removed increasing serviceability. The SSD coverage can be optimized to maximize hermiticity over the previous layout, which had sizeable and non-phi-symmetric holes in coverage.

Additionally, the OSC separates the gas volume of the HFT detectors from the IFC, so if the IST and/or Pixels must operate at other than ambient temperatures, the SSD and IFC will be isolated from their environments.

As the OSC carries the primary moment load of the IDS, the global stability of the IDS is sensitive to its 'thickness' dimension. The present analyses (SEE APPENDIX) treat all lamina as isotropic materials, roughly equivalent to Titanium, with the density of Carbon Fiber. The only way to change the stiffness of the OSC was to change its thickness. With composite materials, another dimension is available, i.e. fiber orientation. The overall thickness of the OSC is currently '1 mm Titanium Equivalent'. It is likely that a moderately thinner, oriented CFRP laminate will provide the same or greater stiffness.

MSC (Middle Support Cylinder)

The MSC (shown in Figure 79) is a stepped cylinder in form and is the primary integrating structure for the PXL and IST detectors. It is supported by the IDS via its east end (west end under consideration). It is composed of two cylinders and a transition plate. The transition plate is the primary interface to the IDS.

The smaller cylinder supports the IST, PXL Detector and new beam pipe. The IST is supported on its outer surface via individual stave mounts. The PXL Detector is supported by 'Kinematic Mounts' integrated into the MSC small cylinder. The beam pipe is supported on both ends of the MSC small cylinder, on the West end by a flange and the East end by a longitudinal plate, integrated with the transition plate, that allows for longitudinal expansion during bake-out.

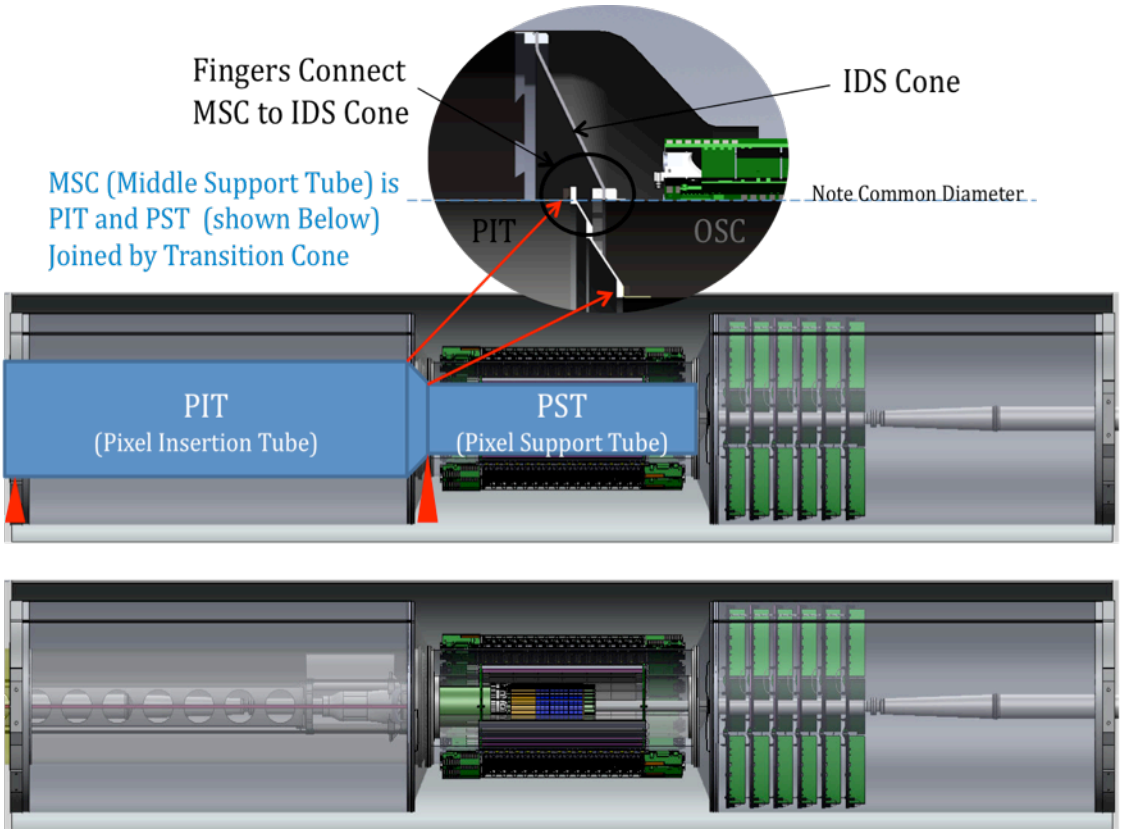


Figure 79: Middle Support Cylinder.

The smaller cylinder is cantilevered off of the ESC via the transition plate, which is attached to the larger cylinder of the MSC. The larger cylinder supports the IST services on its outer surface and the PXL insertion rails on the inside. The length of the larger cylinder will be optimized to facilitate PXL Insertion. It is planned for the larger cylinder to share diameters with the OSC, minimizing tooling for shells and flanges.

The MSC also performs as an environmental enclosure for the PXL system, forming the return ducting for the PXL air cooling system. The IST will be on the outside and in a separate gas environment. The support of the beam pipe on the far end of the PXL detector (west) will also serve as the gas return/seal for the PXL environmental gas.

The FGT requires an enclosed volume for its cooling air, which is currently a separate structure. This may be integrated into the IDS thus providing a support point for the west end of the MSC.

4.5.2. Assembly Sequence

There are two configurations of the IDS required for HFT. The first allows for the PXL Engineering run with FGT in Run-12, the second is the complete HFT (PXL, IST, SSD) configuration slated for Run-14. All of the structures described above, IDS, E-Field Shrouds, and an MSC are required for both run configurations, however mounts and services for SSD and IST are not required on any of the structures for Run-12, implying that pre-production MSC and OSC structures could be used for Run-12. The following assembly sequences will illustrate why pre-production versions should be used for Run-12 and later production versions of the MSC and OSC should be used for Run-14.

There will be two opening events planned for STAR, first to install the HFT PXL Engineering system and FGT for Run-12, and later to install the complete HFT system (SSD and IST) along with PXL for Run-14. All subsystems (IST, PXL, SSD, and FGT) desire some extended commissioning prior to installation in STAR, implying availability of integration structures several months prior to installation. Installation of either configuration of the IDS in STAR is tied to a STAR Opening, so are necessarily on the critical path for RHIC shutdown. The primary integration structures for SSD and IST, OSC and MSC respectively, are required for Run-12, meaning that they are installed in STAR. Preparing these detectors for Run-14 also requires an OSC and MSC allowing both SSD and IST to commission externally to STAR several months prior to STAR opening.

For Schedule purposes, it is highly desirable to produce two versions/copies of the MSC and OSC to allow assembly and commissioning of the IST and SSD in parallel to Run-13 so that they are immediately available for integration into the IDS as soon as it is removed from STAR after opening, reducing time on the critical path of the RHIC Shut down.

The aim of producing copies of the structures is to minimize the number of components that need to be recovered from the configuration installed for Run-12 prior to onset of integration for Run-14. All components installed in Run-12, required for Run-14, places the effort for their recovery (disassembly) and later integration/assembly/test on the critical path of the preparation for Run-14.

One thing common to all assembly scenarios is that the beam pipe must be supported adequately along its length with tooling that allows various transitions of loads to let the various cylinders pass over it. Lengths of these cylinders (MSC/OSC/ESC/WSC) may require either cantilever or ‘reach-thru’ tooling to guarantee safety of the beam pipe, and leak-tightness of subsequently inaccessible vacuum flanges. Tooling is not yet designed, but it is likely that all operations involving the beam pipe, from initial integration of MSC thru integration of the IDS will be on a common tool of approximately beam pipe length.

The beam pipe is a BNL deliverable with many auxiliary processes. The beam pipe, its delivery to STAR, and auxiliary requirements, will be described later, however it is important to know that the new beam pipe is envisioned to be 3 parts, a middle section of small diameter with a Be middle, then two end pieces with conical transition to larger diameter.

Initial IDS Assembly

It is assumed that the FGT will be pre-integrated into the WSC; for further purpose of this discussion, WSC and FGT are synonymous. Neither the SSD nor the IST are available for Run-12. The FGT will have been previously integrated into the WSC and the main goal of this assembly procedure for HFT is to incorporate the beam pipe with the MSC, and insert that structure into the ESC, mount the OSC and attach these to the WSC. The PXL insertion happens after the assembled IDS is inserted into STAR. PXL Insertion is currently described in the PXL Mechanics Section 4.2.3. Following is a presentation of the order of assembly. Some activities may happen in parallel, but this represents the basic order of assembly—note that this is aimed at the assembly required for Run-12; sequence for Run-14 will follow.

New Beam Pipe integrated with MSC.

This can likely be completed prior to STAR being opened, but depending on beam pipe delivery, may need to occur in parallel with assembly of the IDS. Ideally, this would have been dry fit at LBNL prior to arrival at BNL.

As mentioned above, the integration of anything with the beam pipe involves a tool which fully supports the beam pipe. The base procedure is that after the beam pipe is supported in the tool, the cylinders are passed over it transitioning supports. First the small cylinder of the MSC is passed thru to the middle, where the beam pipe is attached to supports at both ends of the cylinder--the cylinder then takes the load of the beam pipe, and has its load transferred to the tooling

The beam pipe flange that transitions to the larger diameter section will be in the middle of the larger MSC cylinder which comes next in the assembly of the MSC. The beam pipe section of larger diameter with the conical transition is of longer length than the MSC Large diameter cylinder. The beam pipe extension will be introduced simultaneously with the Large MSC Cylinder so that it can be supported on both ends for mating to the Be section of the beam pipe. After mating, but before joining the MSC together, the beam pipe flange must be leak checked, perhaps allowing for 2+ days to pump down and check. Space must be allowed for pure gas purge and full access to the flanges setting some limits on the interplay between lengths of MSC large cylinder and beam pipe extension.

The larger cylinder of the MSC is then bolted to the transition flange to the MSC small cylinder. An auxiliary support from MSC to beam pipe is installed. The beam pipe is now only supported by the MSC internally and the Tooling Externally.

This procedure yields the beam pipe supported by the MSC, and ready to insert into the ESC (and perhaps test insert PXL on the same bench (longer length required).

MSC into ESC

The ESC will have been prepared in parallel to the previous integration and mounting the MSC/beam pipe Assembly into the ESC can proceed immediately. Similar to the MSC integration, the beam pipe and thus the MSC must be fully supported. As the MSC supports the beam pipe, some tooling that reaches thru the ESC as it passes over the MSC may be required. Alternately a study of how to cantilever the MSC (likely possible) will be conducted to minimize tooling cost. The primary driver for ‘inserting’ the MSC into the ESC is support of all elements during assembly.

OSC over extended MSC

Once the MSC is joined with the ESC, the OSC can be installed over the small cylinder of the MSC. It is shorter than the ESC so can either share the same tooling or benefit from the increased stiffness/cantilever possibility of the ongoing assembly. The tooling should be designed to allow for an SSD in this configuration, but as this will be two years hence, the tooling can be simplified somewhat, perhaps even done by hand considering the absence of any sensitive silicon.

WSC attached to OSC

Introducing the WSC to the combined structures of ESC/MSC/OSC is similar to the assembly of the MSC with the beam pipe. There is a flange in the beam pipe which will be covered by the WSC. The WSC is similar in length to the large diameter cylinder of the MSC so the procedure will be similar, though necessitates tooling on the West side; either as an extension of the tooling or included previously in the overall tooling length.

As soon as the beam pipe has been leak checked, the WSC can be bolted to the OSC. Once WSC is bolted to the OSC west end, the IDS is complete and nearly ready for insertion into the IFC

Shroud Installation

The East end of the shroud could be installed as soon as the ESC is installed over the MSC, but likely both sides will be installed simultaneously. The Shrouds are necessarily half shells, so they can be installed around the pre-assembled IDS. They will be attached to the ESC/WSC via some form of film backed PSA (tape), conductive or not, and their halves joined similarly. If a bias voltage is required, appropriate terminations and various and sundry resistance testing will be conducted. It is unclear if a further cylindrical cover, normally meant to cover the SSD, now not present, is required. This will likely depend on whether and how the shrouds are biased.

Once Shrouds are fully installed and properly tested, the IDS is fully ready for installation

Installation into STAR IFC

Intention is that IDS identically replicates all current ‘cone’ interfaces for installation up to how it mounts to (is supported by) the TPC. All steps used to insert/remove the current cone structure should remain valid; only transfer of the load of the IDS to the TPC wheels should differ. The transfer protocol is currently TBD.

PXL Detector

PXL Insertion into the MSC is covered in the PXL Mechanics section of this document. In the interest of covering requirements related to Integration, the HFT PXL detector is included here.

The engineering run for the PXL detector will need to be commissioned simultaneously with the FGT, likely requiring space in the clean room and access to DAQ, Power crates and some method of cooling (ducted air system). This capability, and space requirement, needs to be maintained throughout the duration of the HFT project to support the later commissioning of the final PXL System.

Obviously, some time to terminate (plug in and test connection of) the PXL Services will be required after full STAR closure. It is currently unclear where external PXL Services run, i.e. inside or outside of the Magnet Return Iron, thus uncertain where in the schedule this activity occurs.

Final HFT Assembly

The discussion in the chapter below assumes the integration for the engineering run takes place before RHIC Run-12, and the final installation before Run-14. As discussed in the cost and schedule section this may in fact take place shifted by one year, either one of those or both. Though the sequence and the procedures for assembly remains the same.

Run-14 will include all HFT deliverable detectors, PXL, IST and SSD. The PXL system will provide the next generation of their detector in entirety with mechanics to allow for insertion after end of Run-13. The PXL System also requires something similar in form/footprint or identical to an MSC to properly cool during system testing. The IST and SSD will be integrated (assembled), surveyed and commissioned prior to the end of Run-13 in preparation for installation for Run-14. All of these activities will require space in the clean room for any operations involving exposed Silicon. The clean room is also a primary resource for access to STAR DAQ and similar infrastructural requirements during the commissioning of these detectors. The commissioning of these detectors is foreseen to start during Run-13 and continue thru final integration into the IDS in preparation for Run-14.

To integrate the full HFT into the IDS several structures involved in Runs 12 and 13 will need to be recovered from the IDS after conclusion of Run-13 and before onset of Run-14. This operation—recovery of, and integration with, structures that will comprise the IDS for Run-14 are on the critical path of the onset of Run-14. Presently, these recovered structures include the ESC and beam pipe. Additionally, the FGT desires to run without the integrated SSD services in the WSC for Runs 12 and 13. The implication is the required removal of the FGT from the WSC to then install the SSD Services followed by re-installation of the FGT. This activity is included in the STAR opening between Runs 13 and 14. It is likely that the FGT would desire maintenance/upgrade during this opening so this is likely off of critical path, but installation of SSD services needs to be included in the HFT Project at this point in the schedule. An auxiliary point is that at this time, the IST, PXL and SSD mostly occupy the Clean Room. FGT may require an auxiliary clean room or force HFT into requiring the same.

A detailed schedule for the activities required during Summer 2013 (prior to Run-14) does not exist. The designs and activities proposed are aimed at minimizing the activities and thus duration required. This factors into the need for auxiliary/replicate structures for the MSC and OSC to allow commissioning/survey of PXL, IST and SSD prior to opening STAR after Run-13. Co-habitation with FGT or other ancillary STAR activities is not addressed.

The following description of HFT assembly will start first with activities, which precede the STAR opening at end of Run-13, and follow with actions required to recuperate required structures, and re-assemble the detector in preparation for Run-14.

PXL Integration

The PXL System is designed to be entirely independent from the global HFT structural assembly—it is meant to be inserted or removed during STAR run configuration. The primary impact of the PXL System on this phase of the assembly is occupancy of the Clean Room. As mentioned above, it will require facilities similar in size to the MSC. Preferably an auxiliary MSC for test insertion and cooling, in addition to similarly sized space upon removal.

IST Integration

The IST Staves are individually attached mechanically onto the outer surface of the smaller MSC cylinder. At this point it can be surveyed, given survey capability at BNL. It is assumed that

Staves are previously tested individually, but 'commissioning' as an assembled array will not occur until they are assembled onto the MSC, preferably with its final internal service plant.

The IST Services are supported by/attached to the MSC large cylinder. As mentioned above, the beam pipe must be assembled into the small cylinder prior to attaching the large cylinder. It is possible to commission the IST with its 'permanent' service chain, but to install the recovered beam pipe, complete disconnection of this tested and commissioned service chain is required to allow installation of the beam pipe recovered from Run-13. Re-connection and sufficient testing of these connections would be required on the CP of the opening between Runs 13/14.

It is pre-supposed that an additional MSC structure is available well in advance of the end of Run-13 to allow dressing and commissioning of services for the IST.

SSD Integration

The SSD is assembled onto the OSC. 'An' OSC is required for Runs 12/13 to bridge the gap between the East and West Support Cylinders. The SSD needs to be assembled and surveyed as a unit on an OSC, and ideally commissioned in this configuration. It is unreasonable to assume that this could occur after recovering the OSC used for Runs 12/13 and before onset of Run-14, thus it is desirable to fabricate an additional OSC with SSD mounts in preparation for Run-14.

The SSD ladders will be assembled onto an OSC and surveyed, either at LBNL or BNL, perhaps both to allay shipping concerns. The SSD Permanent External Services are not available for commissioning as they are integral with the ESC and WSC—these will have to be installed during the opening between Runs 13 and 14.

MSC Integration

This is very similar to the initial integration, but needs to wait for the recovery of the central Be section of the beam pipe after the IDS is removed from STAR (requires basically complete disassembly of installed IDS). In parallel, the IST services can be disconnected, and MSC large and small cylinders separated. After recovery of the central beam pipe, the assembly process follows identically that above.

Tooling may need to be modified to account for the presence of Silicon and Services. After Termination of beam pipe and Small to Large MSC Cylinders, some time to re-test/commission the IST is required. This should not require disassembly of the structure, but may require replacement of some IST Services and re-testing before moving onto the next step.

MSC into ESC (ESC over MSC)

As the IDS must have been completely disassembled to even begin the MSC integration, the ESC is obviously available by when this occurs, however, some time must be allotted to allow for integration of the SSD Services into the inner surface of the ESC. It is possible that this can occur in parallel to the aforementioned activity (MSC Integration), but additionally available manpower will be required.

The procedure is identical to the one for initial installation, however should occur in a 'clean room'. It is not likely that this can occur in 'the clean room' in the STAR Assembly Hall, but should occur in a moderately protected environment as the IST represents exposed silicon and wire bonds.

There is sufficient space in the clean room to accommodate this action, but unclear if previous tooling used to assemble IDS with beam pipe will fit into clean room. The previous (initial)

assembly of the IDS was not done in the clean room due to PXL/FGT occupancy and no exposed silicon. It is likely that an external 'clean' or at least 'protected' environment will be required for this assembly procedure.

OSC onto ESC

The OSC and SSD at this point are mechanically integrated. The goal of this operation is to structurally attach the OSC to the ESC, followed shortly by the attachment of the WSC. Unlike the IST, the SSD will not present exposed silicon or wire bonds. This operation can largely be in the open on the assembly hall floor. It is desirable to protect and cover the area to prevent entrainment of contaminants from ceilings, cranes, and various wildlife from imposing on the exposed detector surfaces.

WSC attached to OSC

This basic mechanical procedure is identical to the procedure described for the initial installation. The WSC and beam pipe will have been recovered from Run-13, and the FGT will have been refurbished, hopefully all in the time it took to get to this juncture in the schedule. As with the ESC, the WSC will require installation of the SSD Services. The WSC can lag on this the proximal time it takes to integrate OSC to ESC, but again points toward additional manpower to minimize schedule impact.

SSD Service Termination

The ESC and WSC both carry either side of the SSD Services. All cooling connections are available on the ESC and could start as soon as the OSC is attached to the ESC, however the SSD requires services from both sides to be fully operational due to the design of its service chain. Full testing of the SSD cannot occur until the WSC and the related SSD services are available.

SSD will require a nominal time to verify that all services are properly connected before onset of covering it's connections with the E-Field Shroud, after which all service connections will be inaccessible

E-Field Shroud Termination

These structures will have been the first recovered from the Run-13 opening. Additional structures will be provided in case of damage during removal—these will be very low mass, thus fragile objects. Mounting, or re-mounting the shrouds will entail some clean-up of the surfaces (previously taped) to assure proper electrical contact and no aberrant asperities.

Attaching of the shrouds can only follow sign off of acceptable SSD connection. Following that, appropriate electrical conductivity (or bias stand-off) tests must be conducted.

Insertion of the Cone into STAR

This is fundamentally equivalent to the current procedure, so should both follow the existing procedure and use current tooling.

Additional operations to terminate the IST, SSD, and FGT to service chains that move with STAR will be completed after STAR is installed on the beam Line.

PXL Insertion

The PXL installation procedure is designed to occur while STAR is in position on the beam line after beam pipe termination and bake out. There is no reason to believe that the PXL detector would ever install with STAR removed from the experimental hall.

Every effort will be made to assure that the PXL detector can be installed within a period shorter than 24 hrs, preferentially 8 hrs, including modification of detector supports of the east BBC for quick removal and reinstallation to gain access to the PXL installation volumes.

Functionally, the PXL detector halves are introduced from either side of the beam pipe on an external platform replicating the installation rails internal to the MSC. This platform is aligned to the internal rails, and the PXL system pushed in, perhaps with additional articulation around external interferences. After insertion, the MSC is sealed to the PXL Package, and its services terminated to the external service plant.

Assembly Area Requirements

As mentioned above, several of the operations may require extended length, and perhaps a clean/semi-clean environment. Clearly, installation of the ISC with or without the IST will require the most length. If possible, it would be desirable to move the removed cone to a location where it can stay for all operations, including initial assembly and any FGT related actions.

The final version of the PXL system will likely compete with the IST/SSD for clean space. The IST will require a clean space to assemble, and test its staves on the MSC. The PXL System will require a similarly clean space to test the new electronics for installation after the engineering run.

4.5.3. Beam Pipe

HFT requires a new beam pipe. The PXL System's innermost radius is smaller than the currently installed beam pipe. The new radius required is identical to that proposed for PHENIX, and thus agreed to by the RHIC Machine interface. The proposed beam pipe has the same length and flanges as the current beam pipe so represents a direct replacement. The primary change is a necked down region surrounding IP. The small diameter region will be thin beryllium (0.8 mm wall) to a length, which is beyond any acceptance of currently installed STAR detectors. The remainder of the beam pipe will be aluminum.

Mechanical

STAR/HFT will be responsible for the mechanical design and layout of the new STAR beam pipe, in consultation with Brush-Wellman, the most likely vendor, and with sign-off from the Collider Accelerator Department (C-AD) of BNL.

The layout, primarily beryllium length, has been optimized to ensure that the beam pipe thickness does not add additional material over the current beam-pipe in terms of radiation length for vertices in $-30 < z < 20$ cm and $-1.5 < \eta < 4$. Transitions to larger diameter are limited on one side by the articulation of the PXL insertion. The other side will transition to larger radius after the Be section, perhaps with some Aluminum transition TBD after consultation with Brush Wellman. The Be section is detailed in Figure 80.

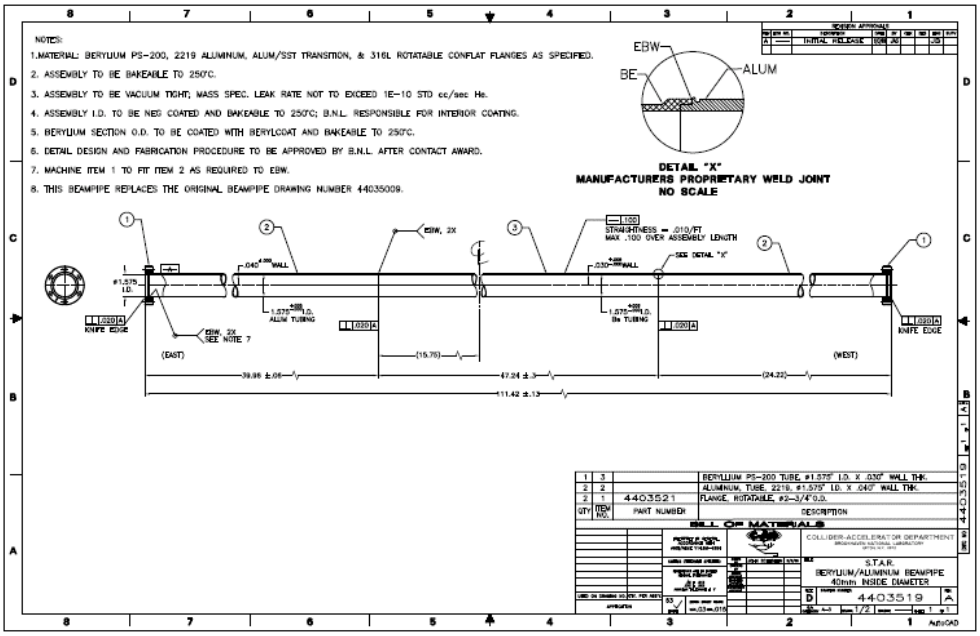


Figure 80: Small diameter beam pipe with Be mid-section.

Bake-out Considerations

The beam pipe will have a NEG coating, which must be activated after the beam pipe is terminated and evacuated. The required bake out temperature is up to 250°C. The PXL Detector is not compatible with this temperature so must be removed during bake out.

It is intended to have insertable bake-out jackets for at least the PXL section (small diameter) of the beam pipe. It is possible that these insertable jackets might also use the same insertion mechanism as the PXL detector, but this mechanism only exists on the east side.

It is proposed that all large diameters of the beam pipe have integrated bake out jackets, similar to those installed on the Be beam pipe of ATLAS. These are heaters laminated directly to the beam pipe, and insulated to keep heat egress to a minimum.

Support

The beam pipe will be relatively fragile, so must be adequately supported during all assembly operations and adjustment within the detector volume. It is assumed that the beam pipe will move with the Support Cone Structure. Any beam pipe adjustment will occur solely by adjusting the position of the support cones within the IFC. As such, the beam pipe will be rigidly supported ultimately to the Support Cone Structure.

Wheels Assembly

As mentioned above in the section on assembly, the beam pipe must be supported adequately during all phases of assembly. This will require a tool mimicking the final support condition, but with auxiliary attachments to allow transfer of loads. Design of this tooling will need to consider safe load limits during all modes of load transfer

Final Support

The beam pipe will have 4 primary support points. Two near IP and two at the extremities of the TPC, all will move with the Support Cone Structure during any STAR movements, and transfer to the external (current) STAR supports after STAR is on beam axis

Two permanent supports will be incorporated into the MSC. The two innermost supports will be directly to the MSC small cylinder to either side of the PXL detector as installed. One of these, the one around which the PXL system must be installed, will need to be only vertically oriented. Because the beam pipe requires stability in all directions, this support must also provide some bending stiffness, thus have some thickness. The other support on the small cylinder (west), opposite the insertion side of PXL needs to also seal the gas volume of the ISC, so can be disk like. Adaption to flanges incorporated into the beam pipe is foreseen.

The temporary east support, will be to the large cylinder of the MSC which in turn is supported by the ESC. After STAR is on axis this can be transferred to the current external support

The far west support will be terminated after the beam pipe is inserted thru the WSC. This will be directly to the WSC and can similarly transferred to the current external support after STAR is on beam axis.

4.6. Software

This section contains the description of the software elements required for the successful processing and analysis of the acquired raw HFT data. Since the HFT is an upgrade detector of the STAR experiment, its software needs modules to be incorporated into the existing software and computing environment of the experiment. After a brief discussion of STAR's software environment, we list and describe the online, offline and simulation modules and tools that are required to be developed for the HFT. We will finish with a discussion of resources and institutional software responsibilities and commitments.

4.6.1. STAR Software Environment

The STAR software environment comprises of a set of tools (development, simulation, production and analysis environment), mainly in the form of plug-in software modules in a ROOT – based backbone interface. At the same time it provides the data model and the coding standards and the data model for new module development and integration in the top-level shell scripts. Each detector subsystem is responsible for the development of all modules necessary for its successful operation. New, major pieces of code need to be reviewed and approved before insertion in the main repository. This work is coordinated with the rest of the experiment through a designated software representative from the group. At the same time there is a software infrastructure group based at Brookhaven National Lab (BNL-core), that maintains and manages critical pieces of code (tracking, calibrations, databases) and also provides help with the integration of new software in the system.

Online Environment

The online software primarily ensures the data integrity during data acquisition via appropriate detector monitoring and sample event reconstruction. Beyond these basic but important tasks,

and as computer processing capabilities improve dramatically, more and more formerly offline tasks move to the online environment. One such task is the hit finding in the STAR TPC. Discussion has started on the possibility for online (pre-) tracking in the TPC. This is of particular interest to this group since we plan for on chip PXL clustering and hit finding for the PXL detector.

Offline Environment

The offline environment consists of the event reconstruction software packages. This starts with the raw data as input and through proper calibrations it proceeds with detector cluster/hit finding, integrated tracking, event vertex finding and event information writing on DSTs.

4.6.2. Online Software

The online software serves as a tool to monitor detector performance. It is also used to perform online calibrations where possible. Online software is detector specific and is described in Section 4.2 for the PXL, in Section 4.3 for the IST, and in Section 4.4 for the SSD.

4.6.3. Offline Software

Hit Reconstruction

The Cluster/Hit finder is the first piece of code applied to the pedestal subtracted raw information from the IST and PXL detectors.

In the IST detector this will be a standard search for all fired strip-lets, i.e. all strips with a pedestal subtracted ADC value above a cut/threshold value (typically a value two to three times the strip noise-RMS level. Groups of adjacent strips that are fired will be clustered and further analyzed by a peak finding program for one or more possible hits. Every such 'hit' is then first going to be assigned a set of local/wafer coordinates based on the strip's position on the wafer. This will be followed by a local-to-global transformation to STAR global coordinate system (detector hit information needs to be saved in global coordinates), which is usually done via a series of partial transformations (wafer to ladder, ladder to shell, shell to detector, detector to STAR). This is common practice in silicon strip detectors and the MIT group, which will build the detector, has extensive experience in this area.

In the PXL detector the first steps (Cluster/Hit finding) are incorporated on the chip's logic, i.e. done online during data acquisition, as discussed in Section 4.2. The local to global transformation process is identical to the IST even though the partial transformations will be different in order to incorporate the specific geometry and the specific hardware-implemented alignment features of the PXL detector (see discussion on Alignment below and in Section 4.2).

Tracking

The current STAR reconstruction environment provides a Kalman-filter based integrated tracker. This tool is in principle ready to accommodate and integrate the IST and PXL hits, with their proper error per weight, in its environment. In reality work and close collaboration with the BNL-core group will be required to tune the tracker's parameters and optimize its performance. For example it has to properly handle the high precision information coming from the PXL layers.

Also, there is a need to develop methods to deal with the path ambiguities in the SSD and IST (effective strip 'hits' with relatively large errors in the long strip direction), as well as dealing with the ghosting in the PXL detector due to out of time events in a high luminosity environment. Dealing with the latter two problems of tracking/ghosting will require studies that use a several-passes tracking approach and/or knowledge of the triggered event vertex obtained from a first-pass (or quick) vertex finder. This is a critical item, which will finally determine the physics performance of the system and therefore needs special attention and effort.

Event Vertex Reconstruction

Currently STAR deploys two different event vertex finders during event reconstruction, one for heavy ion and one for proton-proton collisions. Each of them is specifically tuned to perform best in these completely different environments (high multiplicity w/out pile up in heavy ions and low multiplicity with high pile-up in p-p). In a typical heavy ion collision the TPC has to cope with events of relatively large multiplicity and virtually pile-up free whereas in p-p one needs to extract the primary vertex from a few primary tracks surrounded by a thousand of out of time (pile-up) tracks. As a direct consequence of this fact STAR uses a Minuit-based event vertex fitter (with a seed finder) in heavy ion collisions. For p-p the vertex fitting procedure is based on a chi-square minimization method but, most importantly, the information from fast detectors is used to select (tag) the tracks that belong to the triggered event. Only these tagged tracks participate in the event vertex-fitting step.

In the RHIC-II era's increased luminosity there is going to be pile-up in the TPC but most importantly in the two PXL layers of HFT due to the relatively large integration time of the detector (see Section 4.2 and also *Pileup* discussion below). This will be the case in both p-p and heavy ion collisions. The SSD and IST are assumed to be pile-up free even for the highest rate p-p collisions. The presence of these two (as well as the other) fast detectors will require a new, revised version of the vertex finder that will combine the best features of both current finders. At this point we do not anticipate the need for any new functionality, just the need for tuning and QA-ing the new/combined finder.

We should note here that the mid-term plans of the reconstruction/infrastructure group include the deployment of a Kalman filter-type vertex finder, which at the same time will do the primary track fitting. In high multiplicity events (>30 tracks or so) one can perform without loss the vertex finding/fitting and primary track fitting (i.e. fitting global tracks with the vertex as an extra point on track for tracks with DCA within a cut value, e.g. currently 3cm, from the vertex. This will be revised in the HFT era due to much higher precision in pointing.) in two separate steps. In low multiplicities it is generally better if one performs a simultaneous fit of primary tracks and event vertex. This is worth exploring. Let us remember that the larger fraction of the secondary/decay vertices we are trying to resolve are in the range of 10-100 microns and any improvement in determining the event vertex (the most important single reference point in the event) is indispensable.

Secondary/Decay Vertex Reconstruction

The reconstruction of short-lived particles in a collider environment is an extremely challenging task. The key measurements of HFT involve the reconstruction of D- and B-mesons with typical $c\tau$ in the range of 120 – 500 microns, and Λ_C with a $c\tau$ of 60 microns. The lack of a Lorentz boost typically results in mean decay distances of about half the $c\tau$, for decays at mid-rapidity of a properly p_T weighted sample. For example, the anticipated mean p_T for D_0 mesons in Au+Au collisions at RHIC is about 1 GeV/c. This is a conservative estimate taking into account expected

high p_T suppression effects. The $\beta\gamma$ factor for a mid-rapidity D_0 is 0.54 and thus its mean decay distance ($c\tau$ of 120 microns) is about 65 microns. For a 1 GeV/c Λ_C baryon this will be about 30 microns. This environment demands the highest level of sophistication in the methods used to reconstruct the decay/secondary vertices.

Up to now, the STAR secondary vertex reconstruction code had to deal with decay vertices of strange particles, typically in the few centimeters range. For those distances, simple geometrical reconstruction models coupled to crude, fixed value cuts were sufficient. Only a recent effort to reconstruct D-mesons with the SVT, the first generation silicon vertex detector in STAR, started deploying decay vertex fitting techniques using the full error information of a track, on a track-by-track and vertex-by-vertex basis (sometimes also called μ-Vertexing). Cuts like the decay length are not fixed values but rather a number of standard deviations of the fitted value. This way the cuts are less biased especially the one, like DCA, which have strong momentum dependencies. This work, currently still under development, will be the basis of the modules deployed on the HFT data. These important software modules are to be developed, as they are a key piece of the new software.

Databases – Calibration and Alignment

The accurate monitoring and recording of the state and the position of the detector inside the STAR apparatus is of outmost importance as it directly impacts its performance. Calibration is the online and offline task of monitoring the state of the detector. The online part (often referred to a slow controls) gathers information of the detector in-situ, usually during running periods. Such information might be temperature or position of elements, pedestal files etc. This information is stored in a Database with a timestamp. The slow controls for the SSD, IST and PXL detectors are discussed in Sections 4.4, 4.3 and 4.2 respectively. The offline part of the calibration includes also software methods used to check e.g. the position of the detector elements using tracking information. The results of these procedures are stored as updated values in specific bank in the Database and are used in the massive offline physics production reconstruction passes.

The task of Alignment is a very demanding one especially for the PXL detector where one would like to perform/know the positioning of the detector elements with offsets and tolerances to within a few microns.

The alignment of the SSD and IST is not a challenging task provided good survey data has been collected of the detector's elements beforehand. The in-situ alignment will be done with software techniques (global and/or local alignment) and there is previous experience on this in the collaboration. All it is required is to bring the SSD (IST) hits within the TPC (TPC+SSD) track projection errors to the detector layer, typically around 100 microns or so. Global alignment techniques usually yield results accurate to about 10 microns using a set of only a few hundred thousand tracks. Rotations are also typically kept to a fraction of milliradian.

In the PXL detector this task is more difficult and the designers of the detector decided early on to incorporate 'hardware' techniques in order to minimize element displacement in-situ. The PXL detector is designed with a 20 μm 'envelope' error, i.e. maximum allowed displacement in-situ. To achieve this various sophisticated methods have been developed, e.g. interlocking, easily replaceable pre-surveyed shells with extreme precision on-bench survey data. Details on the method and the specific hardware implementation can be found in Section 4.2.

Despite this excellent 'hardware pre-alignment', software methods will have to be deployed in order to both check and fine-tune the in-situ information of the detector elements. There are two categories of software alignment techniques, the so-called Global and Local alignment.

The *Global* alignment uses TPC (+SSD+IST) track information on a statistical basis in order to obtain systematic silicon detector rotations and shifts. Typically a 'rigid body' model is applied (i.e. ignoring possible ladder twists, sagging effects and wafer non-planarity) and a misalignment model is introduced. Then a Taylor expansion with respect to misalignment parameters (3-D shifts and 3-D rotations) is performed looking for deviations of measured hit position from predicted primary track position on a measurement (wafer) plane. The track prediction comes from the detector(s) used as reference, e.g.\ initially the TPC alone, and later the combined TPC+SSD (+IST) tracking. In the next step, from the hit deviations distribution, a misalignment parameter has been calculated as a slope with a straight line fit. A global least-squares fit is also simultaneously performed on all available information. The method is applied iteratively until the fitted parameters reach stability. This global method was first applied to TPC+SSD+SVT data in STAR and it is well developed and understood. It will serve us in the IST alignment but it will need modifications for the PXL detector. This is because the PXL elements (wafers) on a ladder will have deviations from the 'flat plane' hypothesis.

In a *Local* or *Self*-alignment method one aims at the most precise *relative* placement of the detector elements. In this procedure only high precision hit information is used coming exclusively from the detector under local alignment. A successful method using the event vertex constraint was developed and tested on simulations by the BNL-core group and this should be further developed into a working module with data for the HFT complex.

4.6.4. Simulation Framework

The current simulation framework in STAR is based on GEANT-3.0 with custom script extensions to facilitate detector geometry implementation and event generation. It also includes event generators like HIJING, PYTHIA, Phase-space etc. that are interfaced to GEANT. This framework is soon to be abandoned and will be replaced by a ROOT-based geometry and tracking package (VMC, Virtual Monte Carlo). Nevertheless, we are still using it and we will continue to do so in the immediate future. The tasks, and therefore software modules one needs to develop here are: a) the **detector geometry** definition, b) the **detector response** packages (fast and slow simulators), c) track **embedding** in real/raw events, d) a hit **pileup** handler, e) the Association Maker and structures for **evaluation** purposes, and f) Physics **analysis** code (performance, physics etc) capable of handling and evaluating the resulting information. Our group will have to contribute modules and effort in all these categories. It is worth mentioning here that besides this full and detailed simulation chain the group has developed very useful tools for quick estimates of various detector configurations, resolutions, layouts etc. These tools, sometimes referred to as 'hand calculations' or 'fast Monte Carlo' will keep playing an important role when either a quick turn around is needed or for cross checking purposes.

Detector Geometry Definition

This task is to include in the GEANT-simulated apparatus of the experiment the latest and most accurate/realistic geometry of HFT (IST and PXL), since this is the only way to ensure reliability of the resulting efficiency numbers. This task also includes the definition of the active areas of the detector, the hit information and the global positioning matrices of the detector. It has been recently realized that for certain studies (e.g. layer optimization studies, overall tracking efficiencies, 'quick' feasibility studies etc), a simplified version of the geometry could be very useful, a version where average material thickness is included but without detailed outline of the discreet components (cables, ICs, ladder support etc).

Detector Response Simulators

The detector response simulation packages in STAR reside outside the GEANT framework. They are actually invoked at the event reconstruction step. Typically there are two or three categories of response simulators: a) *Fast simulators*, which smear the hit position coordinates and assign hit uncertainties based on parameterized analytical functions. The fast simulators run extremely fast and are good for quick studies that do not need detailed implementation of the detector. They are also relatively easy to implement; we already have an HFT fast simulator in place for all subsystems, b) *Slow simulators,* which simulates hits at the ADC level (usually obtained from sampling parameterized response functions. A slow simulator is a must when accurate acceptance and efficiency numbers are requested in physics analysis. A slow simulator is also used in embedding as discussed below, and c) *Very Slow simulators*, which track individual electrons through the detector body; from their generation to the readout. This is usually very time consuming and one utilizes this method only in small-scale productions in order to determine or verify the functions used in the first two methods.

A Slow Simulator for the IST Detector

The technology similarities between the SSD and IST (both silicon strip detectors with similar Si wafer thicknesses but with SSD being a double-side, crossed strip detector and IST single-side, shorter strip detector) could be beneficial in developing a slow simulator for the IST. The currently under development SSD code could be modified and adapted for the IST needs.

A Slow Simulator for the PXL Detector

The detailed simulation for STAR Heavy Flavor Tracker PXL silicon detector consists of 4 steps. First, use the information of a charged particle passing through the PXL as inputs. The information contains the particle momentum, incident direction, path length in the PXL, and the sum of electron-hole pairs it generates. The total number of electrons generated from charged track passing through the silicon sensor is calculated using a Bichsel distribution.[46] Second, build the geometry of the detector: one chip of 640 x 640 PXL array. One pixel is 30um x 50um x 30um, consist of four different layers from top to bottom: Readout electronics layer, diode layer, epitaxial layer and substrate layer. Third, simulate the transportation of electrons generated in the PXL[47]: diffusion, recombination and reflection at interfaces between different layers. A Gaussian equation is used to describe the diffusion as a random walk process. The electron recombination rate is dependent on the different doping density of different layers. Finally, calculate the distribution of electrons collected in the PXL array as output signal. The left panel of Figure 81 presents the simulated pixel cluster shape from 1GeV charged pion incident at 45-degree angle. The right panel of the figure shows the comparison of the deposited number of electron profile from data [47] and simulation. The two results agree with each other very well. The major problem for this slow simulator is the speed. It takes about 20 minutes to simulate a single charged track and it comes mainly from simulating the electron diffusion process. This is too slow to be used in future large-scale simulation studies.

To significantly improve the speed while keeping good accuracy, we developed a simplified method. Instead of simulating diffusion process step by step for each single electron, we calculate the probability distribution function for each electron in a specific space location to be collected by different pixels. Since any electron generated in the PXL is independent from each other, by randomly sampling this probability distribution function, we can decide which pixel collected this electron or if the electron recombined before being collected. Following above steps, we collect the pixel IDs that absorb all electrons along a charged track and add them up to

obtain the number of electrons deposited in each pixel. To implement this method, we built a fine 3-D grid in a single pixel and calculated the probability distribution function for electron produced from all grid points using the slow simulator. For any one electron from incident charged track, we directly use the probability distribution function for the grid point that is closest to its production point to determine the pixel ID that collected this electron. Since all pixels are identical, we only need to make coordinate transformation if any electron is produced outside the PXL where the grid is built and repeat the same operation to finish the whole simulation for a charged track. The speed of the simplified simulator is a few seconds per charged track. The accuracy depends on the granularity of the grid and can be very good with high granularity.

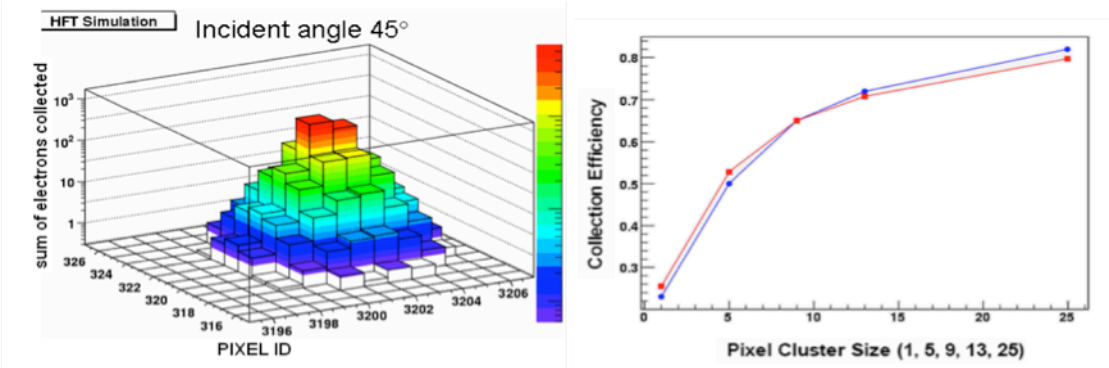


Figure 81: Left: Distribution of the number of deposited electrons on pixels from a charged pion with 45 degrees incident angle from the slow simulator. Right: Profile of the fraction of deposited number of electrons from simulation (blue) and data [47] (red).

Embedding and Pile-Up

The embedding of simulated tracks into the raw data stream (which provides the best 'background environment' for track/particle reconstruction and therefore the best way to estimate accurate efficiency numbers for physics analysis) has been around the heavy ion community for about fifteen years. It is the merging, at the raw ADC level, of a pedestal-subtracted event, for a given detector, with a few, slow-simulated hits. The resulting output is then passed through the reconstruction chain and the output is compared to MC input (this step is performed by the so-called Association Maker in STAR experiment). During the merging of real data with simulated hits and tracks one read the appropriate calibration tables so the dead areas of the detectors are properly excluded.

IST Embedding

As we mentioned above the IST could benefit from existing or under development SSD embedding code and adapt it with minor modifications

PXL Embedding and Pile-up Simulation

The embedding task in the PXL layers is more complex since cluster and hit finding is done online. Also, in simulations, one has to properly account for out-of-time events, Pile-up hits. At the projected RHIC-II luminosity of $50*10^{26}$ $cm^{-2}s^{-1}$ with vertex diamond with σ_z of 20 cm, a significant amount of pile-up from minimum-bias collisions will contribute to the hit density in the PXL layers for 200 μs integration time. The hit density at the first PXL layer will thus rise

from 18 cm^{-2} to 40 cm^{-2}, and at the second PXL layer from 2 cm^{-2} to 4 cm^{-2}. This already includes rescaling applied to account correctly for contributions from UPC electrons.

Based on these numbers and similar to CD-0, a sample of minimum-bias collisions with proper primary vertex distribution was used to obtain a sample of hits in the PXL detector layers. Ten different sets were produced to account for fluctuations in pile-up hit densities. These were merged with the PXL hits in every simulated central Au+Au collision and used to obtain the results presented in Section 2.

Association Makers

The step of association comes directly after the embedding. Its basic functionality, which already exists in the STAR framework, is to correlate the MC input with the reconstructed output so one can calculate hit, track, decay-vertex etc finding efficiency. This is done either through the use of an embedded key (idtrue) in the hit structure or by 'proximity association' of reconstructed and MC clusters. The later one is less accurate and not suitable for our purposes. Currently the Association software generates a structure that contains enough correlated (matching) information to allow hit/track and partial decay-vertex evaluation. The current output is usable but not optimized for our purposes; one has to go through several steps in order to be able to perform a detailed evaluation. The current scheme will need to be modified or augmented to include vital information that will facilitate our work.

Analysis of Simulated Data

There are software modules needed exclusively during the evaluation of simulations, either full-event simulations or embedding. These are in general smaller, utility-type pieces of code. Most of these modules already exist in some form and it is a minor effort to adapt them to HFT.

4.6.5. Physics Analysis Framework

The physics analysis software is the most critical part in signal extraction. When it comes to physics analysis people use a diverse set of tools and methods to extract the physics signals, most of them developed by themselves. Most of the tools and infrastructure needed is either already in place or under development in current charm analyses. Here we will only indentify the broad areas of physics interests for the HFT mainly for the purposes of recording the institutional interests, responsibilities and commitments. These areas are: a) Charm-meson, b) Charm-baryon, c) B-meson reconstruction and d) possible spin-related signals. These are the areas discussed in the next Section.

4.6.6. Institutional Responsibilities

Institutional Commitments

The following discussion reflects and summarizes the software interests of the participating institutions at the time of writing of this CDR. Even though it is possible that institutional interests might get modified and shifted with time, it is expected that institutions with responsibility in key software areas (as discussed above) will provide the manpower needed to deliver their modules.

Resources Required

From a review of the required tasks one can categorize the required resources into two broad categories: a) effort contributed by the participating institutes and b) effort expected from collaboration resources. A first estimate is that HFT institutions should contribute at least the equivalent constant effort of three FTEs for the lifetime of the project (about a decade), and the collaboration the equivalent constant effort of about one FTE, mainly in infrastructure areas (simulations, tracking, databases etc). The collaboration areas of contribution appear under the BNL institution label in Table below.

Institutional Responsibilities and Commitments

After consultation with the institutional representatives, Table 21 summarizes their current interests and commitments to software tasks as outlined and discussed above. At this point only a broad categorization and grouping is attempted and not a detailed outline of commitments within a more general task. Details of implementation will be discussed and defined in the group's weekly meetings.

Software task		BNL	UCLA	KSU	NPI	MIT	LBL	Purdue	
Online									
	IST					X			?
	PXL						X	X	?
Offline									
Hit Reconst.	IST					X			
	Pixel						X	X	?
Tracking		X							?
Event Vertex		X		X	X				
Decay Vertex		X		X	X				
Calibration Db	IST					X			?
	PXL						X	X	
Alignment	IST	X		X		X			
	PXL	X		X			X	X	
Simulation									
Geometry	IST	X				X			
	PXL	X					X		
Fast/Slow Sim.	IST			X		X			
	PXL						X	X	
Embed./Pileup	IST			X		X			
	PXL						X	X	
Assoc/Analysis		X		X	X				
Physics Analysis									
Charm			X	X	X		X	X	
Bottom			X				X	X	
Λ_C				X	X		X		?
Spin							X		

Table 21: Summary of institutional responsibilities.

5. Management

The management of the HFT project is governed by the Project Execution Plan (PEP), that exists as a preliminary PEP at the time of CD-1 review. In this chapter essential parts of the PEP are reproduced. An important addition is a discussion of an alternate funding profile that would results in the HFT detector being securely in place ahead of RHIC Run-14, and thus enabling the proposed STAR heavy quark measurements earlier.

5.1. Management Organization and Responsibilities

5.1.1. Department of Energy

Within the DOE Office of Science (SC), the Office of Nuclear Physics (SC-26) has overall DOE responsibility for the HFT project.

Responsibilities

The Acquisition Executive for HFT is Jehanne Gillo, Director the Facilities and Project Management Division of the Office of Science for Nuclear Physics (SC-26). As such, he/she has full responsibility for project planning and execution, and for establishing broad policies and requirements for achieving project goals. Specific responsibilities for the HFT project include:

- Chairs the ESAAB Equivalent Board.
- Approves Critical Decisions and Level 1 baseline changes.
- Approves the Project Execution Plan.
- Delegates approval authority for Level 2 baseline changes to the Federal Project Director.
- Conducts Quarterly Project Reviews.
- Ensures independent project reviews are conducted.

The Office of Nuclear Physics (SC-26.2) is responsible for planning, constructing, and operating user facilities to provide special scientific and research capabilities to serve the needs of U.S. universities, industry, and private and Federal laboratories. Within NP, the Facilities and Project Management Division (SC-26.2) has direct responsibility for providing funding, and programmatic guidance to the HFT project. The HFT Program Manager, in SC-26.2, is the primary point of contact with the following responsibilities:

- Oversees development of project definition, scope and budget.
- Prepares, defends, and provides project budget with support from the field organizations.
- Reviews and provides recommendations to the AE on Level 1 baseline changes.
- Monitors Level 1 and 2 technical, cost, and schedule milestones.
- Participates in Quarterly Reviews, ESAAB Equivalent Board meetings, and project reviews.
- Ensures ES&H requirements are implemented by the project.
- Coordinates with other SC Staff offices, HQ program offices and the DOE Office of Engineering and Construction Management (OECM).

Helmut Marsiske is the Federal HFT Program Manager.

Nand Narain at the Brookhaven Site Office (BHSO) is assigned as the Federal Project Director. The Federal Project Director responsibilities include:

- Overall responsibility for planning, implementing, and completing HFT.
- Provides overall project management oversight.
- Issues key work authorization.
- Provides necessary funds via approved financial plans.
- Manages and allocates the contingency funds according to the procedure defined in the Baseline Change Control.
- Submits key project documents and critical decisions to DOE and reports project progress.
- Ensures that the project complies with applicable ES&H requirements (e.g., National Environmental Policy Act [NEPA] requirements).
- Approves Level 2 Baseline changes.

5.1.2. Brookhaven National Laboratory

Chairman for the Physics Department at BNL

Funding for this project will be directed through BNL's Physics Department. Fiscal and management responsibility for the fabrication of HFT will reside with the Chairman, Thomas Ludlam.

Responsibilities

The Chairman for the Physics Department at BNL shall be administratively and fiscally responsible for the entire project. In particular he must do the following:

- Provides overall management oversight for all aspects of the project.
- Appoints the Contractor Project Manager.
- Approves key personnel appointments made by the Contractor Project Manager.
- Approves major subcontracts recommended by the Contractor Project Manager.
- Ensures that adequate staff and resources are available to complete HFT in a timely and cost effective manner (within constraints of the budget provided by DOE).
- Ensures that HFT has demonstrated that it meets the functional requirements.
- Provides documentation and access to information necessary for operation of HFT at other sites.
- Ensures the work is performed safely and in compliance with the ISM rules.
- Reports to the Associate Laboratory Director for Nuclear and Particle Physics regarding the operations of the Physics Department.

5.1.3. BNL Contractor Project Manager

The Chairman for the Physics Department, Thomas Ludlam, has appointed Flemming Videbaek the HFT Contractor Project Manager.

Responsibilities

The Contractor Project Manager (CPM) shall report directly to the Chairman for the Physics Department and will be in charge of the overall management of HFT. The CPM shall appoint the key staff needed for the project with the approval of the Chairman for the Physics Department. The CPM also will have the following responsibilities:

- Responsible and accountable for the successful execution of contractor's project scope of HFT.
- Supports FPD in implementing DOE project management process.
- Delivers project deliverables as defined in this PEP.
- Identifies and ensures timely resolution of critical issues within contractor's control.
- Allocates the contingency funds according to the procedure defined in the Baseline Change Control (Section xxx)
- Responsible with DPM and subsystem managers for developing project documentation
- Keeps the STAR management informed on the progress of the project.
- Appoints the Quality Assurance Board (QAB).
- Appoints the Deputy Project Manager (DPM)
- Provides monthly input to the Federal Project Director to be used in report to DOE.
- Submits quarterly status reports to BHSO Federal Project Director.
- Ensures the work is performed safely and in compliance with the Integrated Safety Management (ISM) rules.
- Produces necessary Environment Safety and Health (ES&H) documentation with the HFT safety officer
- Approves baseline changes up to and including Level 3.

Flemming Videbaek has appointed Hans Georg Ritter as the Deputy Project Manager (DPM) The Deputy Project Manager works with, and reports directly to, the Contractor Project Manager. He functions as the CPM when the CPM is absent/unavailable and has the following responsibilities:

Responsibilities

- Maintains the same Project-specific signature authority as the CPM
- Represents the project in discussions with the collaboration concerning physics requirements and functionality requirements as may arise in the change control process.
- Responsible for simulations that establish and support functionality requirements and CD-4 acceptance criteria.
- Communicates the functional requirements and their relation to physics requirements to the Collaboration.
- Provides supervisory oversight in the preparation of the HFT CDR, TDR and other major HFT reports.
- Participates in the preparation of project quarterly reports to the DOE.
- Identifies and ensures timely resolution of critical issues within Deputy Contractor Project Manager's control.
- Identifies and collaborates with the Contractor Project Manager in mitigating project risks.
- Additional responsibilities as delegated by the Contractor Project Manager

5.1.4. Engineering Deputy

The CPM and the DPM have appointed Eric Anderssen as the Engineering Deputy.

Responsibilities

- . Responsible for the development of the HFT system design requirements, including interfaces between subsystems, and methods and practices for achieving these requirements.
- Controls changes in the HFT system design requirements, including interfaces between subsystems.
- Responsible for overall engineering safety of project design
- Identifies and ensures timely resolution of critical issues within Deputy Contractor Project Manager's control.
- Identifies project risks and collaborates with the Contractor Project Manager in mitigating project risks.
- Additional responsibilities as delegated by the Contractor Project Manager.

5.1.5. Subsystem Managers

The HFT Project contains three major systems: Pixel detector, IST detector, and SSD detector. In addition there are managers for Software and for Integration. The HFT Contractor Project Manager has appointed managers to be responsible for the subsystems, which comprise the major systems. They will be responsible for the design, construction, installation, and testing of their subsystem, in accordance with the performance requirements, schedule, and budget.

Responsibilities

- Assemble the staff and resources needed to complete the subsystem in collaboration with CPM and DPM
- Communicate the system design requirements to the staff.
- Ensure that subsystems meet the HFT system design requirements, including interfaces.
- Responsible for carrying out the design, construction and assembly of the subsystem in accordance with the scope, schedule and budget, assuming funding and resources as described in the PEP.
- Provide monthly reports on the status of the subsystem to the Contractor Project Manager.
- Responsible with the project and deputy project managers for providing documentation and presentations for reviews
- Develop and maintain the documentation of the subsystem (provide documentation to integrator)
- Ensure the work is performed safely and in compliance with the safety applicable to the respective institutions.

Table lists all subsystems and managers.

Subsystem	Subsystem Manager
PXL detector	Howard Wieman
IST detector	Bernd Surrow
SSD detector	Howard Matis
Global Structures and Integration	F.Videbaek (acting)
Software	Spiros Margetis

Table 22: HFT subsystems and managers.

5.1.6. Quality Assurance Board

The members of the board are the STAR Engineers Ciro d'Agostino, Robert Scheetz, Dana Beavis and Eric Anderssen.

Responsibilities

- Collaborates with the CPM and Deputy Contractor Project Manager to ensure the quality of HFT.
- Ensures that the quality system is established, implemented, and maintained in accordance with the HFT Quality Assurance Plan.
- Approve with subsystem managers QA procedures and testing for electronic and mechanical components.
- Provides oversight and support to the partner labs and institutions to ensure a consistent quality program.

5.1.7. Project Integrator(s)

The Project Integrators represents STAR and are responsible for coordinating data produced by the HFT team and confirming that the output from the various systems and scientists aligns with the STAR detector. While not responsible for creating the information, the Integrator maintains an overview of all scope requirements, including parameters, energy, power; footprints, quantities and planned locations of equipment; and is responsible for calling meetings as required whenever data from one area appears to be in conflict with expected outcomes and/or Project scope and direction.

Responsibilities

- Reviews all parameters
- Maintains HFT project files and documentation
- Provides electric and mechanical engineering oversight and participates in reviews as needed.

5.2. Integrated Project Team

The composition of the HFT Integrated Project Team (IPT) is given in Table 23. Its responsibilities are described in the DOE directive. The team meets at least quarterly, or more frequently if necessary. The DOE Federal Project Director chairs the IPT.

DOE Federal Project Director (Chair)	Nand Narain
DOE Site Contracting Officer	Evelyn Landini
DOE Program Manager for HFT	Helmut Marsiske
DOE Science Program Manager	Gulshan Rai
BNL Contractor Project Manager for HFT	Flemming Videbaek
LBNL Deputy Project Manager	Hans Georg Ritter
BNL ESSH Lead	Ed Lessard
Physics Assistant Chair for Administration	Robert Ernst
BHSO Facility Representative	Patrick Sullivan

Table 23: HFT Integrated Project Team

5.3. Participating Institutions

BNL will have overall responsibility for the fabrication of this MIE instrument. Institutional responsibility for the major subsystems comprising the HFT are: LBNL for the pixel detector; MIT for the strip detector; LBNL and BNL for the SSD upgrade, Kent State University for the software; and BNL for integration. These institutions have expertise and past experience in designing / fabricating / implementing similar subsystems. Memorandum of Understandings (MOU) will define the relationship between the institutions and BNL and will be in place for CD–2. The following is a list of all the participating institutions.

Brookhaven National Laboratory	BNL
Czech Technical University, Prague, Czech Republic	CTU
University of California, Los Angeles	UCLA
Kent State University, Kent	KSU
Nuclear Physics Institute ,Prague, Czech Republic	
Institut Pluridisciplinaire Hubert Curien, Strasbourg, France	IPHC
Laboratory for Nuclear Science, Massachusetts Institute of Technology, Cambridge	MIT
Lawrence Berkeley National Laboratory, Berkeley	LBNL
Purdue University, West Lafayette	PU
SUBATECH, Ecole de Mines, Nantes, France	SUB
University of Texas, Austin	UT

Table 24: Participating HFT institutions.

The sensor development is taking place at the Institut Pluridisciplinaire Hubert Curien (IPHC) in Strasbourg, France, where the LBNL group is working in close collaboration with Marc Winter and his group. The sensor development path for the PXL detector sensors is tailored to follow the development path of the technology as it was set by the IPHC group. This work and collaboration will be covered by an MOU that is expected to be signed by January 2010.

The electronics upgrade of the SSD is the responsibility of the STAR BNL group in collaboration with electric engineers from the SUBATECH group that will provide engineering for layout and initial testing of the new boards. This work and collaborations will be covered by an MOU that is expected to be signed by January 2010.

5.4. Cost and Schedule

The guiding principle for defining the schedule for the STAR HFT detector is to ensure that it is available as early as possible to provide crucial physics measurements for the heavy quark program at RHIC, and make measurements that will be important for the RHIC physics milestones, in particular DM12 "Measure production rates, high-pT spectra and correlations…"

The HFT has been organized into a Work Breakdown Structure (WBS) for purposes of planning, managing and reporting project activities. Work elements are defined to be consistent with discrete increments of project work. Project Management efforts are distributed throughout the project, including conceptual design and R&D. The HFT has 5 WBS Level 2 components:

WBS	Title
1.0	HFT Project
1.1	Project Management
1.2	Pixel Detector
1.3	Intermediate Silicon Tracker (IST)
1.4	Silicon Strip Detector (SSD)
1.5	Integration

A preliminary WBS dictionary is available as a separate project document for the CD-1 review.

The cost and schedule for the HFT project scope have been developed based on the following assumptions:

1. DOE Approval of CD-1 no later than January 2010
2. DOE Approval of CD-2/3 no later than November 2010
3. Receipt of DOE PED funding no later than January 2010
4. Receipt of DOE Construction funding no later than January 2011
5. The small radius thin-walled Be-beam pipe will be externally funded by RHIC
6. RHIC operations to be shutdown for 16 weeks in summer 2012, and for 20 weeks in summer/fall 2014 before Run- to allow time for installation/integration of HFT equipment.
7. The externally funded beam pipe has been certified and available for integration no later than October 2011 for installation of the IDS for Run-13.

5.5. Schedule

The HFT project has two phases: assembly of PXL ladders, mechanical insertion mechanism, and the mechanical integration with the small diameter beam pipe, and the STAR detector. This is required for the engineering run with either phase-1 or ultimate sensors. This is scheduled for Q1 FY13 in time for RHIC Run-13.

The second phase consists of assembly of final ladders for the PXL, and the IST and SSD detectors, and is scheduled for Q2FY14. The IST detector will have been fully tested on the bench ahead of this. This funding driven schedule does not allow the full system i.e. PXL, IST and SSD to be installed in the STAR detector, since this time of year is usually during a RHIC run. Under such normal running conditions the HFT will be fully installed in STAR for Run-15. The PXL detector, due to the rapid insertion mechanism, could be ready and inserted into beam during Run-14. The SSD detector upgrade schedule would allow that it could also be installed ahead of Run-14. The collaboration will revisit the schedule of the IST before CD-2 with the goal of a Q1FY14 installation.

The above schedule is predicated on the funding profile provided by DOE for new funds as addressed in the preliminary Project Execution Plan. This implies the following costs distributed over the WBS subsystems.

5.6. Milestones

Milestones will be used as schedule events to mark the due date for accomplishment of a specified effort or objective. A milestone may mark the start, an interim step, or the end of one or more activities as needed to provide insight into the Project's progress. Milestones are assigned to different levels (Table 25) depending on their importance and criticality to other milestones and the overall Project schedule.

Milestone Level	Description
0	Critical Decision milestones
1	Start and/or Completion of Major Project Phases
2	Milestones that support the accomplishment of the Level 0 and level 1 milestones
3	Milestones to monitor and assure progress

Table 25: HFT milestone level 0.

Table 26 shows the high level project performance milestones. Table 27 shows the Level 2 milestones. These, and all lower level milestones are maintained in the HFT Microsoft Project cost and schedule database.

Level 0	Date
CD-0	Q2 FY09
CD 1	Q2 FY10
CD 2	Q4 FY10
CD 3	Q4 FY10
CD 4	Q1 FY15

Table 26: High level project milestones.

HFT Preliminary Milestones		
1.2	Receive Prototype sensors from IPHC	Q3FY10
	Pixel Prototype Sector Design Complete	Q4FY10
	Prototype Insertion mechanism Testing Complete	Q2FY11
	Receive final Ultimate Sensors from ICH	Q1FY13
	Sector Assembly start	Q1FY13
	PXL detector available for insertion	Q2FY14
1.3	IST	
	Sensor, Module and Ladder design Complete	Q2FY10
	Prototype Modules tested	Q2FY11
	Sensors, Hybrid and ladders produced	Q3FY12
	Staves Finalized	Q1FY13
	Installed on MSC, ready for installation in STAR	Q1FY14
1.4	SSD	
	Prototype Board Layout Review	Q3FY10
	Prototype Test on bench	Q2FY11
	Final Design Complete	Q4FY11
	Move Full System to STAR for test	Q4FY12
	Ready for installation	Q3FY13
1.5	Beam pipe qualification	Q1FY11
	Beam pipe delivered and accepted at BNL	Q4FY11
	Inner detector Support assembled with FGT	Q1FY13
	Production OSC/MSC at BNL for integration	Q2FY13
	Inner detector Support assembled with SSD/IST/FGT	Q4FY14
1.6	Software	
	Calibration Model Developed	Q2FY10
	Tracker/Vertex finders functional	Q4FY11
	Reconstruction software finalized	Q3FY12
	IST online and calibration software commissioned	Q2FY13

Table 27: Level 2 milestones.

5.7. Cost scope

Table 28 shows the cost range for the project including contingency. Table 29 shows a breakdown of the cost in terms of funding years and source of funding.

This plan is consistent with what can be expected from DOE in a best-case scenario. This will allow for an early completion of the project in Q2FY14, but with the CD-4 dates on Q4FY14. This is not a preferable schedule from the point of meeting the physics goals of the RHIC-II era physics.

The HFT project has worked out a schedule that would require additional funding in FY11, either by increased DOE funding, or by having bridge funding by yet to be identified sources to increase the amount of available funding from 2.9M to approximately 4.0 in FY11. Should this come to pass the project can meet a Q1FY14 milestone for final assembly and readiness for installation in STAR.

WBS	Title	Cost	Contingency %	Contingency $	Low range	High Range
1.1	Project Management	1002	9%	90	1050	1120
1.2	Pixel	4574	35%	1620	5380	6760
1.3	Intermediate Silicon Tracker (IST)	2637	36%	960	3120	3930
1.4	Silicon Strip Detector (SSD)	660	44%	290	810	1050
1.5	Integration	1267	46%	580	1560	2050
	subtotal	10140	35%	3540	11920	14910
	Contributed Labor	2620		0	2620	2620
	Total Project Cost	12760		3540	14540	17530

Table 28: Total project cost range with contingency.

In terms of overall funding this requires the following plan

$M						
	FY 10	FY 11	FY 12	FY 13	FY 14	Total
R&D	0.2					0.2
PED/EDIA	1.8					1.8
Cons		3.4	6.0	5.5	0.9	15.8
Pre-Ops						0.0
TEC	1.8	3.4	6.0	5.5	0.9	17.6
TPC	2.0	3.4	6.0	5.5	0.9	17.8
Planned Redirects	0.6	0.5	0.6	0.7	0.2	2.6
New funds Required	1.4	2.9	5.4	4.8	0.7	15.2

Table 29: Project cost by fiscal year and by funding source.

5.7.1. Contingency

After the Project is baselined at CD-2 the FPD will manage the contingency funds according to the DOE Order 413.3A procedure defined in the Baseline Change Control section and as specified in the Change Control table in the preliminary Project Execution Plan.

At the present pre CD-1 phase (approved Alternate selection and Cost Range), traditional contingency percentages that varied from a low 25% for well-understood and well defined task to 50% for tasks with high associated risks were used. These contingencies percentages were based o expert judgment and were applied at the appropriate WBS level.

5.8. ES&H/ QA

The purpose of this section is to briefly describe the rigorous environmental protection, safety, security, health and quality (ESSH) activities associated with the HFT Project that will be completed prior to commencement of construction, installation and commissioning.

5.8.1. Integrated Safety Management

The Integrated Safety Management (ISM) policy for this project requires full commitment to safety by the project management team. Principles of ISM are incorporated into project planning and execution. The project follows the guidelines described in the LBNL Health and Safety Manual (PUB-3000) and Integrated Environment, Health and Safety Management Plan (PUB-3140) and the BNL Standards Based Management System (SBMS). All phases of the project at other locations will be carried out under those institutions' ES&H policies and procedures, and the HFT Project Manager will work collaboratively with those institutions to help ensure US researchers are working in an appropriately safe manner.

5.8.2. NEPA

Appropriate NEPA and State environmental reviews will be completed in advance of the CD-2 review. Existing Categorical Exclusions at BNL and LBNL are adequate to cover the Project. Work at LBNL will be covered for California Environmental Quality Act (CEQA) purposes under existing CEQA documentation. Work at BNL will be carried out under all federal, state and local regulations and requirements as documented in the SBMS.

5.8.3. ESSH Plans for Construction and Installation

The HFT upgrade for STAR will use the BNL Standards Based Management System (SBMS) to identify and control hazards for all equipment and work at BNL for the HFT. The Physics Department and the C-AD have review processes that comply with the BNL SBMS. The project will prepare designs and work procedures and have them reviewed by the appropriate laboratory or department review committees. Testing of equipment in Physics Department will go through the Experimental Safety Review (ESR) process (see http://www.phy.bnl.gov/~safety/ESRs/). The C-AD Experimental Safety Review Committee (ESRC) will review the equipment and work practices used at STAR. The reviews of the ESRC are covered in C-AD Operations procedures manual (OPM) chapter 9 section 2. The installation will be covered under the rules and safeguards in place for work in the RHIC experimental halls and assembly area. Refer to proper documents.

The risk analysis in the pHAD addresses the hazards of the HFT detector system. It also addresses hazards, controls and risks for experimental halls, experiments and their associated targets and detectors. The SAD follows the generally accepted principles identified in DOE Order 420.2B.

5.9. Project Quality Assurance Program

The project, through the Physics Department, shall adopt in its entirety the BNL Quality Assurance (QA) Program. This QA Program describes how the various BNL management system processes and functions provide a management approach which conforms to the basic requirements defined in DOE Order 414.1B, Quality Assurance.

The quality program embodies the concept of the "graded approach" i.e., the selection and application of appropriate technical and administrative controls to work activities, equipment and items commensurate with the associated environment, safety and health risks and programmatic impact. The graded approach does not allow internal or external requirements to be ignored or

waived, but does allow the degree of controls, verification, and documentation to be varied in meeting requirements based on environment, safety and health risks and programmatic issues. Prior to CD-2 the HFT project team will define a HFT QA-plan.

The BNL QA Program shall be implemented within the Project.

Quality Board Representatives have been assigned to serve as a focal point to assist management in implementing QA program requirements. The Quality Board has the authority to assist subsystem managers in identifying potential and actual problems that could degrade the quality of a process/item or work performance, recommend corrective actions, and verify implementation of approved solutions.

6. Acronyms

APS	Active Pixel Sensor
ARC	APV Readout Controller
ARM	APV Readout Module
CMOS	Complementary Metal Oxide Semiconductor
CDS	Correlated Double Sampling
DAQ	Data Acquisition
DDL	Detector Data Link (ALICE)
DRORC	Dual Readout Receiver Cards (ALICE)
FPGA	Field Programmable Gate Array
IDS	Inner Detector Support
IPHC	Institute Pluridisciplinaire Hubert Curien
IFC	Inner Field Cage
IST	Intermediate Silicon Tracker
JTAG	Joint Test Action Group
HFT	Heavy Flavor Tracker
LU	Latch Up
LVDS	Low-Voltage Differential Signaling
MAPS	Monolithic Active Pixel Sensor
MCS	Multiple Coulomb Scattering
MSC	Middle Support Cylinder
MTB	Mass Termination Board
OFC	Outer Field Cage
OSC	Outer Support Cylinder
PCB	Printed Circuit Board
PEP	Project Execution Plan
PXL	PiXeL Detector
QCD	Quantum Chromo Dynamics
SSD	Silicon Strip Detector
STAR	Solenoidal Tracker At RHIC
SVT	Silicon Vertex Tracker
TPC	Total project Cost
TPC	Time Projection Chamber

7. Appendix 1

7.1. Mechanical Design Simulation and Analysis

A number of mechanical design studies have been carried out to find designs that can meet the PXL requirements for stability and cooling. The work reported here has been carried out by either ARES Corporation or us. These analyses are not complete at this time, but they provide a starting point for prototype work, which can be expected to achieve the required performance.

7.1.1. Ladder Support Structural Analysis

The mechanical design of the PXL support system must meet stringent position stability requirements while also minimizing radiation length. The basic support design analyzed is pictured in Figure 33, but some analyses are also reported for alternative designs that have been considered.

The issues investigated are:

- Ladder backing stiffness required to hold the thinned silicon flat due to its tendency to curl
- Support strength to control gravity sag
- Support strength to control deformation from air flow pressure
- Control of thermal expansion induced deformation
- Control of moisture expansion induced deformation
- Support strength to handle insertion loads

Control of Silicon Curl

The PXL chips are mounted on flex cables with a composite backing and these ladders are mounted on a thin, large moment, carbon composite tubes shown as green in Figure 33. The tubes are the primary source of support and the ladder backers provide support for handling plus these backers must also provide support for the 1 cm overhang of the ladders. In the overhang region the backer provides the only mean for holding the thinned silicon chips flat. Without backing, the silicon chips tend to curl as a result of the stresses imposed in the silicon during chip fabrication. A simple analysis shows that a 2 mil thick carbon composite will allow the silicon to curve out of plain by 700 microns. A thicker but less dense backer of perhaps open weave carbon composite that is 10 mils thick will limit the deformation to 30 microns while maintaining a 0.02% X_0 budget for the backer, namely the equivalent of 2 mils carbon composite. This deformation is outside of the 20 microns envelope, but the deformation will be mapped and the stability should satisfy the 20 micron specification.

Control of Gravity Sag

The most critical component for controlling deformation from a variety of sources is the sector tube shown in Figure 33. This structure is in the tracking path and thus requires the most attention to radiation thickness. Analysis of the sector tube control of gravity sag has been carried out by us and by the ARES corporation. The ARES analyses, included details of the composite weave, and showed that a sector tube could be fabricated with a thickness of 120 microns and more than satisfy our 20 micron stability requirement giving a gravitational displacement of less

than 6 microns. We have performed a similar analysis, but with an isotropic modulus representation of the composite. This work shows a 5 micron deformation for the detector elements and 35 microns for other parts of the structure, but with the addition of an end lip. The analysis gives a gravitational detector displacement limited to 0.6 microns and the maximum displacement of the structure is 4 microns (see Figure 82). These results show that gravity induced distortions are not a problem with this design. As will be shown, other contributions to deformation are more significant.

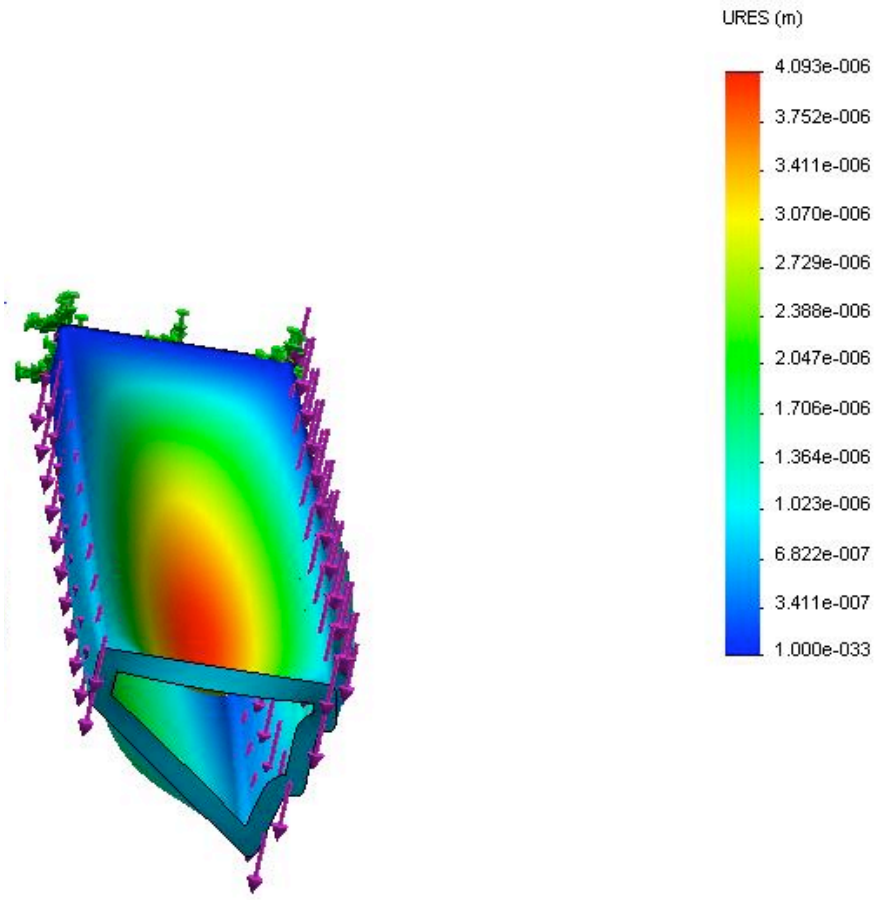


Figure 82: FEA results for gravity deformation of a 120 micron carbon composite support structure carrying 4 detector ladders.

Control of Airflow Induced Deformation

The deformation and vibration induced on the detector support from the cooling air flow requires more study, but preliminary considerations indicate that the current structure may be adequate. The planned cooling air velocity, 8 m/s, has a dynamic pressure that, when acting on the area of the structure, is 1.7 times the gravitational force. From the gravity analysis we conclude that the static deformation will be less than 2 microns. Again, vibration studies with prototype structures and possibly computational fluid dynamics (CDF) simulations will be done.

Control of Thermal Expansion Induced Deformation

One of the greatest potential sources of deformation is differential expansion resulting from changes in temperature between powered on and power off states. It is planned to spatially

calibrate or map the detector structures in a vision coordinate machine with the power off and the structure should not deviate from the map by more than 20 microns while powered on during operation. This requirement was one of the main reasons for choosing the current design with its large moment of inertia and consequently large stiffness. The ladder and beam structure being examined is illustrated in Figure 32 and Figure 33. It was found that the main issue requiring control is the bimetal thermostat effect from differential expansion of the two sides of the ladder. The problem is the result of the very large coefficient of thermal expansion (CTE) of the Kapton cable compared to the rest of the structure. An analysis of a short section of the ladder shown in Figure 83 illustrates the problem where in this case the thermally induced displacement is 500 microns at the edge of the silicon.

A thermal expansion analysis of ladders plus support shows that by using a very compliant adhesive (3M 200MP) the Kapton cable is largely decoupled from the structure greatly reducing the thermal induced bending. Simulation results shown in Figure 84 give a maximum deformation of 9 microns, well inside of the 20 micron requirement envelope.

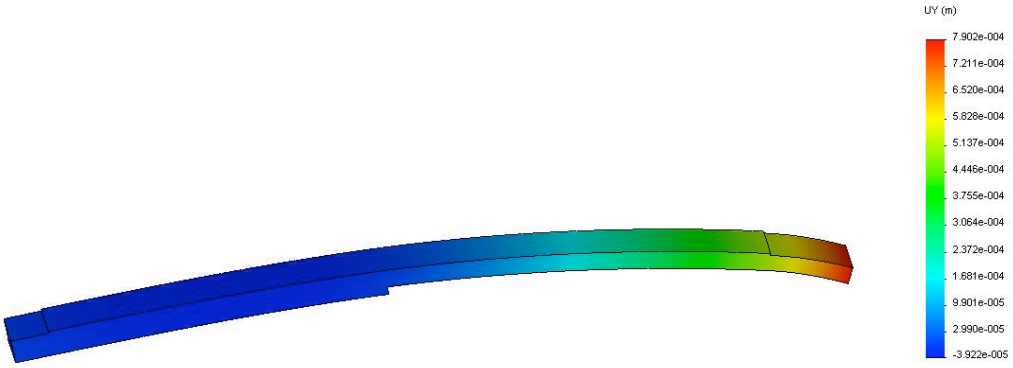


Figure 83: Short section of ladder structure showing problems with excessive thermal bimetal effect bending with using stiff adhesive. The 500 micron displacement resulting from a 20 deg C temperature change is driven by the large CTE of the Kapton cable.

Control of Moisture Expansion Induced Deformation

The carbon composites expand with increased moisture content. There will be a long term reduction in the moisture content from the time of manufacture until completion of operation in the experiment environment which can potentially lead to unacceptable geometry changes. The ARES Corporation has studied this problem for us and has found a composite layup configuration that meets our 20 micron requirement. This work appears on p. 99 and 102 of their summary report. They recommend a laminate: YSH-50/EX-1515 with a layup: [0, +60, -60]. The FEA analysis gives a maximum displacement of 16 microns. Further analysis and prototyping is required to address this issue. The inclusion of a soft decoupling adhesive may help as it appears to help in the thermal case.

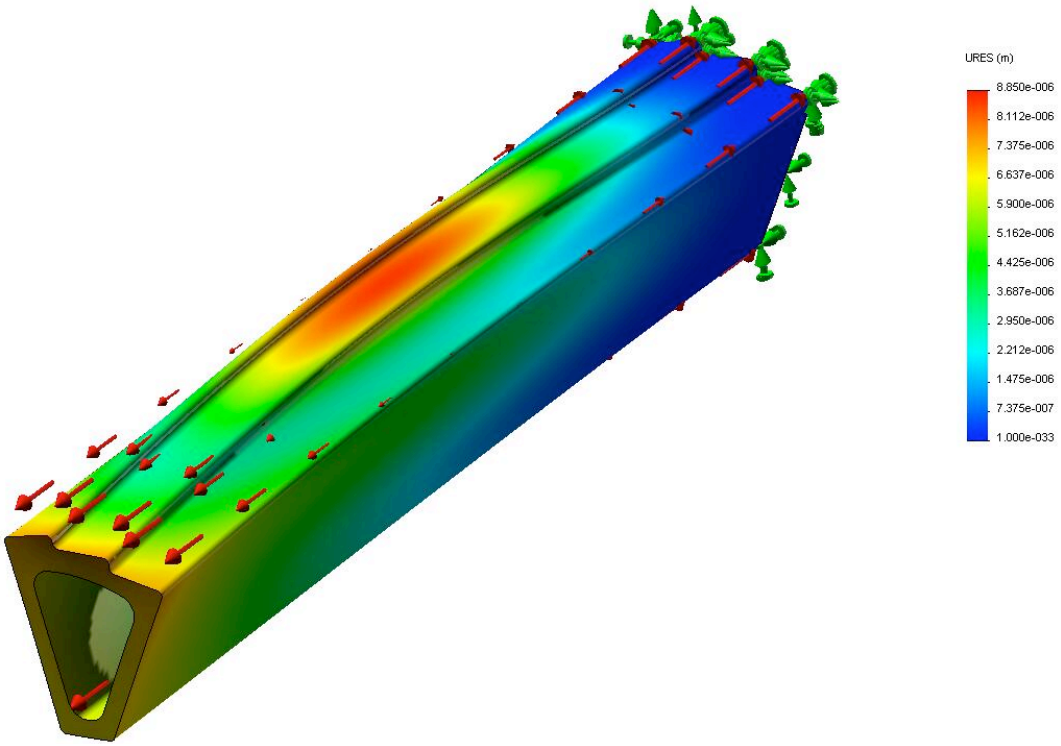


Figure 84: Thermally induced displacement of a sector beam with end reinforcement. The maximum resulting displacement is 9 µm. The beam and end reinforcement is composed of 200 µm carbon composite.

Support Strength to Handle Insertion Loads

When the detector is inserted into the final docking position in the center of STAR it engages spring-loaded over-center-latches into the kinematic mounts. The insertion supports have much less stringent stability requirements than the detector ladders since the positioning only has to be good enough to lie inside the kinematic mount engagement window which is ~1 mm, but the support must be able to handle the cocking load of the latches which is on the order of 15 lbs. Displacements must also be limited such that the two half detector cylinders do not collide during the insertion process. A FEA analysis of the supporting hinge structure has been done to check that it is adequate for cocking loads. The results of this analysis, shown in Figure 85, indicate that the design can safely handle the load without undue distortion. The analysis was not done on the latest complete hinge design, but an analysis of one part (see Figure 86) of the latest design shows that it is more than adequate.

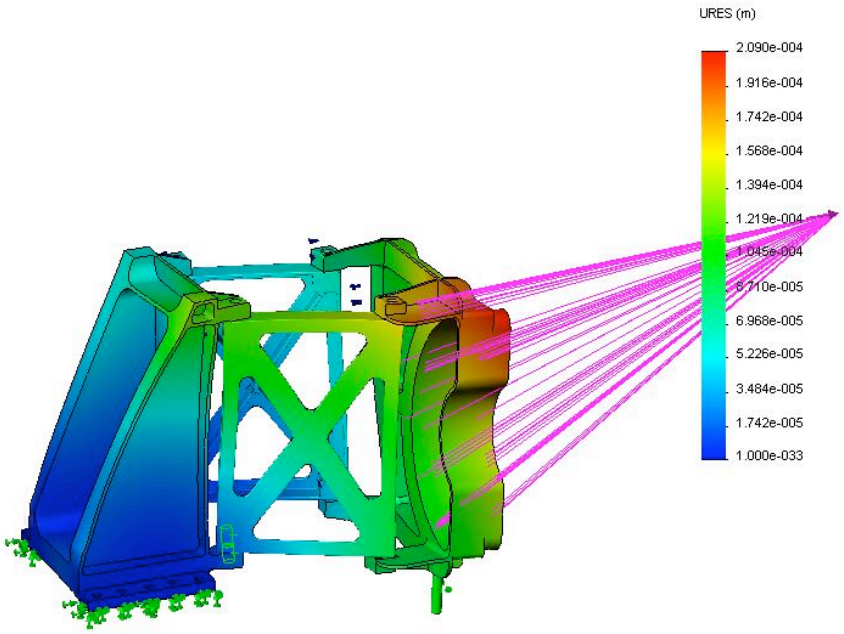


Figure 85: Displacement of an early insertion hinge design under cocking load of the latching mechanism. The displacement in the image is magnified by 140 and the maximum displacement is 210 microns. The pink lines show the position of the remote load as it is carried through the D tube, not shown.

Vibration of STAR Central Support

In STAR the central inner detectors such as the PXL detector are supported through the OSC and the ISC to TPC end caps. An accelerometer was mounted on the TPC end cap to measure possible vibrations that might couple to the PXL detector and affect position stability. A result from this measurement study (Figure 87) shows the response of a harmonic oscillator as a function of its resonant frequency to vibration if mounted directly on the end cap. This data can be used to set limits on the expected vibration of various components and determine whether the performance of the detector is compromised. There are several components of the detector system which each have their own requirements with respect to stability and vibration.

Consider first the vibration of one PXL sector ladder support with respect to the other. This case affects directly the pointing accuracy of multiple tracks to a vertex and therefore the full resolution is required and the vibration should stay below the 9 micron RMS requirement. The fundamental frequency for the sector can be obtained from FEA analysis which gave a 6 micron movement under gravity load. The fundamental frequency is

$$f = \frac{1}{2\cdot\pi}\cdot\sqrt{\frac{g}{d}}$$

or 200 Hz for the 6 micron sag under gravity. From Figure 87 this gives an RMS vibration of 0.04 microns, which is completely negligible compared to our 9 micron requirement. This vibration from this source will actually be significantly less than this because the sector is not directly coupled to the TPC wheel. The less stiff OFC and IFC provide the connection reducing the high frequency coupling.

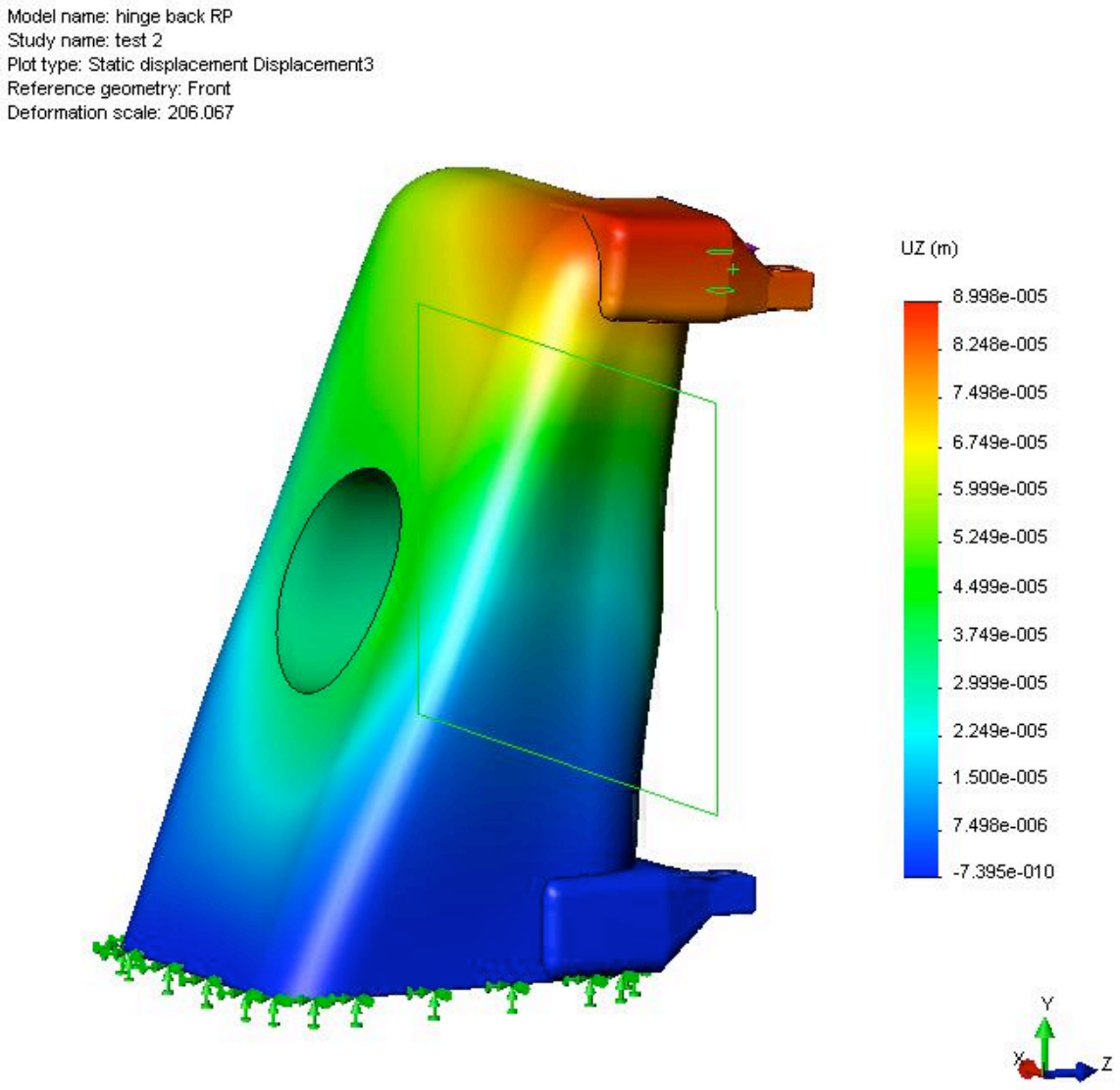


Figure 86: Distortion of the support hinge backer under latch cocking load. The flexing in the beam axis direction is 90 microns.

The next element to consider is the PXL half cylinder as a whole. The stability of this element is most important for track matching from the IST, so the stability of this element should be good enough that it does not compromise the IST pointing resolution, namely it should be less than 100 microns RMS. It is preferable though to be within the PXL limit since there are overlapping pixels between the two half cylinders. The ARES analysis p. 144 gives a fundamental frequency of 110 Hz for the PXL half cylinder when supported on the kinematic mounts. This, according to Figure 87, gives a RMS vibration of 0.2 microns, which again is insignificant.

Finally the vibration of the OFC can be checked. The stability of this element only has to be good enough to not compromise the TPC tracking precision which is ~ 1 mm. It is expected that the OFC will be built with gravity sag of 1 mm or better which was the number for the old support cones that are being replaced by the OFC. The fundamental frequency for this displacement is 16 Hz which according to Figure 87 gives ~ 4 microns RMS vibration. Again, this is not an issue compared to the 1 mm requirement.

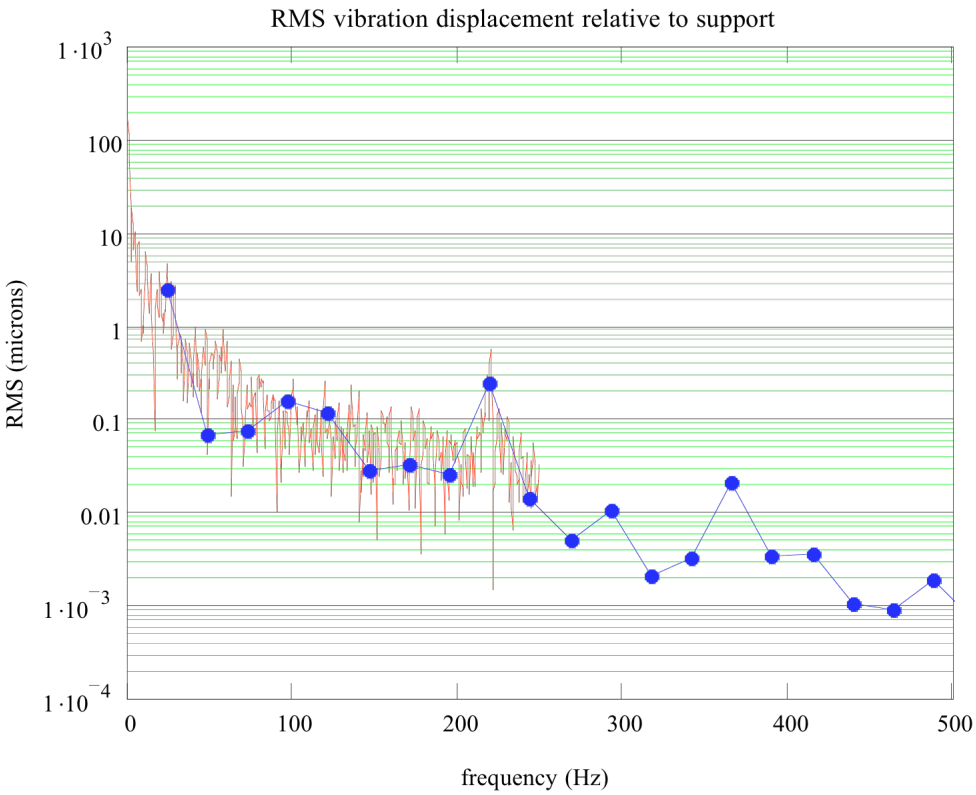


Figure 87: Vibration response of a mechanical harmonic oscillator mounted on the TPC end cap as determined with measurements of an accelerometer bolted to the TPC end cap. The two curves represent measurements made using two different methods of recording the data.

7.1.2. Ladder Cooling Analysis

Air cooling has been chosen for the PXL detector in order to minimize multiple coulomb scattering and a number of studies have been carried out to optimize the air cooling design. Original tests with a heated ladder in a fan driven air stream indicated that ladders with heat loads of 100 mW/cm^2 could be successfully cooled with a moderate air velocity. A study by ARES Corporation, p. 73 found that an airflow velocity of 8 m/s through the sector beam was sufficient to limit the silicon temperature rise above ambient to 13 deg C. To accomplish this however additional cooling fins required under the outer layer of silicon, which adds mass and complicates construction.

Bi-directional Air Flow Cooling

Since then more extensive, but still preliminary, CDF modeling has been done with air flow over both the inner and outer surfaces of the sector structure. The cooling simulation was run for one sector out of the 10 sectors in the complete PXL cylinder. The air flow path is shown in Figure 39 and Figure 88 and the silicon surface temperature profile is shown in Figure 89.

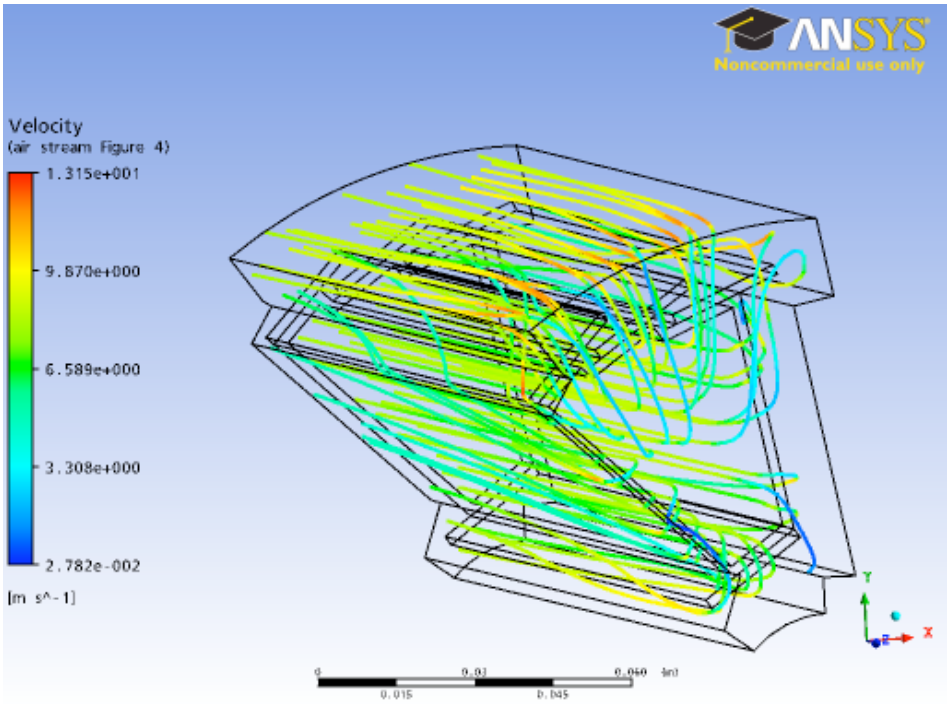


Figure 88: Stream lines showing the cooling air flow. The flow direction is from inside to outside. The color code shows air velocity.

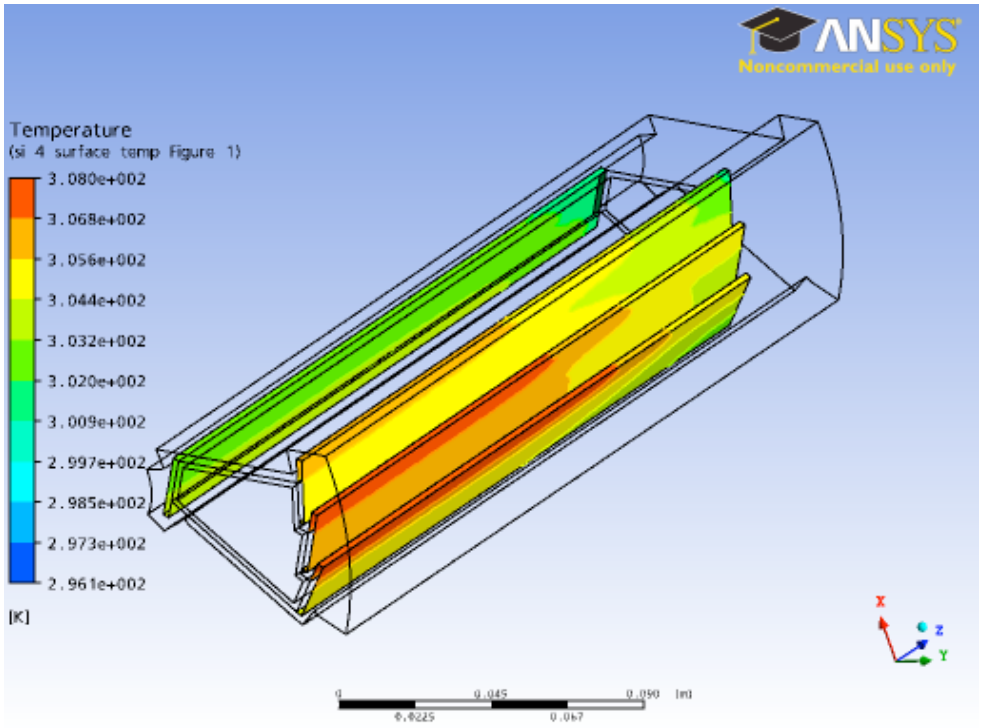


Figure 89: Surface temperature of silicon ladders. The maximum temperature increase above ambient is 12 deg C. The cooling air flows across both the inner and outer surfaces. The air enters from the left on the inside of the support beam, turns around at the right and exits on the left.

In this case an input air velocity of 8 m/s was used. This results in a maximum silicon temperature rise above ambient of 12 deg C, which is acceptable. It is interesting to note that the inside ladders next to the beam pipe cool more effectively than the outside ladders. This is because the surface area of the support beam sides provides a significant fraction of the cooling.

The total air flow in this case for the full PXL detector barrel is ~280 CFPM and the temperature rise in the air for the total power of the ladders, 240 W, is 1.5 deg. C. This is a very small rise in the air temperature, so alternatives can be considered with reduced total air flow which would result in a smaller air cooling system.

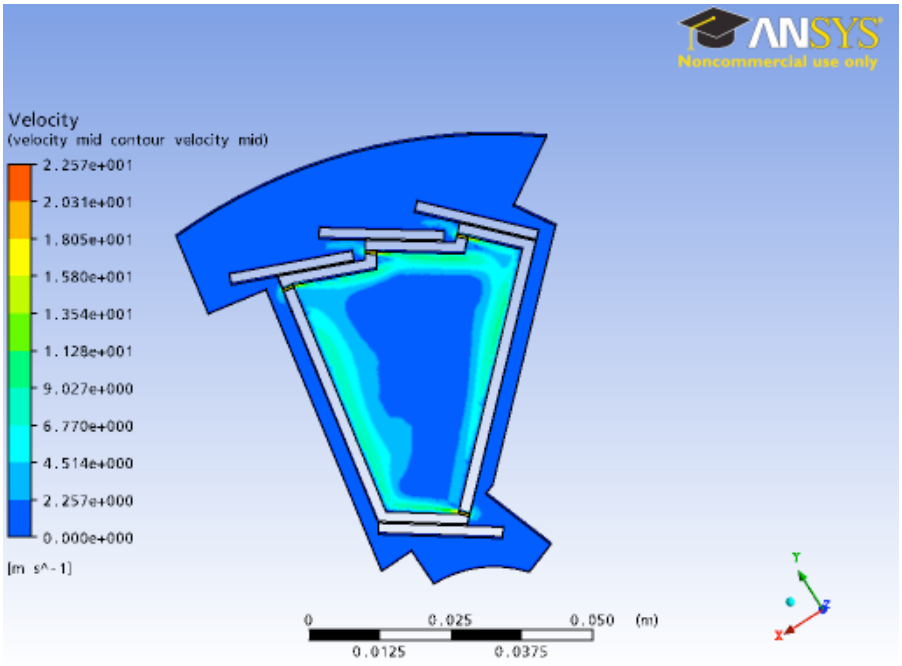


Figure 90: Sector cooling with transverse jets of cooling directed to the inside of the sector beam support structure through thin slots. The air velocity profile is shown in color. The air velocity near the surfaces beneath the ladders is 11 m/s.

Alternative Air Flow Design

An alternative design has been investigated with reduced total air flow volume and an increased air velocity at the surface to improve the heat transfer. In this design the high velocity air flow is in the transverse direction local to the ladder surface (see Figure 90). The air flows through narrow slits in the ladder support beam from outside into the sector beam.

The calculated surface temperature as shown in Figure 91 gives a maximum silicon temperature above ambient of 14 deg C. This is not quite as good as the performance with the simpler longitudinal bi directional cooling design with air flow over both inside and outside surface. For this reason future development will focus on the simpler longitudinal flow design.

Air Flow Induced Vibration

A mechanical finite analysis of the sector structure shows that there are multiple vibration modes close in frequency that can potentially be excited by the cooling air flow. Two design examples are shown in Figure 92 and Figure 93 in one case with a simple open end and another with a

reinforced end. The reinforced end increases the resonant frequency making this the desirable choice.

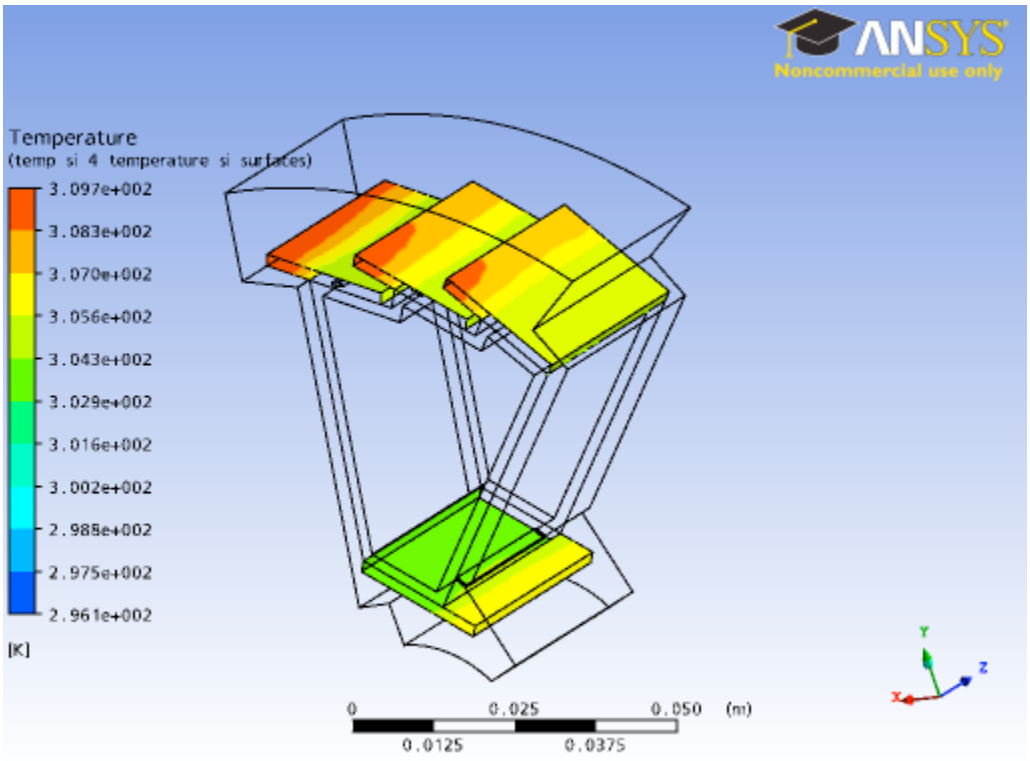


Figure 91: Silicon surface temperature profile for the transverse cooling jet design.

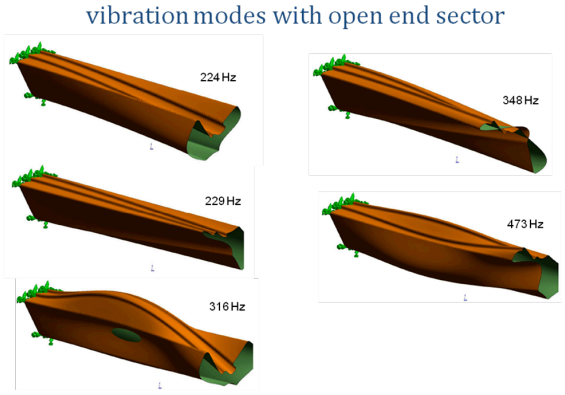


Figure 92: First vibration modes for an open ended sector. Frequencies are relative as composites properties in the FEA are not as-built.

A single sector sized wind tunnel was built and used to measure the vibration of the sector structure when subjected to cooling air flow. The test structure, shown in Figure 94 is equipped with a sensitive capacitive probe to measure vibration, an air velocity probe and a vacuum cleaner to provide air flow.

Figure 95 shows the measured rms amplitude of vibration of the middle outside ladder at the end of the unreinforced sector as a function of the air velocity. This measurement was made with the

probes positioned as shown in Figure 94. The vibration amplitude is at the limit of the acceptable range. Additional measurements on both the open sector and the reinforced sector were made at multiple points as shown in Figure 96 with the desired air velocity required for cooling. For comparison, the first FEA vibration mode shapes are shown, but amplitudes are not calculated. The numbers shown in the figure are the measured RMS amplitudes which are well within our requirement limits.

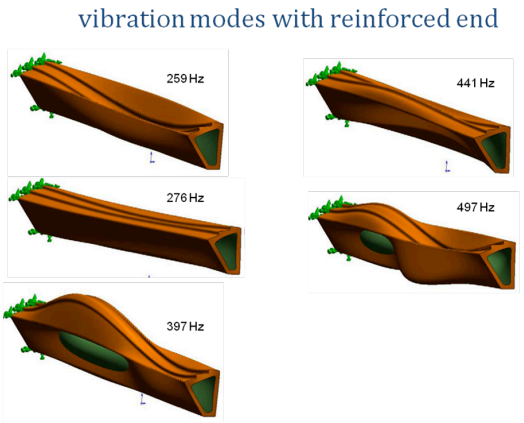


Figure 93: First vibration modes for a sector with a reinforced end. Frequencies are relative as composite properties in the FEA are not as-built.

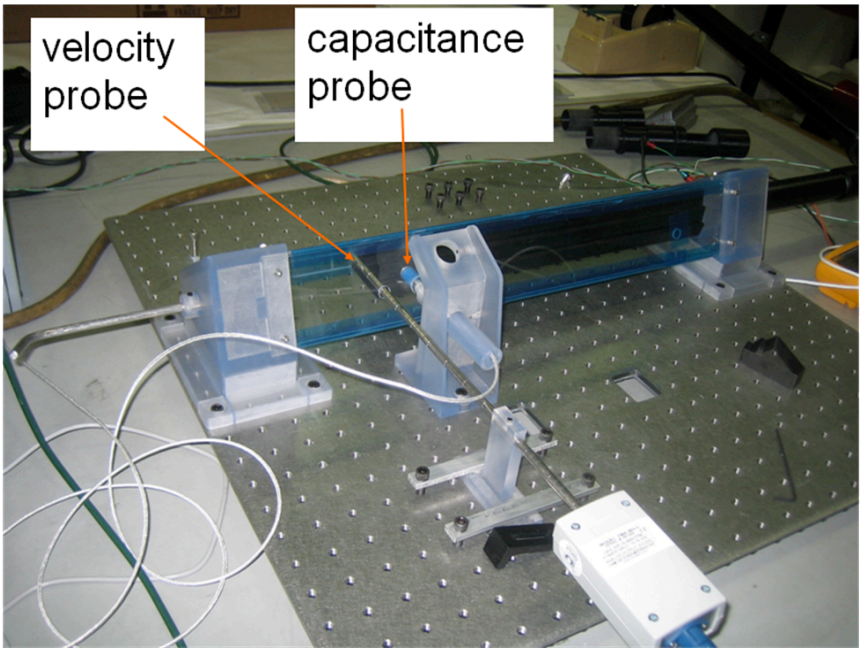


Figure 94: Wind tunnel to measure vibration of the sector structure induced by cooling air flow. The carbon composite sector under test weighs 21 gm. Additional weight was attached to include the effect of installed ladders.

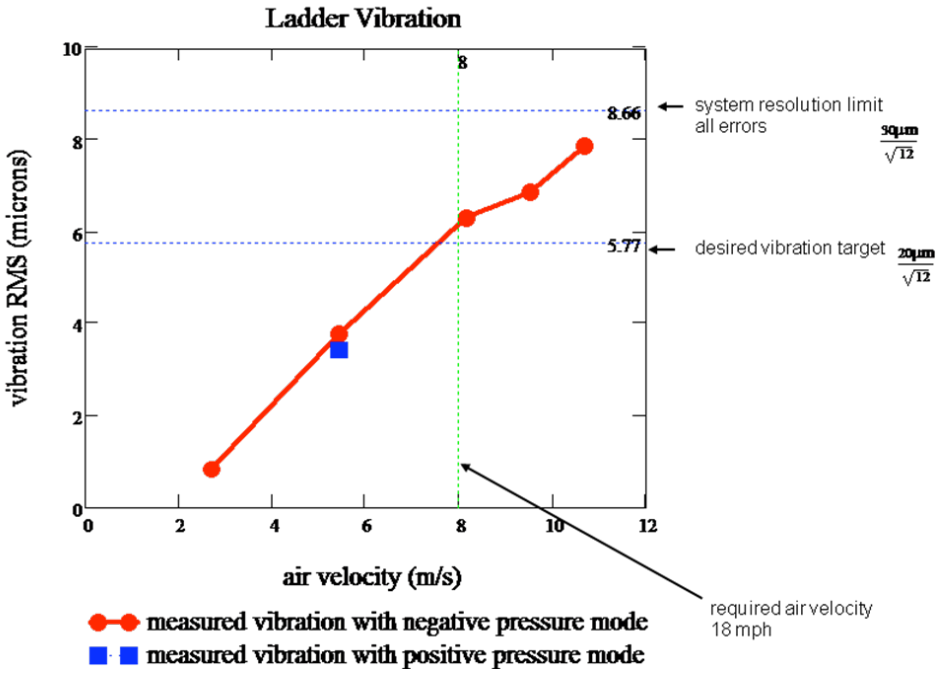


Figure 95: Measured rms vibration of the middle outside ladder position at the point of maximum vibration. The sector in this case was open ended, without reinforcement.

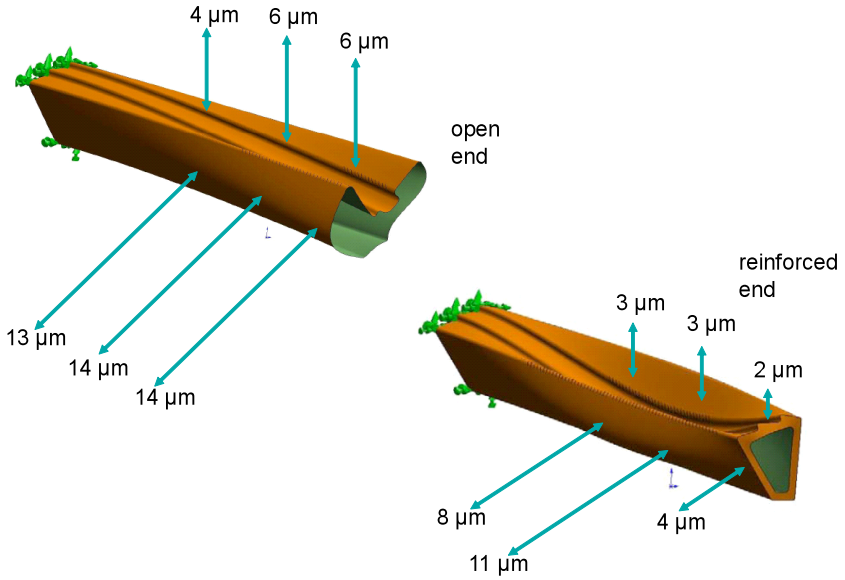


Figure 96: Measured vibration at several points on two sector designs, one with an open end and another with a reinforced end. The first vibration modes from FEA are shown for qualitative comparison. The top position measurements give the ladder vibration which is of interest because this affects the detector performance. The 3 µm value is well within our 20 µm requirement. The side vibration does not affect detector positions.

8. Appendix 2

8.1. Description of the PXL RDO System

This document is an extension of the PXL RDO discussion in the HFT proposal. It is intended to give detailed parameters for the function of the PXL readout system that will allow for an understanding of the logic and memory and requirements and the functionality of the readout system. We will present the designs of the Phase-1 and Ultimate readout systems under periodic triggering conditions. The simulation of the system response to random triggering of the type expected to be seen at the STAR experiment is ongoing and will be available in the future. The readout design is highly parallel and one of the ten parallel readout systems is analyzed for each system.

8.1.1. Phase-1 Readout Chain

The Phase-1 detector will consist of two carrier assemblies, each containing four ladders with ten sensors per ladder. The readout is via identical, but parallel, chains of readout electronics. The relevant parameters from the RDO addendum are reproduced in Table 30.

Item	**Number**
Bits/address	20
Integration time	640 μs
Hits / frame on Inner sensors (r=2.5 cm)	295
Hits / frame on Outer sensors (r=8.0 cm)	29
Phase-1 sensors (Inner ladders)	100
Phase-1 sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5

Table 30: Parameters for the Phase-1 based detector system used in the example calculations shown below.

The functional schematic of the system under discussion is presented in Figure 97.

We will show how the system functions for two cases. The first is for a periodic trigger rate of 1 kHz. The second is for a periodic trigger rate of 2 kHz. These cases make the scaling clear. In both cases we will use the average (pile-up included) event size. We are currently simulating the dynamic response of the system to the triggering and event size fluctuations seen at STAR and will make this information available after the simulations are completed. It is important to note that the system is FPGA based and can be easily reconfigured to maximize the performance by the adjustment of buffer sizes, memory allocations, and most other parameters. The relevant parameters of the system pictured above are described below.

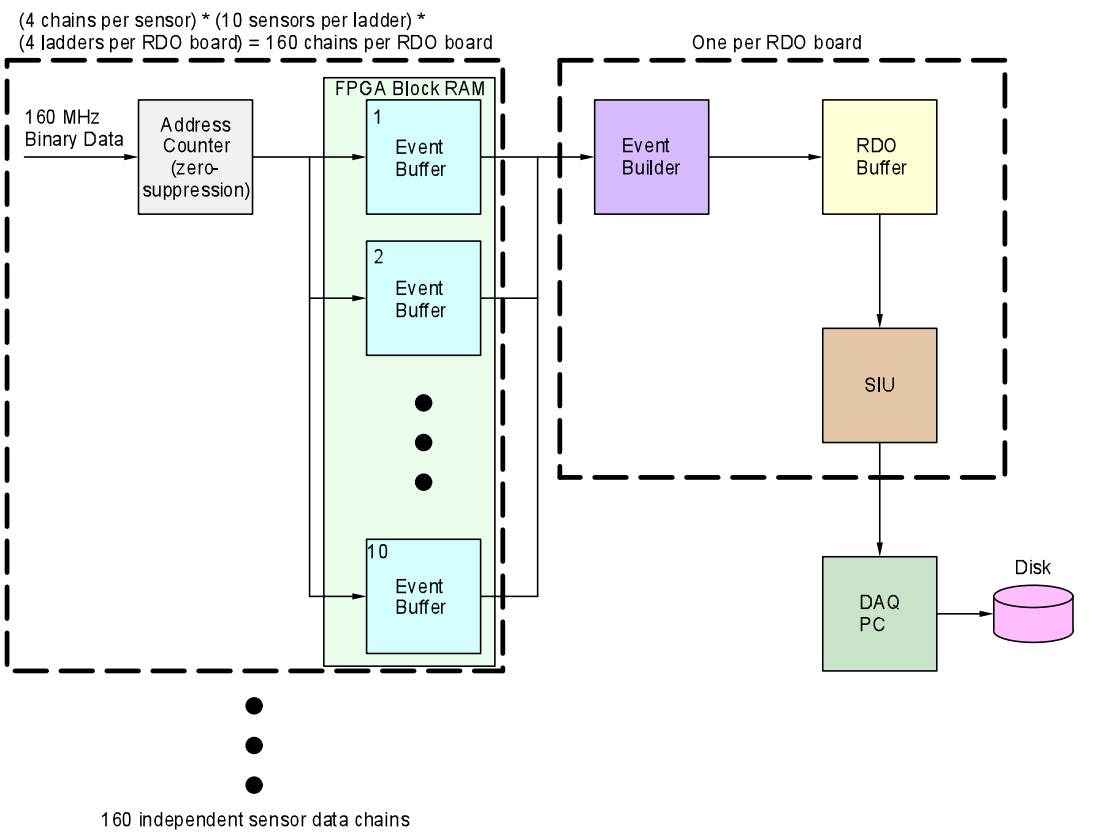


Figure 97: Functional schematic diagram for one Phase-1 sensor based RDO board. Each RDO board services one inner ladder and 3 outer ladders. Each ladder contains 10 sensors.

Data transfer into event buffers – The binary hit data is presented to the address counter at 160 MHz. The corresponding hit address data from the address counter is read synchronously into the event buffers for one full frame of a 640 × 640 sensor at 160 MHz. This corresponds to an event buffer enable time of 640 μs.

Event Buffers – Each sensor output is connected to a block of memory in the FPGA which serves as the storage for the event buffers. Each block of memory is configured as dual ported RAM. The overall FPGA block RAM used per sensor output is sized to allow for storage of up to ten average events with event size fluctuation. This leads to a total buffer size that is 20 × the size required for the average sized event (different for inner and outer sensors). The FPGA block RAM will be configured with pointer based memory management to allow for efficient utilization of the RAM resources. The average inner sensor has 295 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (295 hits) × (20 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 7,375 bits**.** Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each inner sensor output is 73,750 bits or 3,688 20-bit addresses**.

For outer sensors, the event buffer size is calculated similarly. The average outer sensor has 29 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (29 hits) × (20 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 725 bits**.** Multiplying this event buffer size by 10 gives the size of the RAM required

for the full set of event buffers required. **The event buffer block RAM size for each outer sensor output is 7250 bits or 363 20-bit addresses**.

Data transfer into the RDO buffer via the event builder – This process is internal to the FPGA, does not require computational resources, and can run at high speed. In the interests of simplicity, we will assume a 160 MHz clock to move data in 20-bit wide address words. The event builder first adds a 128 Byte header that contains the trigger ID and other identifying information into the RDO buffer, and then moves the address data from the event buffers into the RDO buffer in 20-bit words. The average carrier event size is [(29 hits / sensor (outer)) × (10 sensors) × (3 ladders) + (295 hits / sensor (inner)) × (10 sensors) × (1 ladders)] × (2.5 hits / cluster) = **9550 address words (20-bit)**. The RDO buffer is 5 × the size required for an average event and is thus **955 kb** in size. The full time required to transfer the address data into the RDO buffer (in 20-bit per clock transfers) is then **59.7 μs**.

Data transfer from the RDO buffer over the DDL link – The RDO buffer is dual-ported and thus readout from the SIU to the RORC can proceed as soon as the RDO buffer begins filling. The data transfer rates for the SIU–RORC combination as a function of fragment size are shown in Figure 98.

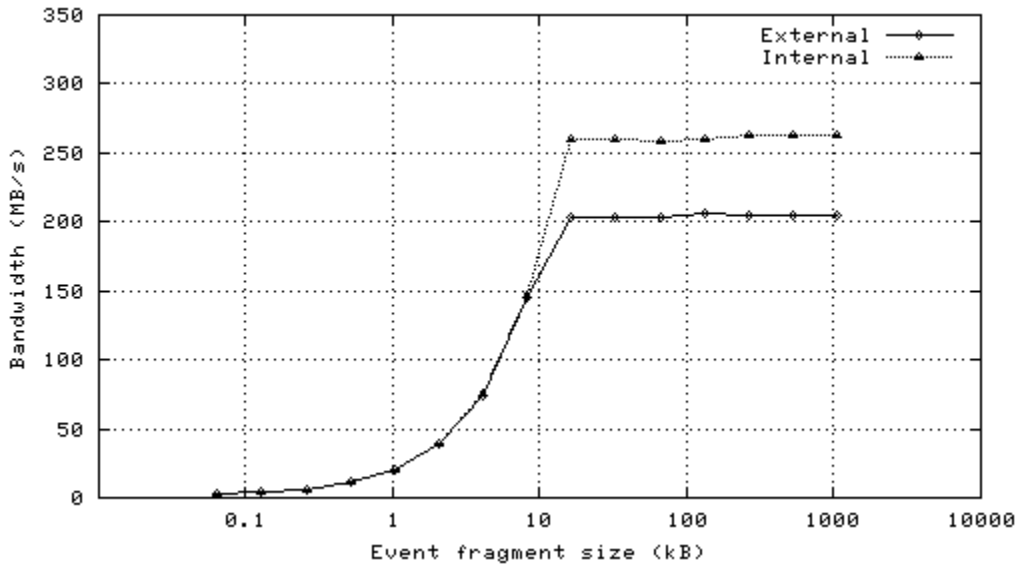


Figure 98: Bandwidth of a single channel of the SIU - RORC fiber optic link as a function of event fragment size with an internal and external (DDL) data source using two D-RORC channels. Figure taken from the LECC 2004 Workshop in Boston.

In this case, we will assume that we are padding the 20-bit address data to 32-bit word lengths for transfer on the DDL link. The event size is then (32 bits) × (9550 address words) **= 305.6 kb or 38.2 kB.** In this example, our transfer rate is ~ 200 MB / s. This transfer then takes **191 μs.**

Data transfer to the STAR DAQ for event building – The event data is buffered in the DAQ PC RAM (> 4GB) until (and only) the accepted events are written to disk and then transferred via Ethernet to an event building node of the DAQ system. Level 2 trigger accepts are delivered to the RDO system and transferred via the SIU–RORC to the DAQ receiver PCs. Only the events that have been accepted by level 2 are then built into an event. In this way, the buffer provided by the DAQ PC RAM provides for the elasticity needed for an average event acceptance of 1 kHz

The results of these calculations and discussion are presented below in the chronograms in Figure 99 and Figure 100.

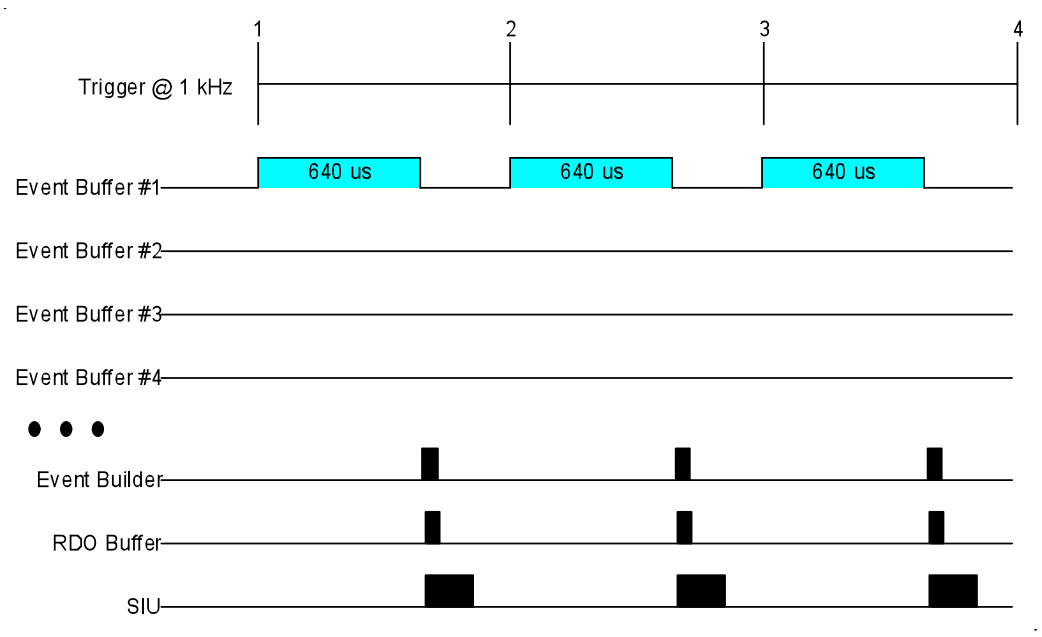


Figure 99: Chronogram of the Phase-1 based readout system functions for a 1 kHz periodic trigger.

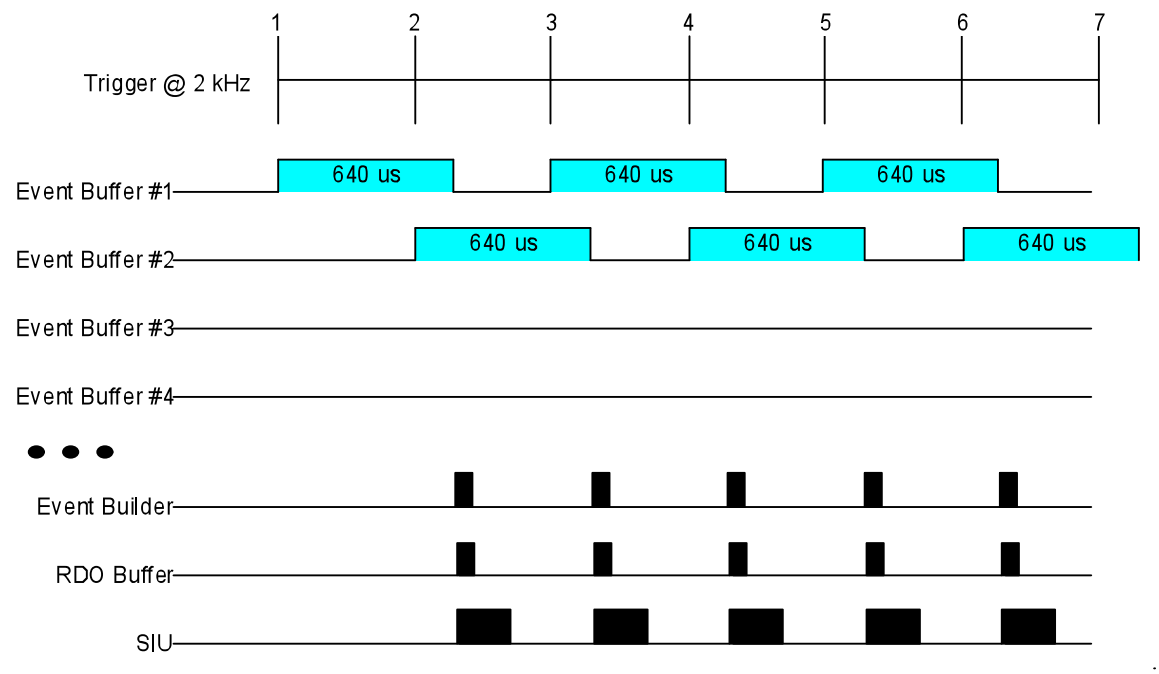


Figure 100: Chronogram of the Phase-1 based readout system functions for a 2 kHz periodic trigger.

The memory resources required in the FPGA / motherboard combination for this readout design are (120 outer sensor readout buffers) × (7.25 kb per event buffer) + (262.5 kb for the RDO buffer) + (40 inner sensor readout buffers) × (73.75 kb per event buffer) + (955 kb for the RDO

buffer) = **4775 kb**. The Xilinx Virtex-5 FPGA used in our design contains 4.6 – 10.4 Mb of block RAM so the entire design should fit easily into the FPGA.

Ultimate Sensor Detector Readout Chain

The Ultimate sensor readout system consists of ten parallel readout chains, as before. The main difference between the Phase-1 sensors and the Ultimate sensors is the inclusion of zero suppression circuitry in the Ultimate sensor, thus only addresses are read out into the RDO boards. In addition, the integration time of the Ultimate sensor is 200 μs and there are two data outputs per sensor. These differences lead to the functional schematic of the readout system shown in Figure 101.

We will show how the system functions for the same two cases as shown for the Phase-1 readout system. The first is for a periodic trigger rate of 1 kHz. The second is for a periodic data rate of 2 kHz. Again, in both cases we will use the average (pile-up included) event size. The relevant parameters of the Ultimate sensor based system pictured above are described in Table 31.

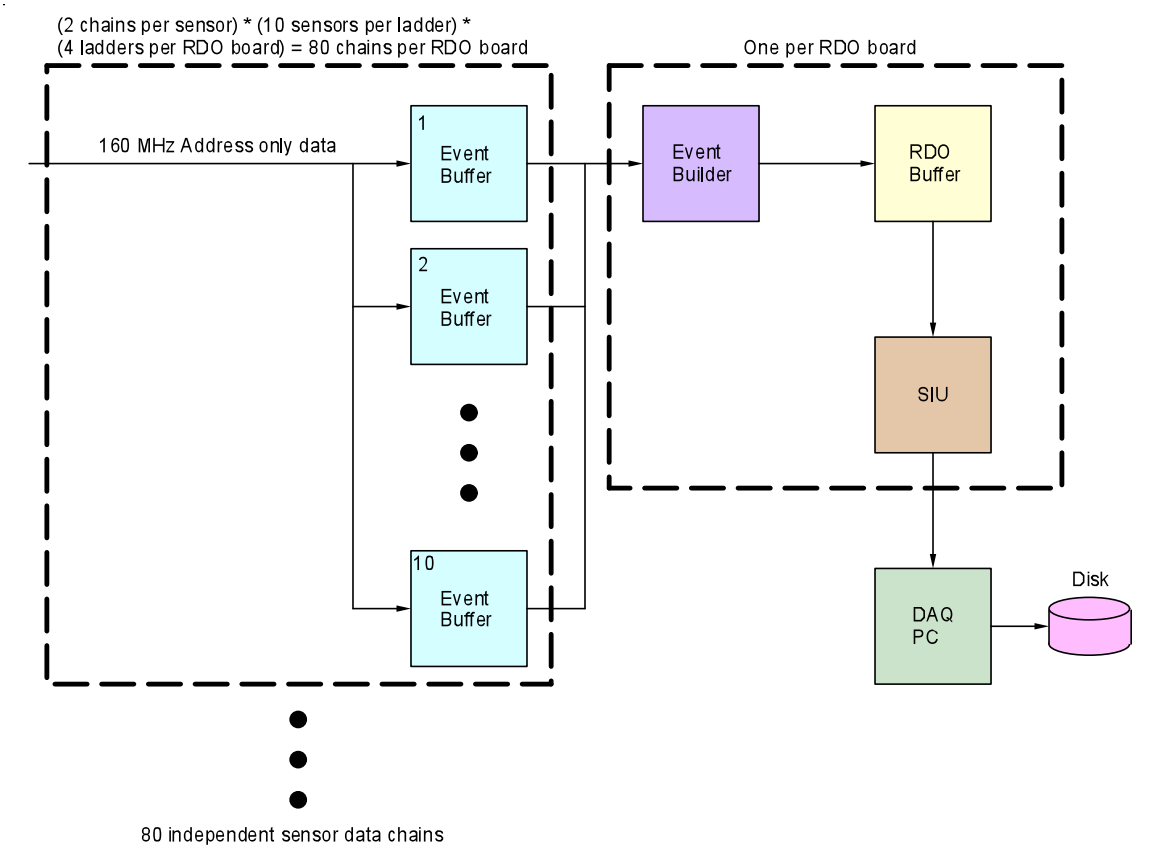


Figure 101: Functional schematic diagram for one Ultimate sensor based RDO board. Each RDO board services one inner ladder and 3 outer ladders. Each ladder contains 10 sensors.

Data transfer into event buffers – The 21-bitaddress data is presented to the event buffer at 160 MHz. The integration time is now 200 μs giving an event buffer enable time of 200 µs.

Item	Number
Bits/address	20
Integration time	200 μs
Hits / frame on Inner sensors (r=2.5 cm)	246
Hits / frame on Outer sensors (r=8.0 cm)	24
Ultimate sensors (Inner ladders)	100
Ultimate sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5
Average Trigger rate	1 kHz

Table 31: Parameters for the Ultimate sensor based detector system.

Event Buffers – Again, we will calculate the amount of FPGA block RAM required for event buffering. The average inner sensor has 246 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (246 hits) × (21 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 6150 bits**.** Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each inner sensor output is 64,580 bits or 3,075 21-bit addresses**.

For the outer sensors, the event buffer size is calculated similarly. The average outer sensor has 24 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (24 hits) × (21 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 630 bits**.** Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each outer sensor output is 6300 bits or 300 20-bit addresses**.

Data transfer into the RDO buffer via the event builder –We will again assume a 160 MHz clock to move data in 20-bit wide address words. The event builder first adds a 128 Byte header that contains the trigger ID and other identifying information into the RDO buffer, and then moves the address data from the event buffers into the RDO buffer in 20-bit words. The average carrier event size is [(24 hits / sensor (outer)) × (10 sensors) × (3 ladders) + (246 hits / sensor (inner)) × (10 sensors) × (1 ladders)] × (2.5 hits / cluster) = **7950 address words (21-bit)**. The RDO buffer is 5 × the size required for an average event and is thus **835 kb** in size. The full time required to transfer the address data into the RDO buffer (in 21-bit per clock transfers) is then **49.7 μs**.

Data transfer from the RDO buffer over the DDL link – The RDO buffer is dual-ported and thus readout from the SIU to the RORC can proceed as soon as the RDO buffer begins filling. Again, we will assume that we are padding the 20-bit address data to 32-bit word lengths for DDL transfer. The event size is then (32 bits) × (7950 address words) **= 254.4 kb or 31.8 kB.** In this example, our transfer rate is ~ 200 MB / s. This transfer then takes **159 μs.**

Data transfer to the STAR DAQ for event building – Again, only the events that have been accepted by level 2 are then built into an event. In this way, the buffer provided by the DAQ PC RAM provides for the elasticity needed for an average event acceptance of 1 kHz.

The results of these calculations and discussion are presented below in the chronograms in Figure 102 and Figure 103.

The system memory resource requirements are somewhat less than those required for the Phase-1 RDO system. This fits easily into the memory resources of the Virtex-5 FPGA.

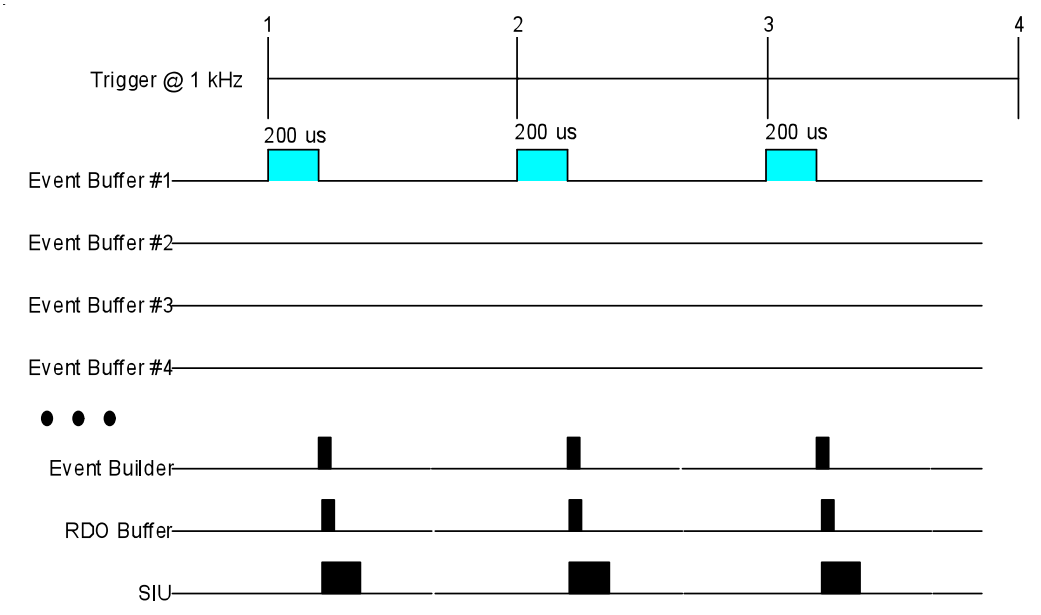


Figure 102: Chronogram of the Ultimate sensor based readout system functions for a 1 kHz periodic trigger.

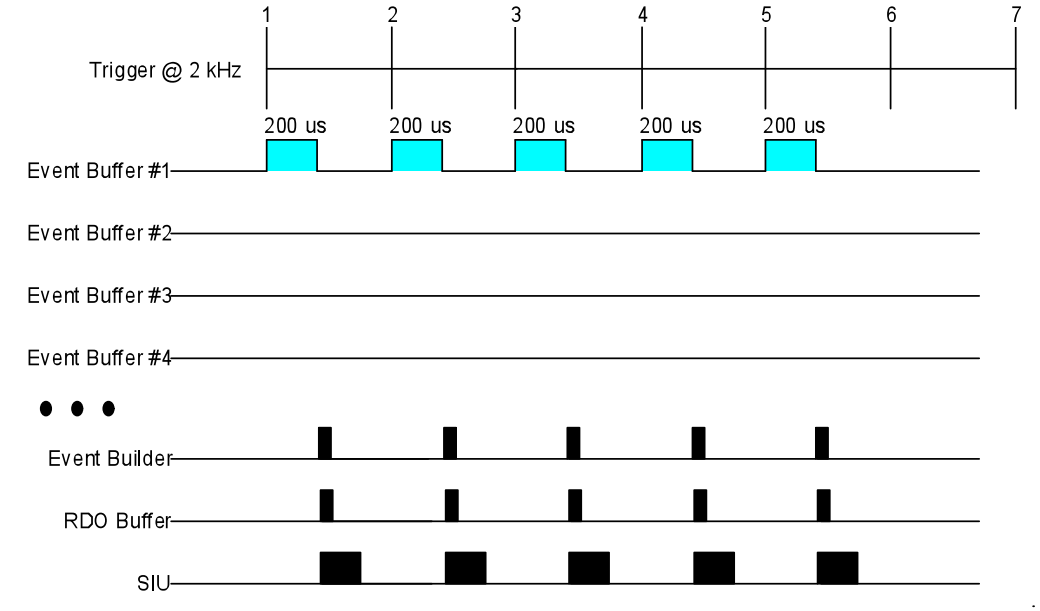


Figure 103: Chronogram of the Ultimate sensor based readout system functions for a 2 kHz periodic trigger.

9. Appendix 3

9.1. LVDS Data Path Testing Discussion

The readout system architecture for the Phase-1 and Ultimate sensors to be used in the PXL detector for the Heavy Flavor Tracker upgrade at STAR contains a high speed digital data path that is required to read out the sensor hits during the sensor integration time. This data path is well described in the addendum to the HFT proposal and can be found at http://rnc.lbl.gov/hft/hardware/docs/Addendum_rdo_2007_12_26.pdf. The RDO sensor data interface path requires that LVDS data move over a total distance of 6 – 8 meters with a frequency of 160 MHz for Phase-1 and 125 MHz for Ultimate. 1-2 meters of this distance is over high impedance fine twisted pair wire. Since this design is challenging, though it works on paper, it is prudent to make a prototype set of testing boards and check the performance of our design as a precursor to starting a production design for the final set of readout boards. A diagram of the physical layout of the parts of the PXL RDO system is shown as Figure 104.

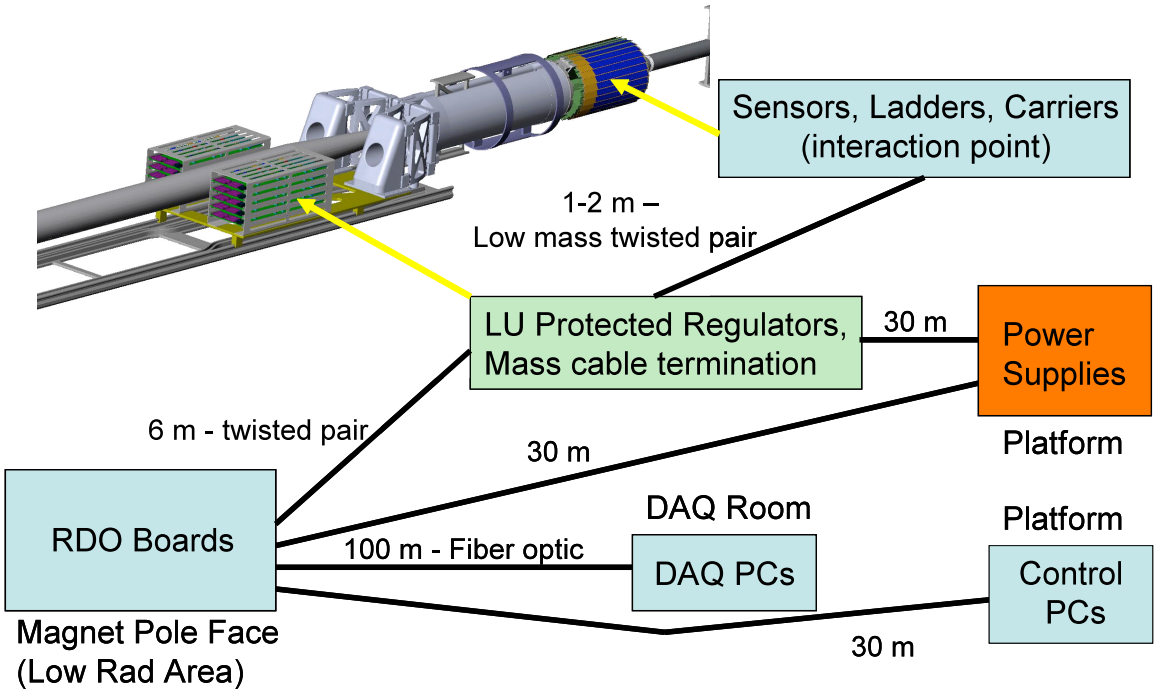


Figure 104: Physical layout of the RDO system.

To accomplish this testing task, we have constructed a set of PCBs that mock the components expected to be used in the final system. A functional system diagram is shown in Figure 105. We intend to produce a system that is a mockup of the complete data path for a single ladder starting and returning from the Virtex-5 development board. The wire used to connect the system boards will be the same as what we expect to use in the final system. The fine twisted pair wire bringing LVDS signals to and from the ladders are 42 AWG Wiretronic part # 2-42QPN-05 in two tested

lengths, 1.0 m and 2.3 m. The cables carrying the LVDS signals from the mass termination boards to the Virtex-5 interface readout boards are 3M type 3644 CL2 rated.

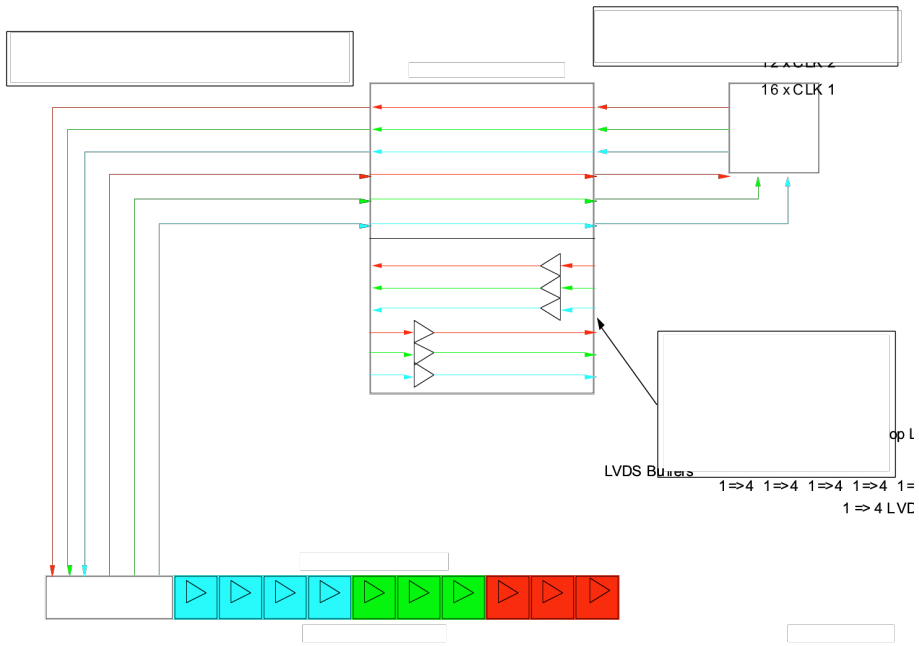


Figure 105: Functional block diagram of the LVDS data path test system.

9.1.1. Hardware

There are four basic components to the test system:

1. Mock Ladder – We have constructed a mock ladder. Since Phase-1 sensors are not available, we have used an LVDS 1:4 fan-out chip SN65LVDS104 to take the place of the Phase-1 sensor. The mock ladder contains ten SN65LVDS104s on 2 cm spacing, and six FIN1108 8-port LVDS repeater chips as buffers at the end of the ladder. The mock ladder receives 3 input LVDS signals that are multi-dropped in groups of 4, 3 and 3. Correspondingly, there are 40 outputs that are buffered at the ends of the mock ladder and carried to the Mass termination board. The mock ladder is constructed of standard FR4 with copper traces and has a finish thickness of 0.032" for 4 layers. We have constructed two mock ladders. They are identical except for the fine twisted pair signal wire lengths of 1.0 and 2.3 meters. A photograph of the mock ladder is shown as Figure 106.
2. Mass termination board – The mass termination board (MTB) is a close model of what we expect to have for a single ladder in the final system. Latch-up protected power is generated on the MTB and delivered to the mock ladder via 24 AWG wire. In the interest of testing multiple possible signal paths, the MTB used in these tests has two possible data paths. One is straight through from input to output connectors. The other is buffered with the same FIN1108 parts used on the mock ladder. A photograph of the MTB is shown as Figure 107.
3. Virtex-5 interface – The Virtex-5 interface board (V5IB) attaches to the Xilinx Virtex-5 development board with 1200 contact points. The data signals into and out of the Xilinx V-5 are buffered on the V5IB with FIN1108s and there are test points to look at all differential signals.

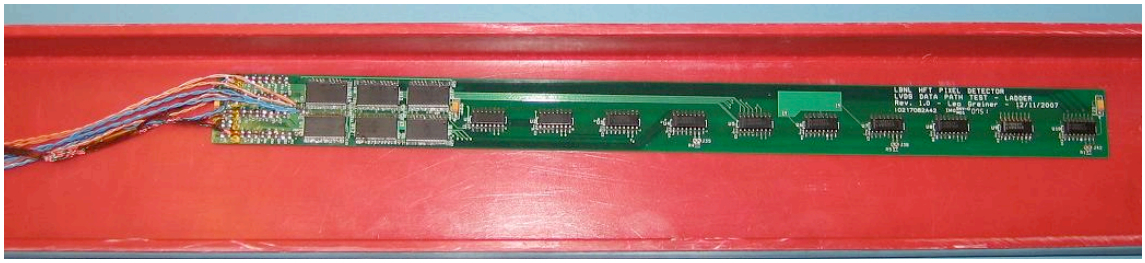


Figure 106: Mock ladder PCB as used in the tests.

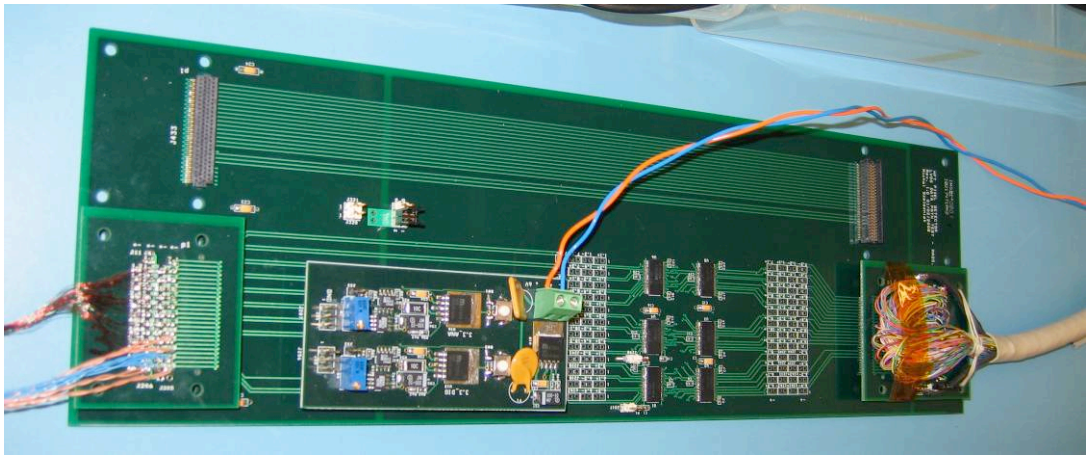


Figure 107: Mass termination board as used in the test. Ladder connections are on the left hand side of the board, a 6m cable to the Virtex5 interface RDO board is on the right. The daughter card mounted in the middle of the board supplies latch up protected and monitored power. Note that there are two data paths. One is un-buffered and the other is buffered through Fin1108 LVDS buffers.

9.1.2. Firmware and Software

The firmware and software developed for these tests have the primary task of measuring the time offsets needed to calibrate the IODELAY elements in the Virtex-5 FPGA. The IODELAY element is a function in the Xilinx Virtex-5 family of FPGAs that allows for the adjustment of the latching time on any input pin(s) with a very fine granularity. This is the essential functionality that allows us to do a channel-by-channel adjustment for each input. This compensates for all fixed time shifts in the system due to cable lengths, buffer propagation times, etc. and allows the data transfer to be limited only by the intrinsic system jitter. There are two modes for operation of the firmware. The first mode of operation is a calibration of the system. In this mode, the firmware sends a single pulse through each channel of the system. The transit time through the system is measured for each LVDS channel and the data is sent over the fiber optic communication link (SIU) to the software in the DAQ RDO PC. The firmware then executes a sequence of steps where the timing of the latching of data into each of the FPGA inputs is varied in 75 ps steps via the IODELAY element and the transition of the received pulse from one clock cycle into the next is observed. This procedure is repeated 20 times for each input to map the range of the jitter envelope. The data is transferred via the SIU into the software in the DAQ PC where it is used to calculate the optimum delay setting for each individual input that places the average midpoint of the data pulse at the FPGA latch time. The data is then transferred back into the FPGA to set the optimum delay for each i/o pin and the FPGA is then set to the bit error rate

mode. In this mode, pseudo random data is generated and transferred (with different offsets) over the three data outputs. In the firmware, each data path is checked against what was sent and errors are counted.

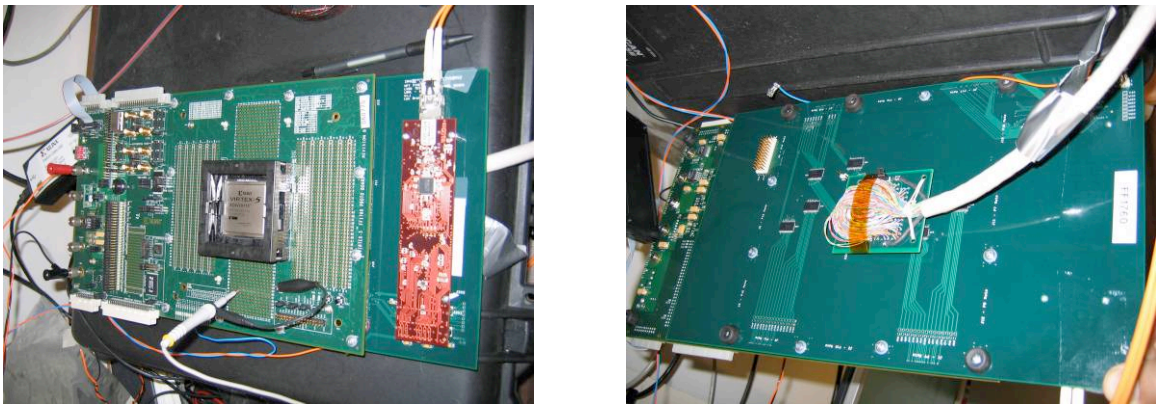


Figure 108: Virtex-5 interface board mounted to the Xilinx Virtex-5 development board. The top view is shown in the left hand diagram. It shows the Xilinx Virtex-5 development board on top with the SIU visible on the V5IB. The photograph on the right shows the cable attachment and test points on the V5IB.

9.1.3. Operation of the LVDS Test System

The Virtex-5 development board generates 3 streams of pseudo random data that are fed through the data path chain and returned to the V5IB. Each stream of data is compared to what was sent and any errors are counted. The results are then displayed on LEDs on the V5 development board and can be read out over the SIU interface. In this way we have tested the following;

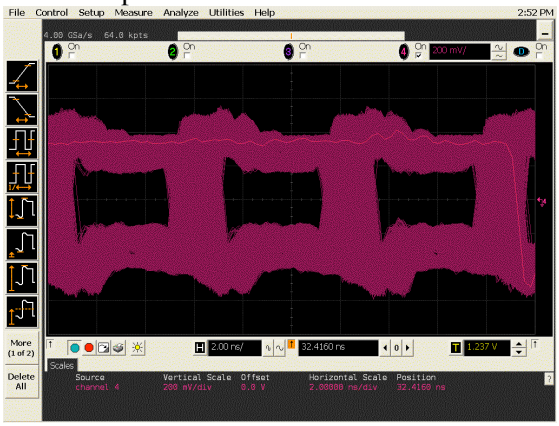
- 1 full data path for a complete ladder.
- Multi-drop LVDS distribution in groups on 4, 3, 3.
- Cross-talk through the whole system – each muti-drop group carries different random data.
- The signal paths on the PCBs and the cabling are as comparable as possible to the final implementation.
- External SIU communication and software/firmware to set IODELAY for each channel.
- Bit error rate for different read out frequencies, paths, cables, etc.

9.1.4. Results

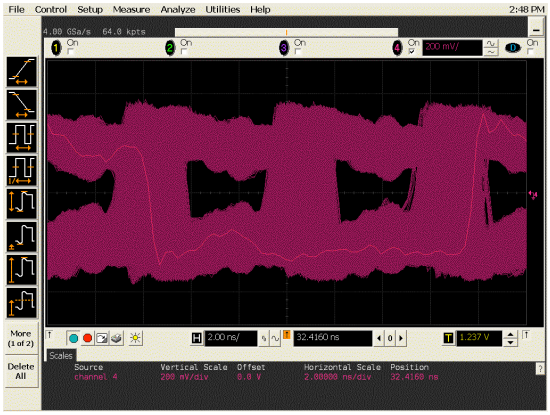
The test system was used to evaluate the system response to data transfer frequency, fine twisted pair wire length and buffering in the data path on the MTB. Some representative eye patterns are shown below.

Oscilloscope pictures with 2ns per division:

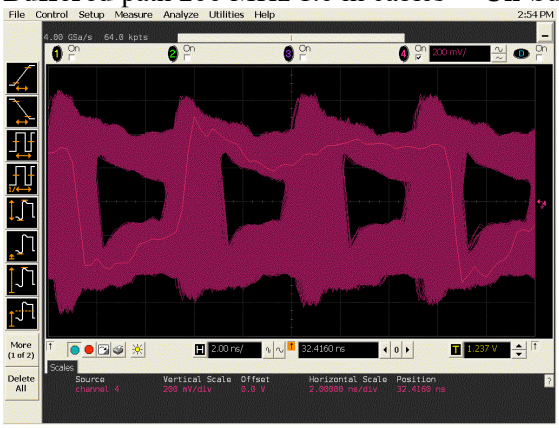
Buffered path 160 MHz 1.0 m cables



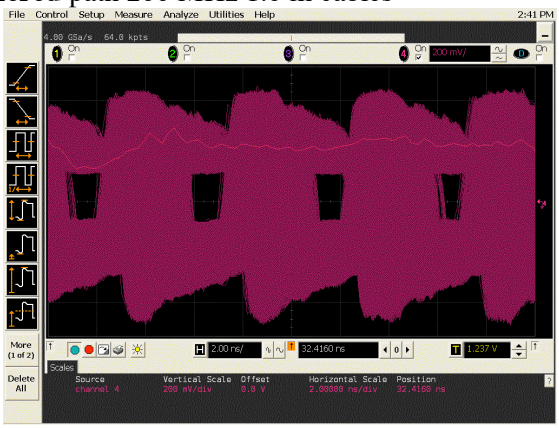
Un-buffered path 160 MHz 1.0 m cables



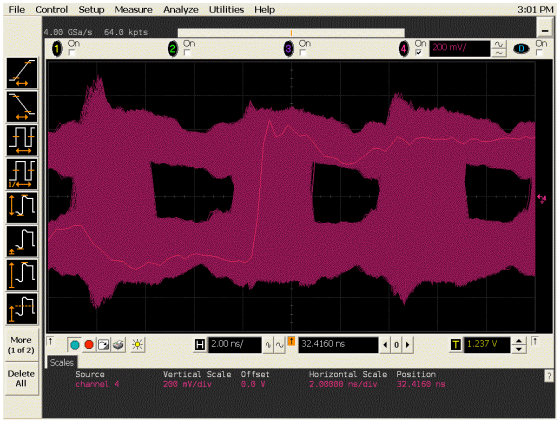
Buffered path 200 MHz 1.0 m cables



Un-buffered path 200 MHz 1.0 m cables



Buffered path 160 MHz 2.3 m cables



Buffered path 200 MHz 2.3 m cables

Bit Error Rates (BER) results are summarized in Table 32.

	160 MHz	200 MHz
Buffered path	1.0 m tp cables BER ~10^{-15}	1.0 m tp cables BER ~10^{-15}
	2.3 m tp cables BER ~10^{-15}	2.3 m tp cables BER ~10^{-10}
Unbuffered path	1.0 m tp cables BER ~10^{-15}	1.0 m tp cables BER ~~10^{-15}
	2.3 m tp cables BER = high	2.3 m tp cables BER = high

Table 32: Bit error rates for two different configurations.

Long data runs were taken with the buffered path at 160 and 200 MHz to give the results shown in the table above. In addition, we used a heat gun to heat the LVDS fan out chips on the mock ladder to 50 degrees C to look for temperature change induced errors. None were observed at the above frequencies. The increased error rate for the fine 2.3m twisted pair data wires on the un-buffered paths is not unexpected. The resistance of the 42 AWG twisted pair wire is 5.5 Ω/m and a buffer is required on the MTB to restore the signal integrity.

Conclusions

The conclusions from the LVDS data path test are given below:

- We have prototyped a one ladder RDO data path in a detector system that consists of 40 parallel ladder readout systems.
- Bit error rates are measured at ~ 10^{-15} (equivalent of ULTRA-2 SCSI or about one error every week / 40 ch @ 200 MHz) for the configurations that are candidates for use in the final system.
- The prototyping is considered a success as the very low error rate is quite acceptable and would result in a very small inefficiency or fake hit rate in the Phase-1 detector. The error rate for Ultimate is expected to be lower due to the decreased readout speed.
- The RDO system architecture is considered to be validated and we are now working on the design of the full functionality prototype.

References

[1] X. Zhu, N. Xu, P. Zhuang, Phys. Rev. Lett. 100, 152301 (2008); X.Zhu, M. Bleicher, S.L. Huang, K. Schweda, H. Stoecker, N. Xu, P. Zhuang. Phys. Lett. B647, 366 (2007).
[2] S.H. Lee, K.Ohnishi, S. Yasui, I-K.Yoo, C.M. Ko, Phys. Rev. Lett. 100, 222301 (2008).
[3] Y. Oh, C.M. Ko, S.H. Lee, S. Yasui, Phys. Rev. C 79, 044905 (2009).
[4] C. Chasman et al., LBNL # 5509-2008, http://rnc.lbl.gov/hft/docs/hft_final_submission_version.pdf
[5] J. Adams et al., STAR Collaboration, *Phys. Rev. Lett.* 94, 062301 (2005).
[6] http://www.agsrhichome.bnl.gov/RHIC/Runs/RhicProjections.pdf
[7] S.S. Shi, STAR Collaboration, Quark Matter Conference, 2009.
[8] V. Greco, C.M. Ko, and R. Rapp, Phys. Lett. B595, 202 (2004).
[9] J. Adams et al., STAR Collaboration, Phys. Rev. Lett. 91, 172302 (2003).
[10] C. Adler et al., STAR Collaboration, Phys. Rev. Lett. 90, 082302 (2003).
[11] M. Gyulassy and M. Plümer, Nucl. Phys. A527, 641c (1991).
[12] Y. L. Dokshitzer and D.E. Karzeev, Phys. Lett. B 519, 199 (2001).
[13] B.I. Abelev et al., STAR Collaboration, Phys. Rev. Lett. 98, 192301 (2007).
[14] G. D. Moore and D. Teaney, Phys. Rev. C 71**,** 064904 (2005).
[15] H. van Hees et al., Phys. Rev. C 73, 034913 (2006).
[16] B.I. Abelev et al., STAR Collaboration, Phys. Rev. Lett. 97, 152301 (2006).
[17] M.A.C. Lamont et al., STAR Collaboration, J. Phys. G32, S105 (2006).
[18] S.A. Voloshin, Nucl. Phys. A715, 379 (2003); R.J. Fries, B. Mueller, C. Nonaka, and S.A. Bass, Phys. Rev. Lett. 90, 202303 (2003); V. Greco, C.M. Ko, and P. Levai, Phys. Rev. Lett. 90, 202302 (2003).
[19] A. Andronic et al., Phys. Lett. B571 36 (2003).
[20] S. H. Lee et al., arXiv: 0709.3637v3.
[21] X. Dong and P. R. Sorensen, Phys. Rev. C **74**, 024902 (2006).
[22] B.I. Abelev et. al., STAR Collaboration, Phys. Rev. Lett 98,192301 (2007).
[23] J. Adams et al., STAR Collaboration, Phys.Rev.Lett. 91, 172302 (2003).
[24] O. Barannikova et. al., STAR Collaboration, Nucl. Instrum. Meth. A558, 419 (2006).
[25] T. Sjöstrand, Comp. Phys. Commun. 82, 74 (1994).
[26] X. Lin et al., STAR Collaboration, J. Phys G34, S295 (2007); G. Wang et al., STAR Collaboration, arXiv:0804.4448.
[27] D. Acosta et al., CDF Collaboration, Phys. Rev. D 71, 092001 (2005).
[28] F. Abe et al., CDF Collaboration, Phys. Rev. D 57, 9 (1998).
[29] C. Amsler *et al.*, Phys. Lett. B667, 1 (2008).
[30] A. Adare et al., PHENIX Collaboration, Phys. Rev. Lett. 98, 232002 (2007).
[31] Private communication with J. Dunlop.
[32] M. Calderon, et al http://www.star.bnl.gov/protected/heavy/www/proposals/onium.pdf
[33] Private communication with H. Crawford.
[34] R. Turrisi et al., ALICE Collaboration, ACTA PHYSICA POLONICA B38, 1039 (2007).
[35] M. Cacciari et al., Phys. Rev. Lett. 95, 122001 (2005).
[36] S. Sakai, J. Phys. G: Nucl. Part. Phys. 3, 064056 (2009).
[37] H. van Hees et al., ArXiv: 0808.3710.
[38] M. Kaneta, PHENIX Collaboration, J. Phys. G: Nucl. Part. Phys. 30, S1217 (2004).

[39] G. Bunce et al., Ann. Rev. Nucl. Part. Sci. 50, 525 (2000).
[40] G. Bunce et al., 'Plans for the RHIC Spin Physics Program', BNL Internal Report submitted to DOE Nuclear Physics, June 2009.
[41] D. de Florian et al., Phys. Rev. Lett. 101 072001 (2008).
[42] D. de Florian et al., hep-ph 0904.3821v1.
[43] L. Greiner et al., Nucl. Instr. Meth. A 589, 167 (2008).
[44] M.J. French et al., Nucl. Instrum. Meth. A466, 359 (2001).
[45] L. Arnould, *et al*., Nucl. Instrum. Meth. A 499, 652 (2003).
[46] H. Bichsel, Review in Modern Physics, vol.60, pp. 663, (1988).
[47] "Modeling, Design, and Analysis of Monolithic Charged particle Image Sensors" Shengdong Li, Ph.D thesis, Univ. of California, Irvine, 2007.