SSD electronics status report

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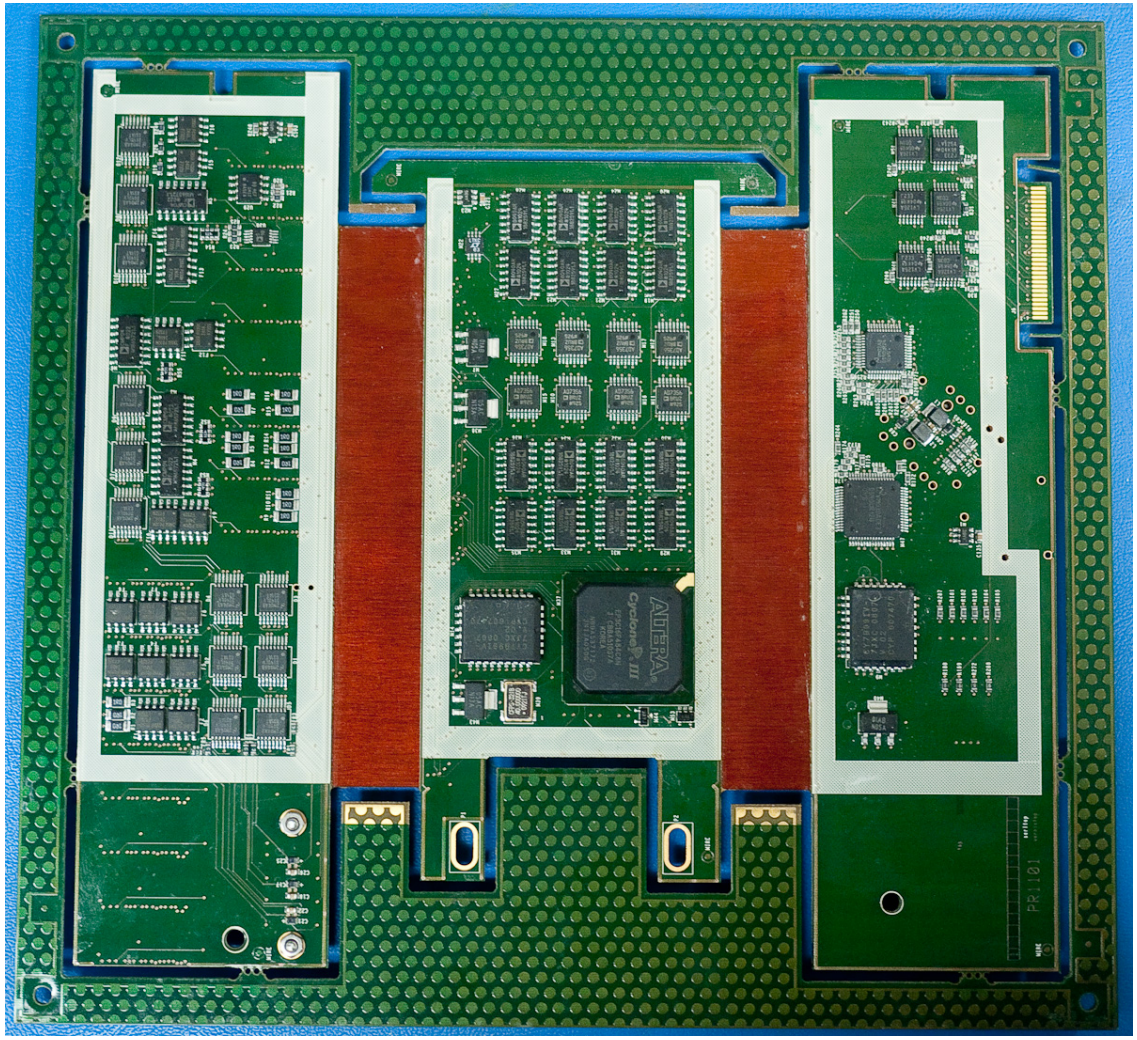
Project scope – readout upgrade

- Ladder card
- QRDO
- RDO (VME card)
- DAQ computers
- Slow controls
- Power supplies

Ladder card

Prototype ladder board

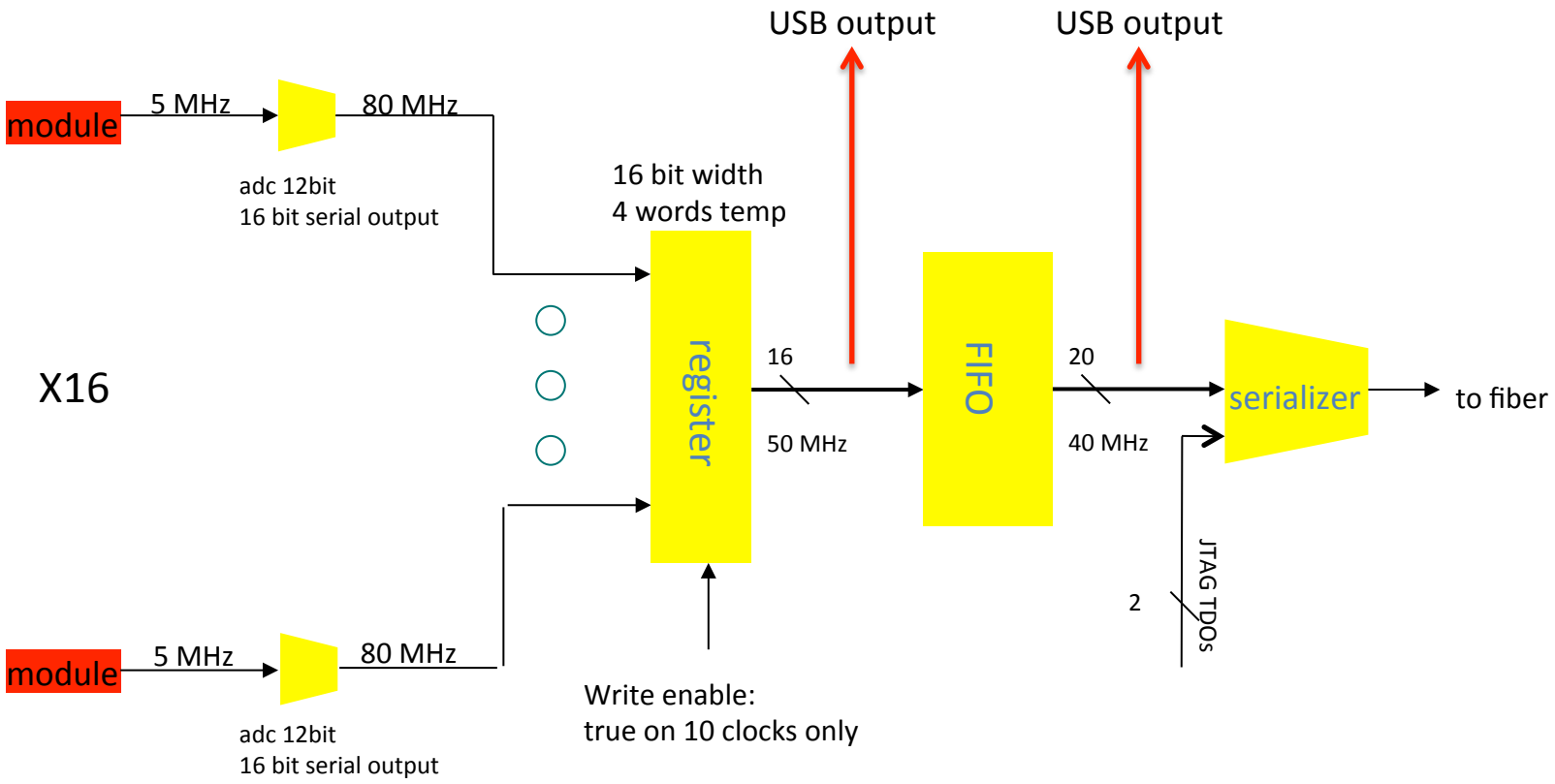


Ladder card hardware

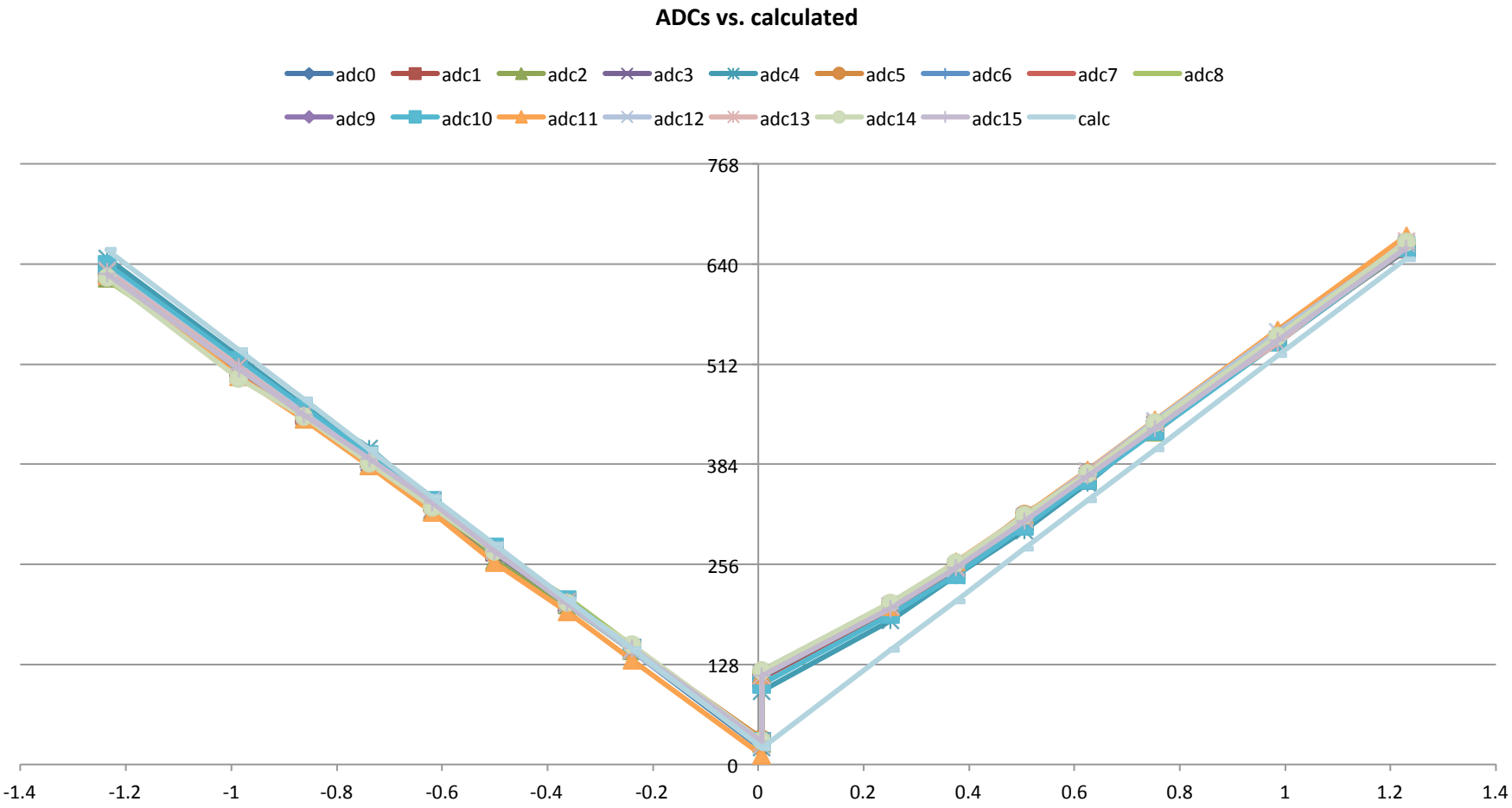
- Testing of ladder card has only exposed 2 problems
  - FPGA orientation
    - Will be corrected on production version
  - Susceptibility of analog section to PS variation
    - Can degrade ability to interpolate centroid
    - Will be corrected on production version

Verification of packing code

- USB output for ADC data
- Install USB spy at output of FIFO



Analog response for all ADCs



Analog response

- Non-linear behavior of N-face needs to be understood
  - not a show stopper
- Discovered we are sensitive to PS fluctuations via DAC
  - production version will address this problem

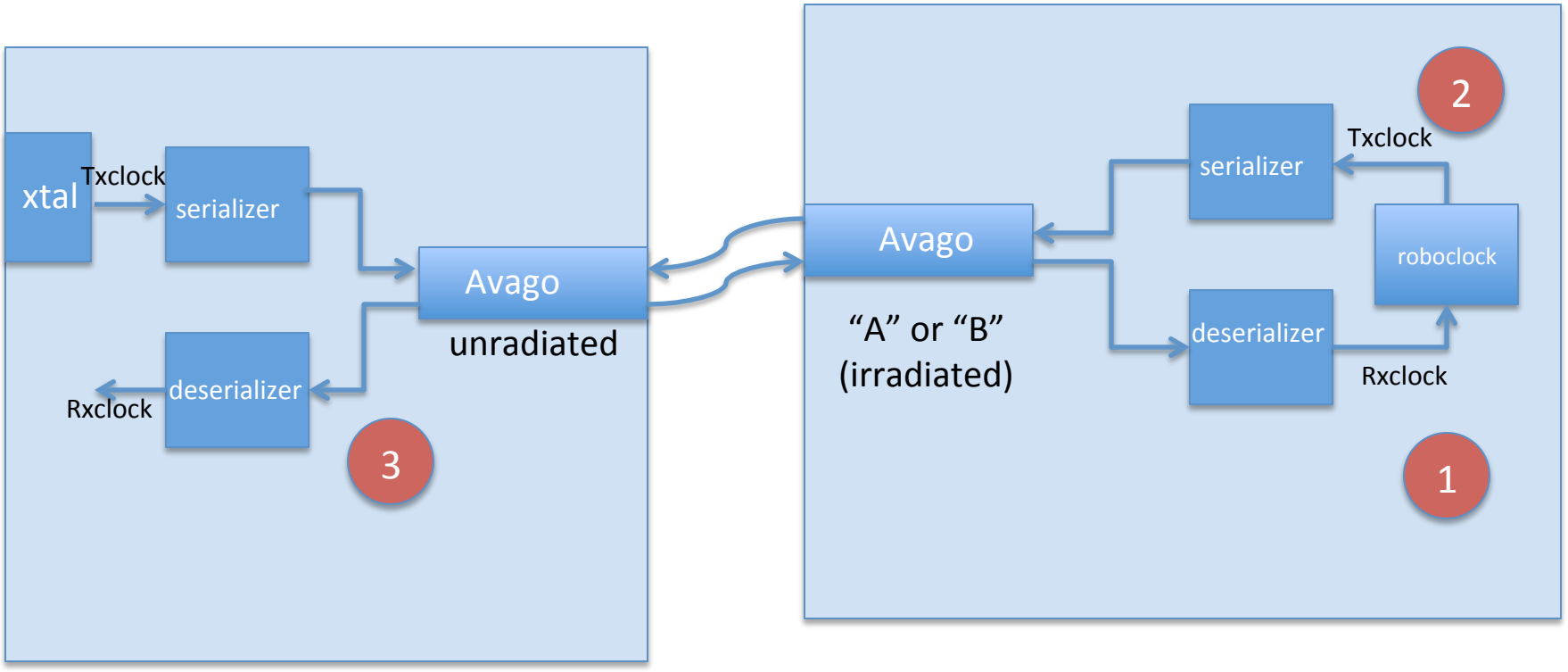
Determining radiation tolerance

- SSD DAQ review raised this as an action item
- Optical transceiver may be the most susceptible to radiation damage
- Observations on the operation of Avago optical transceivers after irradiation with γ-radiation

Measurement program

- Two Avago optical transceivers, model AFBR-57M5APZ, were subjected to γ-radiation from a Co-60 source at BNL.
  - Transceiver “A” received a dose of 100 kRad
  - “B” received 200 kRad
- These transceivers were tested in an existing setup, consisting of the prototype ladder card and the QRDO (prototype of the RDO).

Measurement setup



QRDO

Ladder card

Observations

Ladder Avago	Ladder Rclock (1)	Ladder Tclock (2)	QRDO Rclock (3)	comment
Normal	40MHz good	40MHz good	40MHz good	normal
A (100 kRad)	40MHz good	40MHz good	Absent	Several trials
B (200 kRad)	Absent	Absent	Absent	Trial 1
B(200 kRad)	16MHz	16MHz	Absent	Trial 2

Interpretation:

- 100 kRad kills transmitter
- 200 kRad kills receiver

Different results for "B" trials due to marginal signal.
[Clock observed has wrong frequency.]

Expected Radiation 2014

Rad cm			2.5	2.5	14.0	22.0	2.5	2.5	14	22
		# of wks	Phys krad	Phys + UPC krad	Phys krad	Phys krad	Ramp and Total krad	Ramp and Total n/cm²	Ramp and Total krad	Ramp and Total krad
200 GeV	Au + Au Max	12	28.3	59.8	0.9	0.4	88.0	1.1E+12	1.8	0.7
	Au + Au Min	12	5.3	11.3	0.2	0.1	16.6	0.2E+12	0.3	0.1
500 GeV	p + p Max	12	133.3	133.3	4.3	1.7	266.7	5.3E+12	8.5	**3.4**
	p + p Min	12	28.9	28.9	0.9	0.4	57.8	1.1E+12	1.8	0.7

Expected radiation (Wieman)

	Radius [cm]	200 GeV	200 GeV	500 GeV	200 GeV
		Au+Au Max	Au+Au Min	p+p Max	p+p Min
Physics	**2.5**	28	5.3	133	29
Physics+UPC		60	11	133	29
Total		**88**	**17**	**267**	**58**
Physics	**14**	1	0.2	4	1
Total		**2**	**0.3**	**9**	**2**
Physics	**22**	0.4	0.1	2	0.4
Total		**1**	**0.1**	**3**	**1**

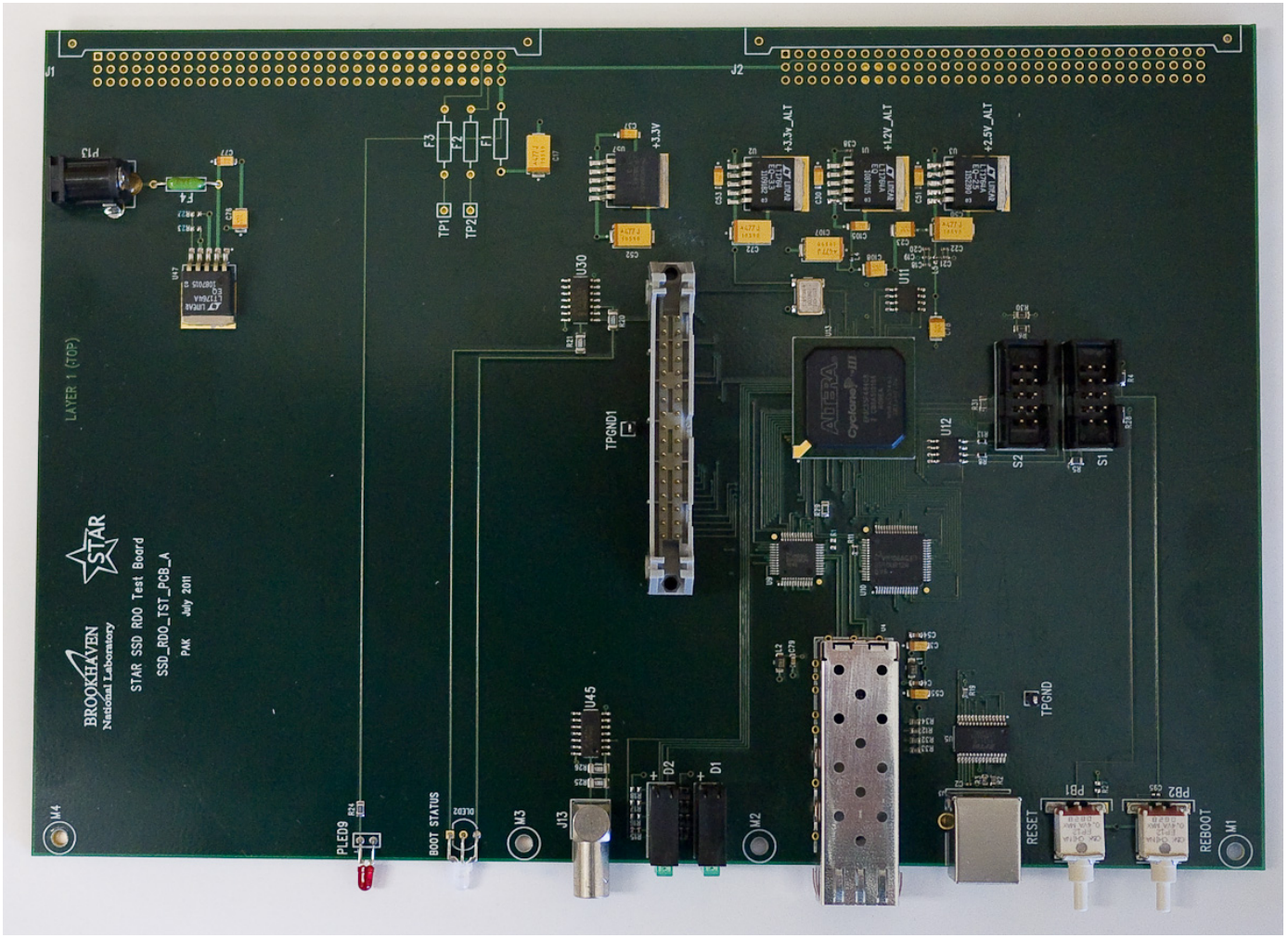
Table 1: Radiation field in kRad in the center of STAR extrapolated to RHIC II luminosities for different radial positions for 12 weeks of run time for the radii of PXL layer 1, the IST, and the SSD.

Radiation: conclusions

- There is a possibility that after 2-3 years of running we will start to see failures in the Avago transceiver
- Ongoing project (ATLAS) to develop a rad hard substitute for the Avago transceiver
  - Samples available this CY
  - We need to make a minimal change in the ladder card (Vcc) to accept this rad hard version
- ATLAS project has monitored the behavior of an Avago transceiver while being irradiated
  - Sample size: 1
  - Failure occurs at 75 kRad

QRDO

QRDO


J1
J2
P13
F3
F2
F1
TP1
TP2
+3.3V
+3.3V_ALT
+1.2V_ALT
+2.5V_ALT
U30
U11
U12
TPGND1
TPGND
S2
S1
LAYER 1 (TOP)
BROOKHAVEN
National Laboratory
STAR
STAR SSD RDO Test Board
SSD_RDO_TST_PCB_A
PAK July 2011
U45
D2
D1
PLED9
BOOT STATUS
J13
M4
M3
M2
M1
RESET
REBOOT
PB1
PB2

Testing with QRDO

- Verify ADC data arriving via fiber same as USB version local to ladder card ✔
- Confirm JTAG behavior via fiber ✔
  - Slow control path to
    - ladder card and
    - hybrids on ladder (TBD)
- Configure ladder FPGA via the fiber (TBD)
  - Each ladder FPGA has its own serial prom on the RDO, managed by the slave FPGA
  - Mostly a question of verifying/debugging QRDO firmware

JTAG components

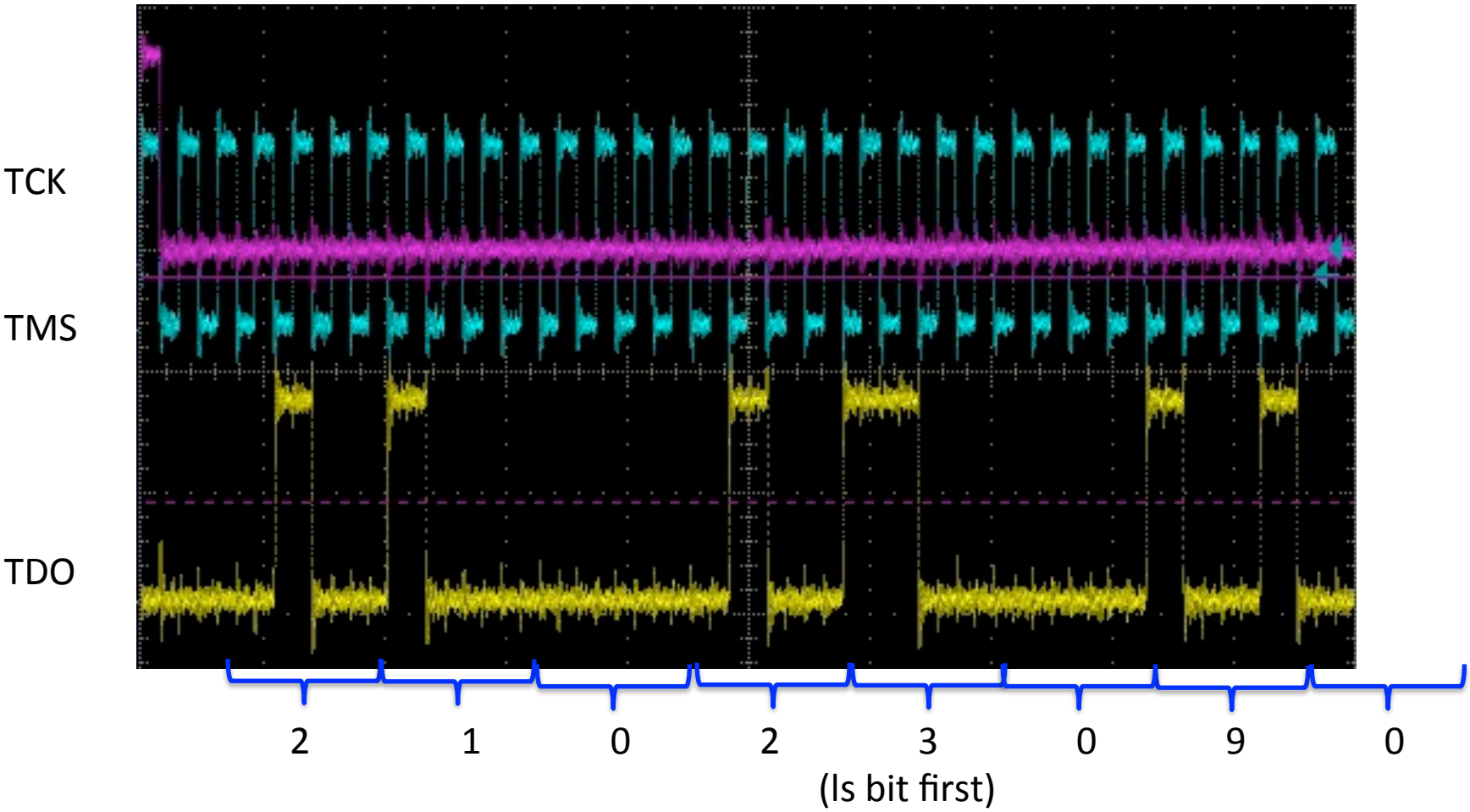
- Ladder card firmware
  - Already verified using local JTAG via debug card
- QRDO firmware (transport layer)
- PC/linux software

- Implemented so far:
  - Write to ladder board-resident register
  - Non-destructive read of ladder board-resident register
  - TBD – access registers in hybrids

- Results on following slides

JTAG testing 1

Read version date register (contents = 0x09032012)



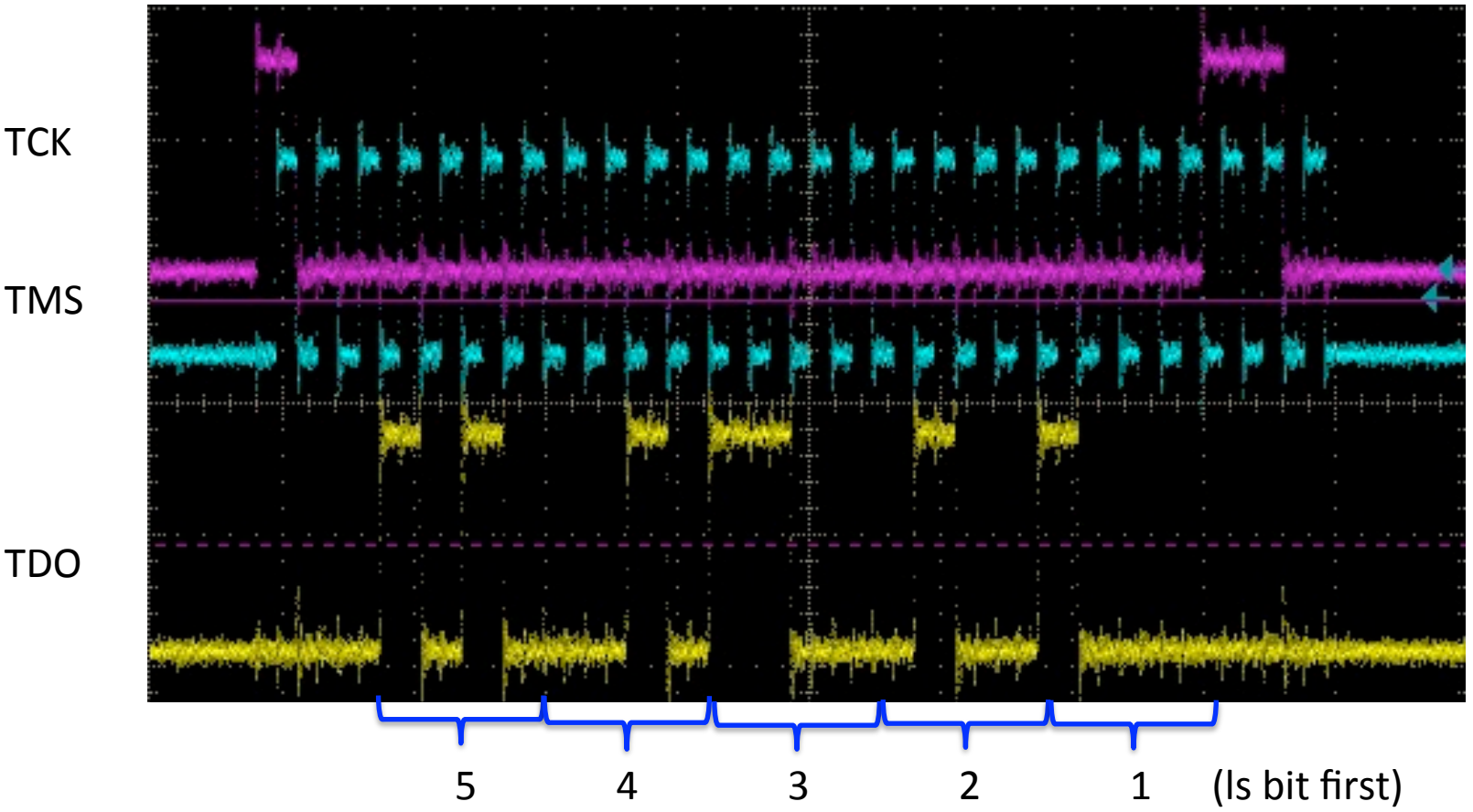
JTAG testing 2

./read_reg 12
Version date register

invoked as ./read_reg 12
ssdReadReg: read_buf[0]:
1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 1 0
ssdReadReg: read_buf[1]:
1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 1 1
ssdReadReg: tempint[0]:
0 0 1 0 0 0 0 0 0 0 1 0 0 1 0
ssdReadReg: tempint[1]:
0 0 0 1 0 0 0 0 0 0 0 0 0 1 1
Reading register 0x0c: 0x10 0x03 0x20 0x12
DD MM YYYY

JTAG testing 3

Read register 4 (contents = 0x12345)



JTAG testing 4

./read_reg 4
DAC values (initialized as 0x12345)

invoked as ./read_reg 4
ssdReadReg: read_buf[0]:
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1
ssdReadReg: read_buf[1]:
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0
ssdReadReg: tempint[0]:
0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1
ssdReadReg: tempint[1]:
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
Reading register 0x04: 0x01 0x23 0x45

RDO

RDO

Principal functional blocks:

Fiber interface to ladders (5)

Slave FPGA

- 5 FPGAs, one per ladder
- Buffers for 4 event fragments
- Zero suppression

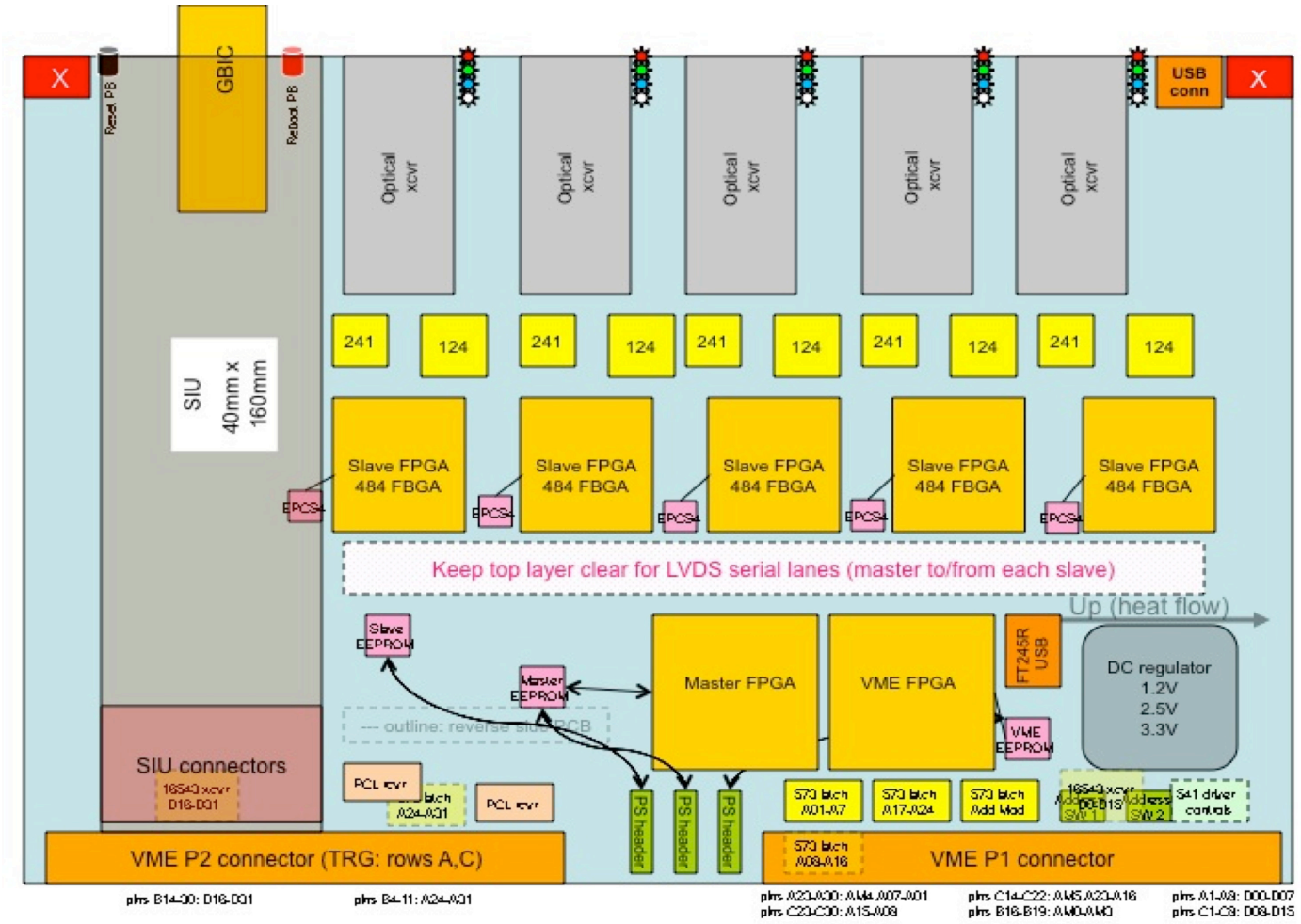
VME interface

- Slow control and debugging interface

Master – DAQ/TRG

- DDL interface to DAQ
- Event data, pedestal management
- Trigger command interface
- Event builder using fragments prepared by slave FPGAs

RDO layout


X
GBIC
Reset PB
Reboot PB
Optical xcvr
Optical xcvr
Optical xcvr
Optical xcvr
Optical xcvr
USB conn
X
SIU 40mm x 160mm
241
124
241
124
241
124
241
124
241
124
Slave FPGA 484 FBGA
Slave FPGA 484 FBGA
Slave FPGA 484 FBGA
Slave FPGA 484 FBGA
Slave FPGA 484 FBGA
EPCS4
EPCS4
EPCS4
EPCS4
EPCS4
Keep top layer clear for LVDS serial lanes (master to/from each slave)
Up (heat flow)
Slave EEPROM
Master EEPROM
Master FPGA
VME FPGA
FT245R USB
VME EEPROM
DC regulator
1.2V
2.5V
3.3V
--- outline: reverse side PCB
SIU connectors
16543 xcvr D16-D01
PCL xcvr
16543 xcvr A24-A31
PCL xcvr
PS header
PS header
PS header
S70 bitch A01-A07
S70 bitch A17-A24
S70 bitch Add Mod
16543 xcvr D08-D15
Address SW 1
Address SW 2
S41 driver control
S70 bitch A08-A16
VME P2 connector (TRG: rows A,C)
VME P1 connector
pins B14-30: D16-D01
pins B4-11: A24-A31
pins A23-A30: A14,A07-A01
pins C23-C30: A15-A08
pins C14-C22: A13,A23-A16
pins B16-B19: A12-A10
pins A1-A8: D00-D07
pins C1-C8: D08-D15

Master – slave communication

- Event data flow from 5 slaves to master
  - Concurrently
  - Using high-speed serial channels
  - 200 MB/s each channel
- Exceeds PLL capability in master FPGA
  - Abandon Altera implementation
  - Use C. Renard custom PLL
- Requires PCB to have equal round-trip times for all 5 slaves (~1cm tolerance)
- Works fine in simulation

Configuring the FPGAs

- RDO FPGAS can be configured
  - Via header (Master, VME, Slaves)
  - Via VME FPGA
    - USB
    - VME

RDO status

- FPGA code ✔
- Schematic ✔
- PCB layout – in progress
- Components – ordered

RDO (continued)

- VME is an obsolete environment
  - Can no longer buy CPUs
  - VxWorks
- USB - alternate slow control path
  - All building blocks have been implemented by Orsay for ALICE
  - Uses commercially available USB-FIFO interface
  - Same as we are using for debugging ladder card
- Layout cannot proceed until all FPGA pin outs have been assigned

Conclusion

Status

- Ladder card rerouting – in progress (critical path)
  - Expected finish 07/12
- Ladder card debugging
  - Analog finished
  - JTAG finished
  - Configuration - TBD (estimate 2-3 weeks)
- RDO board layout in progress
  - Expect 2 assembled boards end 4/12
- DAQ computers
  - 1 in house and configured
  - 1 en route to BNL