The STAR Heavy Flavor Tracker

Conceptual Design Report

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1.   Introduction

The Heavy Flavor Tracker (HFT) is a state-of-the-art microvertex detector utilizing active pixel sensors and silicon strip technology. The HFT will significantly extend the physics reach of the STAR experiment for precision measurement of the yields and spectra of particles containing heavy quarks. This will be accomplished through topological identification of D mesons by reconstruction of their displaced decay vertices with a precision of approximately 50 μm in p+p, d+A, and A+A collisions.

The HFT consists of 4 layers of silicon detectors grouped into three sub-systems with different technologies, guaranteeing increasing resolution when tracking from the TPC towards the vertex of the collision. The Silicon Strip Detector (SSD) is an existing detector in double-sided strip technology. It forms the outermost layer of the HFT. The Intermediate Silicon Tracker (IST), consisting of a layer of single-sided strip-pixel detectorssdetectors, is located inside the SSD. Two layers of Silicon Pixel Detector (PIXEL) are inside the IST. The PIXEL detectors have the resolution necessary for a precision measurement of the displaced vertex.

The PIXEL detector will use CMOS Active Pixel Sensors (APS), an innovative technology never used before in a collider experiment. The APS sensors are only 50 μm thick with the first layer at a distance of only 2.5 cm from the interaction point. This opens up a new realm of possibilities for physics measurements. In particular, a thin detector (0.28% radiation length per layer) in STAR makes it possible to do the direct topological reconstruction of open charm hadrons down to very low transverse momentum by the identification of the charged daughters of the hadronic decay.

2. Physics Motivation

The primary motivation for the HFT is to extend STAR's capability to measure heavy flavor production by the measurement of displaced vertices and to do the direct topological identification of open charm and bottom hadrons. These are key measurements for the heavy-ion and spin physics programs at RHIC. Heavy quark measurements will facilitate the heavy-ion program as it moves from the discovery phase to the systematic characterization of the dense medium created in heavy-ion collisions as well as obtain a detailed measurement of the nucleon spin structure in polarized p+p collisions. The primary physics topics to be addressed by the HFT include heavy flavor energy loss, flow, and a test of partonic thermalization at RHIC. This program has been identified as key goals for the RHIC program in the Long Range Plan RHIC-II science program and in the RHIC mid-term scientific plan.

From a precise measurement of the spectra and the production ratios of D-meson states, we will be able to extrapolate to the total yield for charm quark production. Furthermore, the open charm production rate is high enough at RHIC that the coalescence process becomes relevant for Charmonium production. Knowledge of the total production cross section for charm quarks is essential as a baseline for J/ψ measurements. A meaningful answer to the question of whether the J/ψ mesons are suppressed or enhanced at RHIC requires knowledge of the charm production in heavy-ion reactions.

A heavy quark can be used to probe the properties of the medium created in heavy-ion collisions. The radiation of gluons is kinematically suppressed for heavy flavored quarks passing through the medium: thus they should lose less energy in the dense medium. An important measurement to be made with the HFT is $R_{CP}R_{AA}$, the ratio of charmed meson production in central Au+Au collisions to the binary-scaled production rate in peripheral Auor +Au collisions. Current measurements using non-photonic electrons as a measure of the abundance of charm and bottom hadrons indicate that the rate of energy loss for heavy quarks is unexpectedly high and inconsistent with our current understanding in pQCD models. Based on the non-photonic electron data the theory of heavy quark energy loss is uncertain and may be completely wrong, especially with regards to bottom. The ability to separate and identify charm and bottom contributions is of crucial importance for such measurements.

Another important study to be made with the HFT is a measurement of the elliptic flow of D-mesons down to very low p_T values. It is generally accepted that elliptic flow is established in the partonic phase. If charm quarks, with a mass much larger than the temperature of the system, undergo elliptic flow then it has to arise from many collisions with the abundant light quarks. Thus, flow of charm quarks can be taken as a probe for frequent re-scatterings of light quarks and is an indication of thermalization that may be reached in the early stages of heavy-ion collisions at RHIC. We believe that proof of thermalization constitutes the last step in the characterization of the strongly interacting matter created at RHIC. These important measurements require a very thin detector to push the measurement down to very low transverse momenta where elliptic flow is manifest.

Without the HFT upgrade the STAR experiment will not be able to execute the comprehensive heavy flavor program proposed here. However, STAR has been able to complete some initial charm measurements with the TPC alone, and with the data from the recent Run 7 STAR might be able to make limited progress towards an initial estimate for the B-meson contribution to the spectrum of the non-photonic electrons in Au+Au collisions.

The complete physics case for the HFT has been presented in the HFT proposal[110] and has been vetted in the HFT Science Review. In this Conceptual Design Report we will present the physics capabilities of the HFT in terms of charm flow, charm suppression, Λ_C measurements, and the capability to distinguish between charm and bottom production. The first two points have been presented in detail already in the original proposal. Here we will present a brief summary of the first two items while concentrating on the latter two points.

2.1. Charm Flow

Charm quarks are abundantly produced at RHIC energies. Due to their high mass and small interaction cross section, the strength of elliptic flow of heavy flavor hadrons may be a good indicator of thermalization occurring at the partonic level. If all quarks in heavy flavor hadrons flow with the same pattern as the quarks in the light flavor hadrons, this indicates frequent interactions between all quarks. Hence, thermalization of light quarks is likely to have been reached through partonic re-scattering.

Figure 1 shows what precision in flow measurement can be reached with 500 M minimum bias events taken in STAR with the HFT. The red points show expectations from a cascade model[2] for the case that the charm quark has the same size partonic flow as measured for the light quarks. The green points show the limiting case where the charm quark has zero partonic v_2. Our measurement is expected to fall between those limits. It is obvious that the HFT will allow for a precision measurement that will shed light on the question of thermalization.

2.2. Heavy Quark Energy Loss

The discovery of a factor of 5 suppression of high p_T hadrons ($5 < p_T < 10$ GeV/c) produced in Au+Au collisions at RHIC and the disappearance of the away-side jet has been interpreted as evidence for jet quenching.[3,4] This effect was predicted to occur due to radiative energy loss of high energy partons that propagate through a dense and strongly interacting medium.[5] The energy loss of heavy quarks is predicted to be significantly less compared to light quarks because of a suppression of gluon radiation at angles $\Theta < M_Q/E$, where M_Q is the heavy quark mass and E is the heavy quark energy. This kinematic effect is known as the "dead cone" effect.[6] However, a recent measurement of the nuclear modification factor,[7] R_{AA}, for non-photonic electrons, the products of D- and B-meson decay, yielded the surprising result that D- and B-mesons apparently show the same large suppression of light hadrons. This clearly indicates that

the energy loss mechanism is not yet understood and has triggered new theoretical development.[8,9] In order to make progress in understanding the nature of the energy loss mechanism, it is important to measure R_{AA} or R_{CP} for identified D-mesons..
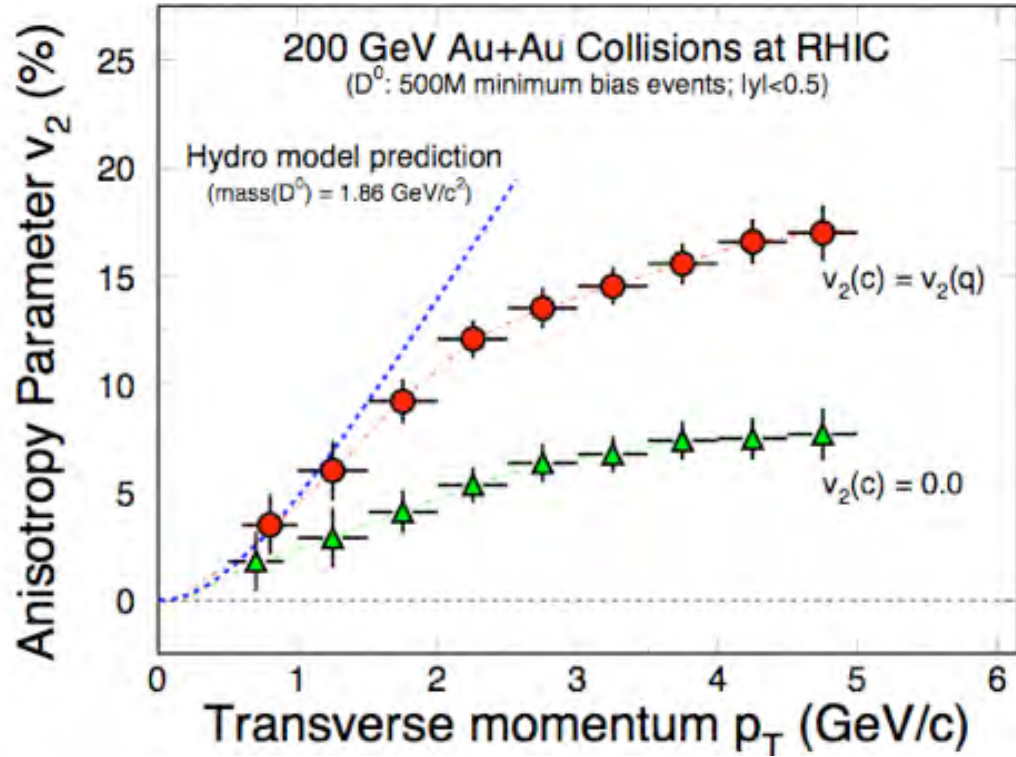
Figure 1: v2 as a function of p_T for the case of charm flow the same as light quark flow (red) and for the case where charm does not flow (green).
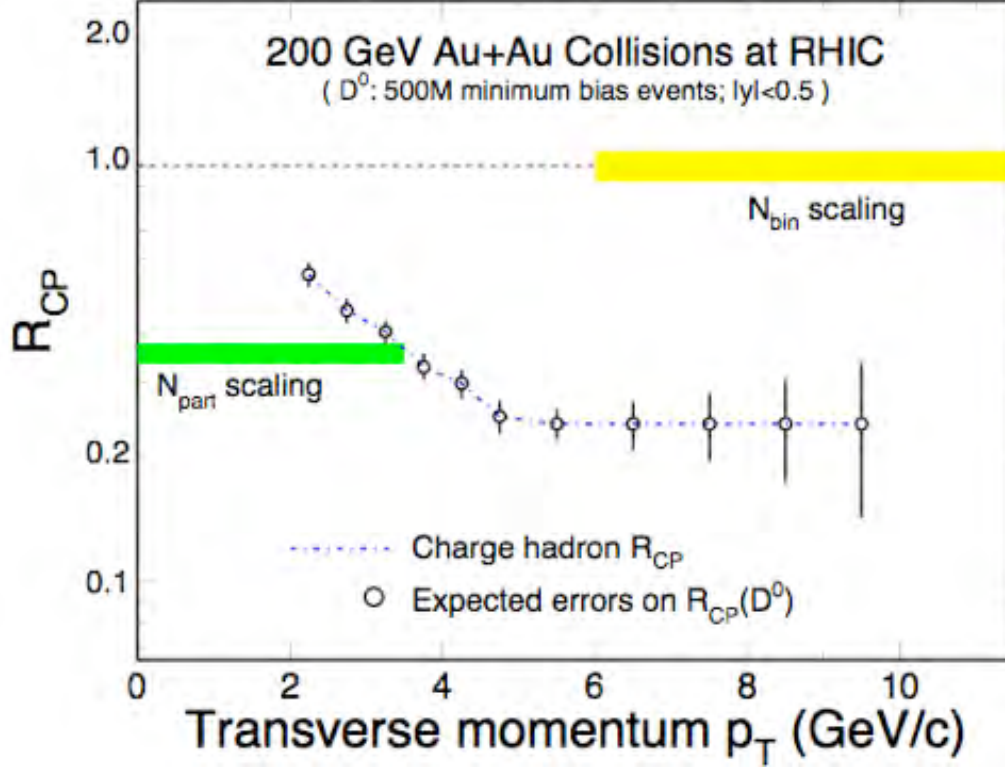
Figure 2: Expected errors for a R_{CP} measurement as a function of p_T.

Figure 2 shows the precision for R_{CP} that can be achieved with 500 M minimum bias events in STAR with the HFT under the assumption that the suppression for heavy quarks is of the same size as the suppression for the light quarks.

2.3. Λ_C-Baryons

In central Au+Au collisions at RHIC, a baryon to meson enhancement has been observed in the intermediate p_T region ($2 < p_T < 6$ GeV/c).[10,11] This is explained by a hadronization mechanism involving collective multi-parton coalescence rather than independent vacuum fragmentation.[12] The success of the coalescence approach implies deconfinement and possibly thermalization of the light quarks prior to hadronization.

Since Λ_c is the lightest charmed baryon and its mass is not far from that of the D^0 meson, a similar pattern of baryon to meson enhancement is expected in the charm sector.[13] Λ_C/D^0 enhancement is also believed to be a signature of a strongly coupled quark-gluon plasma.[14] Therefore it would be very interesting to measure R_{CP} of Λ_c baryons and compare it to R_{CP} of D^0 mesons. In addition, Λ_c/D^0 enhancement could be an explanation[15] for the large suppression of high- p_T electrons from charm and beauty decays.[16]

With the HFT STAR will be able to identify Λ_c baryons and to perform a measurement of R_{CP}.

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2.3.1. Measurement Method

Λ_c baryons can be reconstructed through their hadronic p-K$^-$-π^+ decay channel (B.R. 5.0 %), despite the very short decay length of cτ = 59.9 μm. By selecting only tracks with a large distance of closest approach to the event primary vertex, DCA_PV, most of the background from primary tracks is rejected. This DCA_PV cut depends on the p_T of the Λ_C and ranges from 40 μm to 80 μm.

To select 3-track combinations coming from primary Λ_C decays, further topological cuts are used: a well reconstructed Λ_C decay vertex (daughter tracks intersect within ~2 sigma) and a Λ_C momentum pointing back to primary vertex. The final cut is on the three-particle invariant mass (2.27 < m$_{inv}$ < 2.30 GeV/c^2).

The possibility of using a resonant intermediate Λ(1520) state has been investigated. A significant improvement of the S/B ratio could be expected. However, a full simulation has not yet been performed. The results shown here are for non-resonant decays.

2.3.2. Simulation Procedure

18000 central Au+Au HIJING events ($\sqrt{s_{NN}}$ = 200 GeV) have been used to estimate the combinatorial background. In order to enhance statistics at high p_T, 10 Λ_C with a flat p_T spectrum have been inserted into each event. The Λ_C were decayed through the p-K$^-$-π^+ channel. The events were simulated with a vertex position of $\pm$ 5cm from the detector center. The detector geometry used for these simulations is described in detail in Reference [1].

In order to rescale the flat distribution, we assumed a power-law shape for the Λ_C spectrum with $\langle p_T \rangle$ = 1.0 GeV/c, and n = 11. The yield estimate (for no Λ_C/D^0 enhancement) assumed a Λ_C/D^0 ratio of 0.2.[13] A dN/dy = 0.002 per binary collision has been used, which is about half the value measured by the STAR Collaboration.[17]

At RHIC-II luminosity, the PIXEL detector will integrate over about 16 minimum bias collisions. For a realistic estimate of pile-up, pseudo-random hits were added to the PIXEL detector layers, corresponding to a minimum bias interaction rate of 80 kHz and a Gaussian primary vertex z-distribution with σ_z = 15 cm. This is an upper limit for pile-up hit densities when running at RHIC-II luminosity.

To estimate the Λ_C signal and background in peripheral collisions, binary scaling, N$_{bin}$, with R$_{CP}$ similar to that of charged hadrons[18] was assumed for the signal and (N$_{part}$)^3 scaling for the background (3-particle combinations). For particle identification (PID) of daughter tracks, the STAR Time of Flight (TOF)[19] performance was assumed to separate pions from kaons for p_T < 1.6 GeV/c and protons from pions and kaons for p_T < 3.0 GeV/c with 90% efficiency.

The Λ_C analysis relies on untriggered data, as there is no obvious trigger. Therefore, large datasets of minimum bias and central events will be needed. With the DAQ1000 upgrade, the STAR data acquisition will be able to reach a sustained DAQ rate of over 500 events per second. With this rate and an estimated 40% accelerator and detector duty

factor, about 500M events will be recorded per month. The results in the next Section are for 250M central and 2B minimum bias events, of which the 500M most central and the 500M peripheral (60-80%) events are used. This makes the Λ_C measurement a goal for the third year of HFT detector operation.

2.3.3.   Results

Figure 3 shows that a secondary decay vertex displaced by cτ = 59.9 μm can be separated from the event primary vertex. Note, that this corresponds to a mean decay length of a Λ_C at mid-rapidity with a transverse momentum of about the Λ_C mass, where the βγ factor is equal to one.

Figure 4 shows the combined acceptance and tracking efficiency for D^0 (red) and Λ_C (blue) in the pseudorapidity interval |η| < 1. We required the daughter tracks to have good hits (not pile-up hits) in the PIXEL detector. Since the Λ_C decays into three daughter particles, its reconstruction efficiency is lower than that of the D^0. Because of large combinatorial background, particle identification information is required for Λ_C daughter tracks. This further limits the detector acceptance (magenta points in Figure 4).
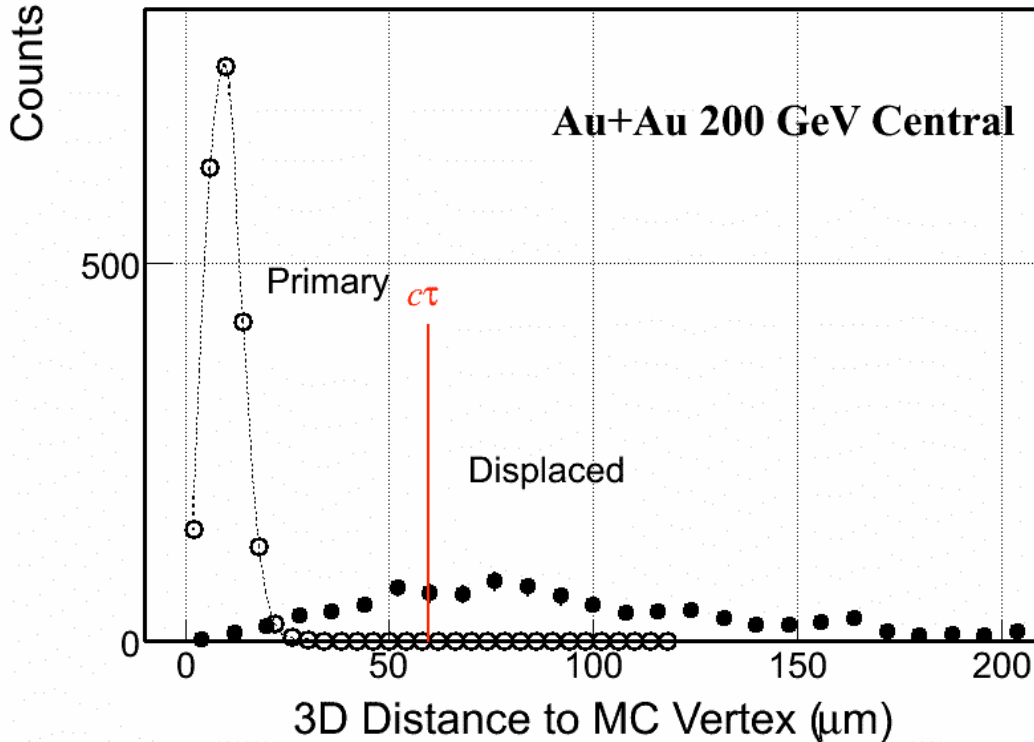
Figure 3: Open circles show the primary vertex resolution in central Au+Au collisions. Solid circles show the Λ_C decay vertex resolution. The mean decay distance, cτ = 59.9 μm for the Λ_C, is shown to guide the eye. Each decay length was scaled by the appropriate ct factor to provide a universal peak for the purpose of illustration.

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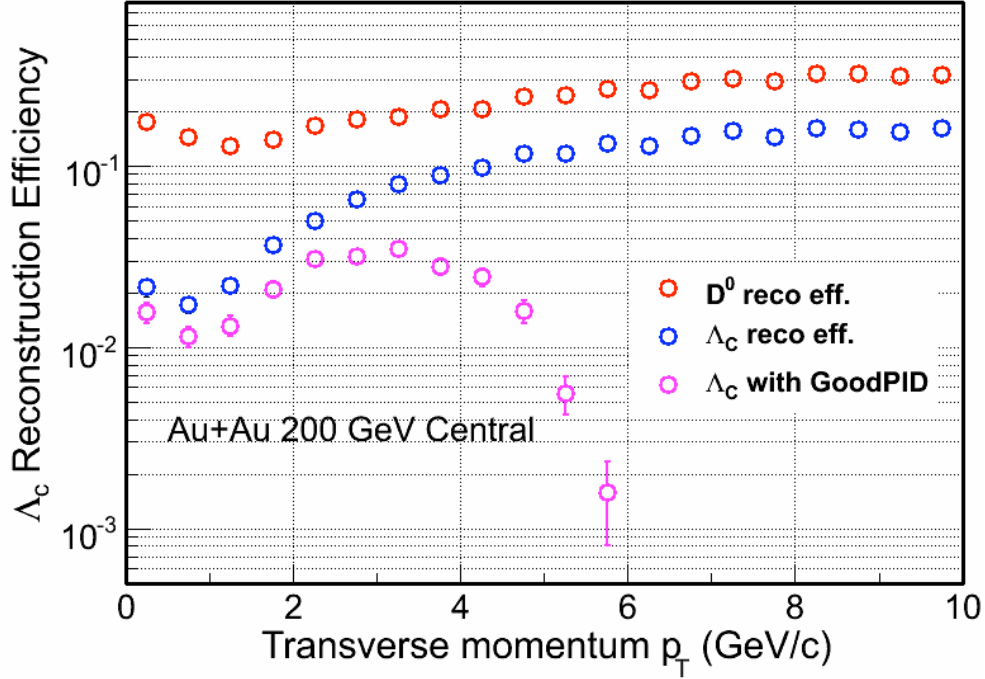
Figure 4: Acceptance and efficiency for Λ_C and D^0 reconstruction.

A topological cut optimization procedure was performed for both central (0-10%) and peripheral (60-80%) collisions, to maximize the signal significance, $S/\sqrt{(S+B)}$. The results are shown in Table 1 and in Table 2.

The estimated invariant mass peak for a 3-4 GeV/c p_T bin is shown in Figure 5. A three-sigma signal has not been achieved for $p_T < 2$ GeV/c. However, for $p_T > 5$ GeV/c, a good significance could be achieved without requiring daughter track PID information. This has not been studied in detail yet.

p_T [GeV/c]	$S/\sqrt{(S+B)}$	$S/(S+B)$	Λ_C produced	Λ_C observed
2-3	4	0.03	23M	507
3-4	8	0.3	7.3M	184
4-5	14	0.9	2.4M	203

Table 1: Signal significance, purity and number of produced and reconstructed Λ_C in 500M central Au+Au collisions (for no Λ_C/D^0 enhancement). Decay branching ratio, acceptance, efficiency and topological cuts are taken into account.

p_T [GeV/c]	$S/\sqrt{(S+B)}$	$S/(S+B)$	Λ_C produced	Λ_C observed
2-3	5	0.9	940k	26
3-4	6	0.9	410k	40
4-5	6	0.9	180k	35

Table 2: Same as Table 1, for 500M peripheral Au+Au collisions.
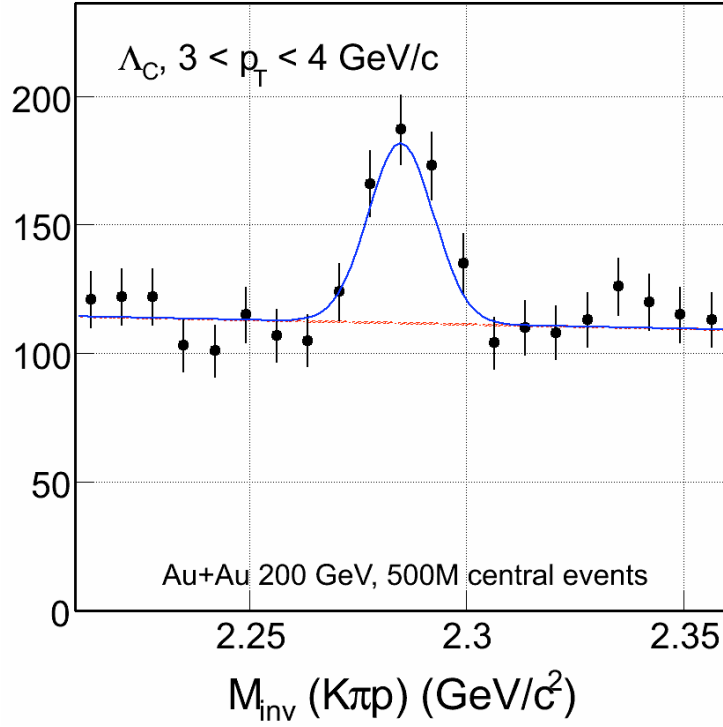
Figure 5: Estimated invariant mass peak for p_T 3-4 GeV/c, in 500M central Au+Au collisions.

Figure 6 shows the estimated statistical errors for the $\Lambda_\mathrm{C}/\mathrm{D}^0$ ratio, for the case where there is no baryon enhancement, i.e. that the ratio is equal to 0.2 and flat in p_T, in black and for the case of the same enhancement as for $\Lambda/\mathrm{K}^0_\mathrm{S}$ in red. Given the D^0 yield and $c\tau$, the errors coming from its measurement are negligible. Statistical errors on $R_\mathrm{CP}(\Lambda_\mathrm{C})/R_\mathrm{CP}(\mathrm{D}^0)$ are dominated by the measurement in peripheral collisions.
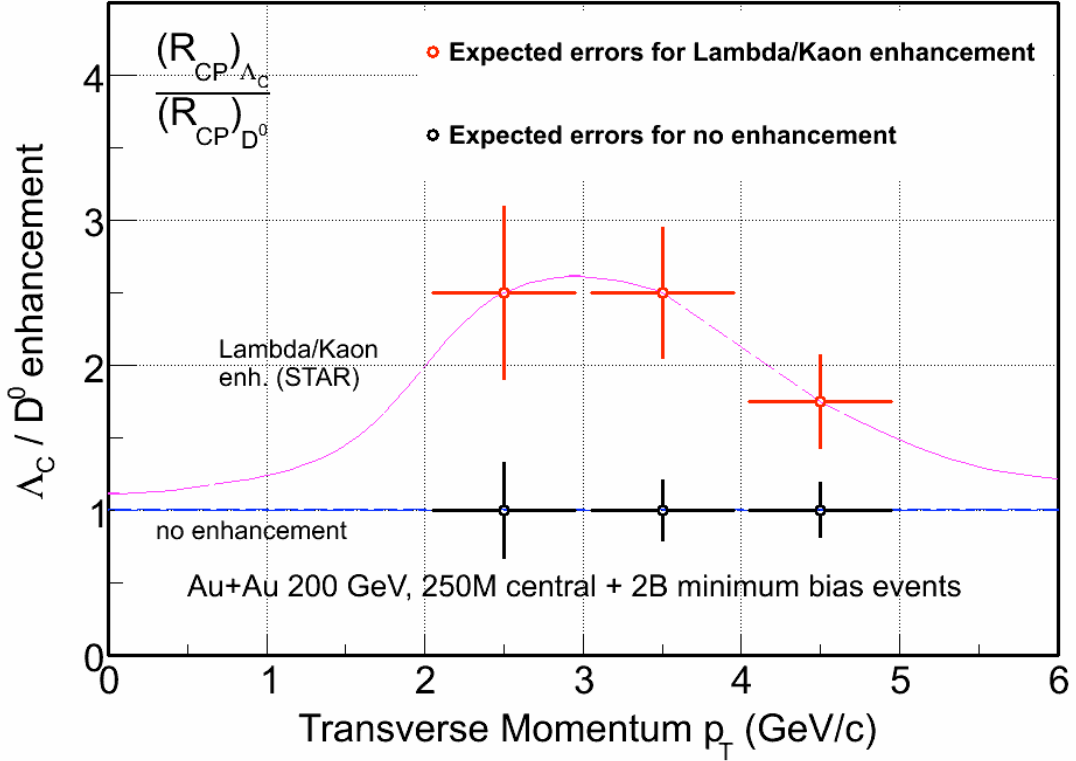
Figure 6: Statistical errors of the Λ_C/D^0 ratio for the case of no enhancement and of Λ/K^0_S-like enhancement.

2.3.4. Summary

The feasibility of Λ_C reconstruction with the HFT has been shown using a Monte Carlo simulation with STAR reconstruction and tracking software. The measurement of the Λ_C/D^0 ratio will allow us to determine if the baryon enhancement seen in the light quark sector will extend to heavy quark hadrons. We expect to improve the significance of this measurement through improved analysis techniques and through extending the analysis to resonant intermediate states.

2.4. B-Mesons

Due to their large mass the bottom and charm quarks are expected to behavior differently from the light quarks in a QGP. As already argued in Section 2.2, it is very important to directly identify bottom and charm mesons. At low transverse momentum the charm contribution is dominant. At a p_T of about 4 GeV/c PYTHIA[20] predicts both contributions to be equal while at higher p_T bottom production is dominant. Independent measurements on bottom quark production would be critical to disentangling different heavy meson production mechanisms and provide crucial information on the medium properties. Also, measurement of bottom meson is important to clarifying the J/ψ production mechanism in the medium. Apart from the primordial production, a

significant fraction of J/ψ comes from the B meson decay. Measurements on B meson production would allow us to subtract the contamination from the B-decay component.

With the current detector configuration, the B contribution to the non-photonic electron spectrum was estimated[21] to be about 50% at $p_T > 5$ GeV/c with large uncertainties. With the HFT, the measurements will dramatically improve. Besides exclusive measurements with large luminosity, B mesons are usually measured using leptons and J/ψ particles through their semi-leptonic decay and J/ψ decay channels, respectively. In the following we explore both possibilities.

2.4.1. Simulation Procedure

In the simulations we used the geometry described in the HFT CD0 proposal.[1] For semi-leptonic decays we generated 3600 HIJING background events for central (b < 3 fm) Au+Au collisions at 200 GeV, with vertex Z between -5 and 5 cm for the best utilization of the pixel layers. For each event we embedded 10 B^+ mesons which were forced to decay only into neutrino, positron and $\overline{D^0}$, and 10 D^+ mesons which were forced to decay into neutrino, positron and $\overline{K^0}$. The B and D mesons were required to have a flat p_T distribution to enhance the statistics at high p_T,. p_T weights were applied later in the analysis to generate spectra. The embedded events then went through the STAR data reconstruction chain to simulate the particle tracking by STAR detectors, and were stored into the standard data files for analysis.

In the simulations of B → J/ψ decay, PYTHIA is used to generate 353.5k direct J/ψ → e^+e^- and 162.1k B → J/ψ → e^+e^- decays in full phase space. Comparison of the acceptance of J/ψ with collision Z_{vertex} at the center of STAR and within ±5 cm shows little difference. We therefore fixed the collision vertex at the STAR center in most of the simulations for simplicity. These J/ψ are then embedded into most central Au+Au collisions generated from HIJING. 20 J/ψ are embedded into one single HIJING event to save computing time. Finally, the events are pushed through the STAR reconstruction chain to simulate realistic detector response. We also included PIXEL detector pile-up effects from expected RHIC-II luminosities.

2.4.2. Measurement through B Semi-leptonic Decays

The simplest measurement of B mesons is by identifying leptons from their semi-leptonic decay. We utilize the impact parameter (d_0) method used by the ALICE collaboration[22] to separate electrons of B decays from those of D decays. Since B mesons have mean proper decay lengths of about 500 μm, their decay electrons are characterized by large impact parameters with respect to the interaction vertex. With the two Pixel layers d_0 will be measured with a resolution of $\sigma_{d0} \sim 20$ μm for $p_T \geq 2$ GeV/c. A cut imposing a minimum value of d_0 rejects a large fraction of the electrons from light meson decays and photon conversions, as well as primary pions misidentified as electrons. The charm contamination can be reduced with a p_T cut, as electrons of B decays have a harder p_T distribution than those of D decays due to the larger mass of the b quark. The UA1

Collaboration has developed a Monte-Carlo method[23] to extract the minimum transverse momentum differential cross section at the B-meson level from the decay-electron p_T differential cross section, assuming that the B-meson decay kinematics is well understood.

We applied the p_T weights so that B/D spectrum and their relative contributions to non-photonic electrons follow the FONLL calculations,[24] and the combined electron sample from B^+ and D^+ decays obeys the measured non-photonic electron spectrum for central (0-5%) Au+Au collisions at 200 GeV.[25] The total tracking efficiency is about 55%, including both the TPC and the HFT pixel layers. Figure 7 presents the simulation results of the impact parameter distributions of electrons from B and D decays, for four p_T bins. In accordance with Ref. [21], the non-photonic electron sample is dominated by the D contribution for $2 < p_T < 3$ GeV/c, and the B contribution increases with p_T.
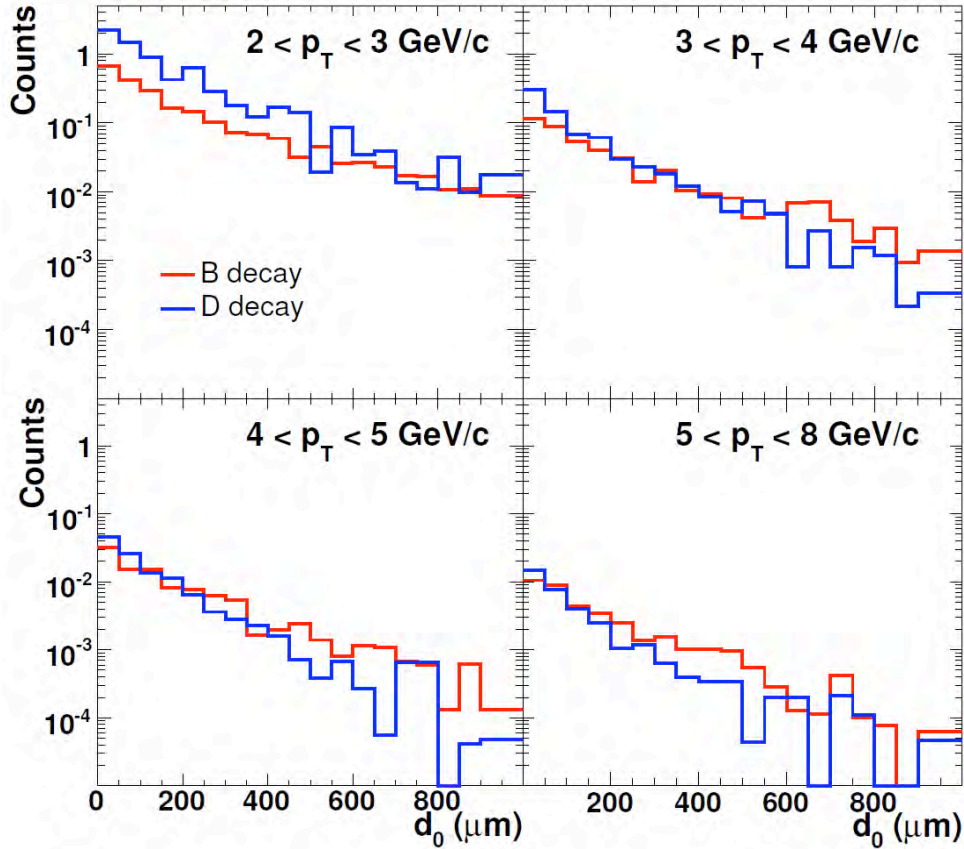
Figure 7: The simulation results of the impact parameter distributions of electrons from B and D decays.

Above 4 GeV/c, there is a d_0 region (200−600 μm) where the B contribution is dominant. We selected electrons within this d_0 region to enhance the B contribution. The electrons satisfying this condition were counted for each p_T bin. The purities of the B-tagged electrons are 25%, 48%, 60% and 69% respectively, from low to high p_T bins, and the yields are 150, 28, 7.5 and 2.5 per million minimum bias central Au+Au events with vertex Z between -5 and 5 cm. The ALICE Collaboration reported the purity of B-tagged

electrons to be 80% for the collisions at LHC with the same method.[26] When we tried our approach with the FONLL B contribution[24] for LHC, we did see a purity of ~80% for p_T > 4 GeV/c. The purity obtained in this approach depends on the relative B/D contribution, which is an input yet to be measured. In the analysis of the real data, we first go through the above simulation procedures without applying the weight for the relative B/D contribution, and leave the simulated d_0 distributions un-normalized for electrons from B and D separately for each p_T bin. The measured d_0 distribution will then be fit with a parameterized combination of the simulated d_0 distributions for electrons from B and D, and the relative B/D contribution will be retrieved as fitting parameter. With the relative B/D contribution measured, we can estimate the purity of B-tagged electrons for different DCA regions and determine the optimal cuts for B reconstruction.

We have estimated the feasibility of the impact parameter method for the proposed STAR HFT detector with the worst case: all the D-decay electrons come from D^+ mesons, whose decay length is ~300 μm. In reality, D^0 and D_s^0 mesons also decay into a substantial portion of D-decay electrons, and the corresponding decay length is only about 100 μm. In the future, we will consider the more realistic case, where the D-decay electrons in the d_0 region (200–600 μm) should be significantly suppressed, and hence, the purity of B-tagged electrons should increase. The yield of B-tagged electrons above 4 GeV/c is 10 per million minimum bias central Au+Au events with vertex Z between -5 and 5 cm. This number was obtained with the assumption of a 100% efficiency of the electron identification, which will be smaller in reality, depending on the detectors involved and the identification approach. However, we can enhance the statistics of high-p_T electrons by applying high-tower triggers using STAR BEMC. When triggering on the track's minimum energy deposition in the BEMC tower, we can almost guarantee one high-p_T electron per event. The electron yield above 4 GeV/c could be enhanced by a possibly large factor.

In summary, identifying B mesons through their semi-leptonic decay is technically feasible and easier than the identification of D mesons. However, rates are marginal when using untriggered data samples. We are studying the possibility to use the existing STAR electron trigger and to develop a high level trigger.

2.4.3.   Measurement through B → J/psi + X Decays

B mesons can also be identified through their decay into J/ψ. Here we utilize the method developed by CDF[27] to calculate the pseudo-cτ of J/ψ and apply a cut to distinguish direct J/ψ from J/ψ from B decay. Figure 8 illustrates how the relevant variables are defined. The pseudo-cτ is defined as $c\tau' = \vec{L} \cdot \frac{p_T^\psi}{|p_T^\psi|} \cdot \frac{M_\psi}{|p_T^\psi|}$, where $\vec{L}$ is the path length between the

J/ψ production point and collision vertex, M_ψ is the J/ψ mass and p_T^ψ is the J/ψ p_T which is required to be larger than 1.25GeV/c. We define DCA as the distance of closest approach between paired electrons. The pseudo-cτ is less than 15% smaller[28] than the actual B meson cτ. In this analysis, the only physical background considered is direct J/ψ production including feed-down contribution from higher mass charmonium states.

Charm continuum and Drell/Yan might have similar level of contribution (see later discussions). The background due to the random combination of electron pairs during the mass reconstruction is removed via subtracting the same sign electron pairs when analyzing mass and pseudo-cτ distributions. The signal is a mixture of $B^{\pm}$ and B^0 mesons with a 1.094% branching ratio for the decay to J/ψ.[29]
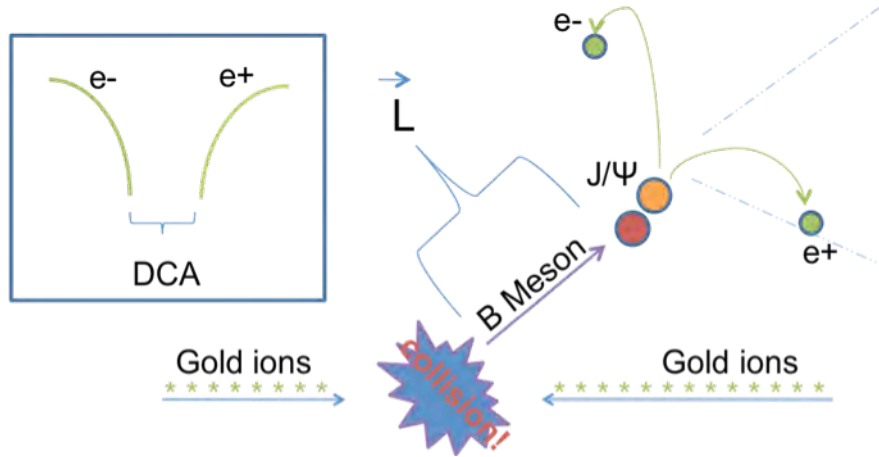
Figure 8: Definition of variables used in the analysis. See text for details.

The goal of this analysis is to obtain the S/B ratio and efficiency as a function of pseudo-cτ cut in most central Au+Au collisions with the addition of PIXEL detector pile-up effects at RHIC-II luminosities.

The J/ψ signal is obtained by subtracting the mass spectrum of like-sign electron pairs from the unlike-sign electron pair mass spectrum within a mass window between 2.8GeV/c^2 and 3.2GeV/c^2. Figure 9 shows the mass distribution for unlike-sign and like-sign pairs in a p+p and Au+Au collisions where perfect electron identification is assumed. The like-sign mass spectrum represents the combinatoric background very well. The track quality cuts require $N_{fit}>20$ and $N_{fit}/N_{max}> 0.5$, where N_{fit} and N_{max} are the number of fit points and maximum number of possible registered points for the reconstructed track.
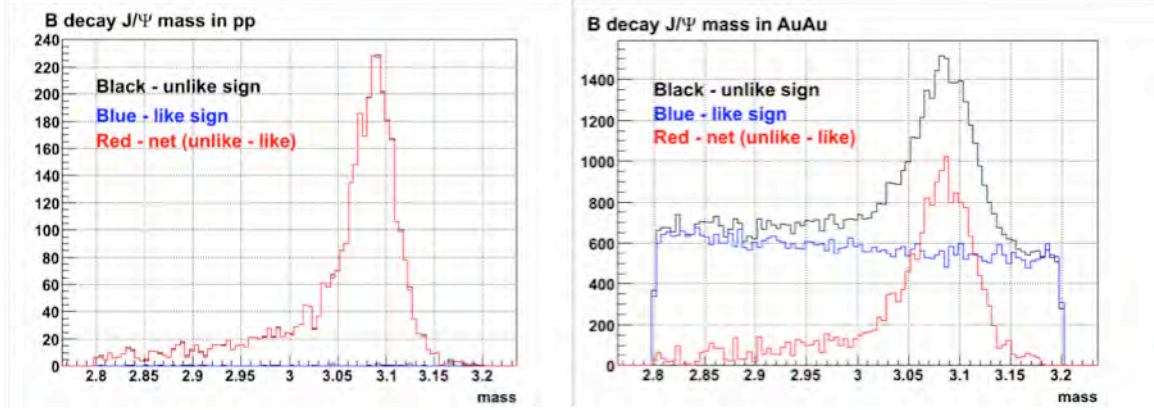
Figure 9: J/ψ mass distribution in p+p collisions (left) and central Au+Au collisions (right). Black and blue histograms represent unlike and like-sign electron pairs, respectively. The red histograms are obtained after subtracting like-sign spectrum from unlike-sign spectrum. Note that 20 J/ψ−>ee are embedded into one Au+Au collision, therefore the S/B in the mass distribution does not reflect the actual value in real data.

Figure 10 shows the pseudo-cτ distribution for B-decay and direct J/ψ in most central Au+Au collisions with and without PIXEL pile-up effects. We used the normalization from p+p collisions. The FONLL calculation[24] predicts the total $b\bar{b}$ cross section in p+p collisions at RHIC to be 1.87 μb leading to 3.74 μb for B meson production. Measurements from PHENIX p+p collisions show that the total direct J/ψ → e⁺e⁻ production is about 178 nb. Taking into account the B → J/ψ → e⁺e⁻ branching ratio, we obtained a yield ratio of direct J/ψ over B-decay J/ψ is of 65. The tail from the track and PIXEL hit mis-association is the major background for B mesons. This background becomes larger when pile-up effects are added. The B-decay J/ψ distribution contains a long tail in the positive pseudo-cτ due to the long B meson life time, a sharp Gaussian tail on the negative region due to tracking resolution and a tail due to the wrong association of tracks and PIXEL hits as in the case of direct J/ψ.
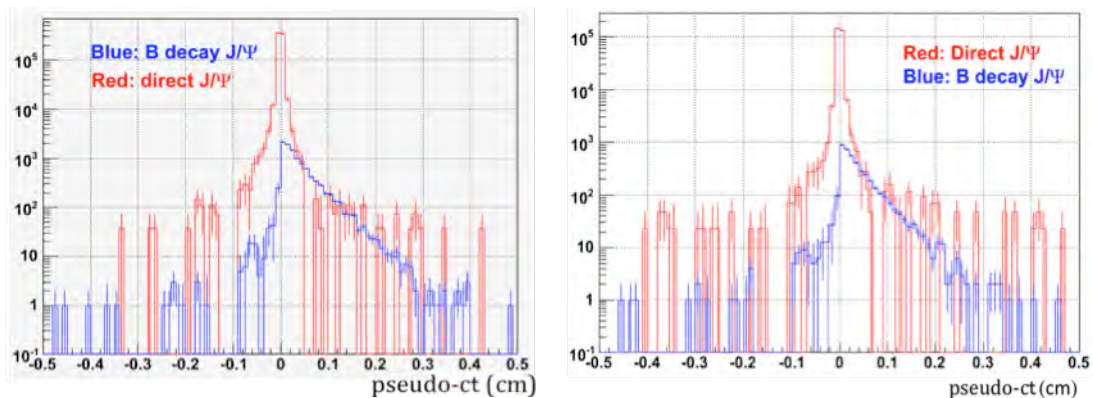
Figure 10: Pseudo-cτ distributions for direct and B-decay J/ψ in central Au+Au collisions before (left panel) and after (right panel) including PIXEL detector pile-up effect in 1× RHIC-II luminosity. The red and blue histograms are from direct and B-decay J/ψ, respectively.

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Figure 11 shows the S/B ratio and efficiency in measuring B meson as a function of cut on pseudo-cτ. The pile-up effects increase when the cut increases. This is because the pileup hits on PIXEL detector enhance the probability of track and PIXEL hit mis-association which is the source for the non-Gaussian tail in the pseudo-cτ distribution. The S/B ratio reaches a maximum of about 2 at a pseudo-cτ cut at 500 μm where the efficiency for B-decay J/ψ is about 30%. Notice that these results do not include any nuclear or QGP effects for J/ψ and B meson production. As we know from the PHENIX measurement,[30] J/ψ production at mid-rapidity is suppressed by a factor of three in most central Au+Au collisions. If B mesons are much less suppressed, the S/B ratio can increase significantly. In the real data analysis, one way to measure the B → J/ψ yield is to obtain, for example, the background p_T shape by applying a very small pseudo-cτ cut and later a large cut to obtain the B-decay J/ψ p_T shape using the background shape as a reference.
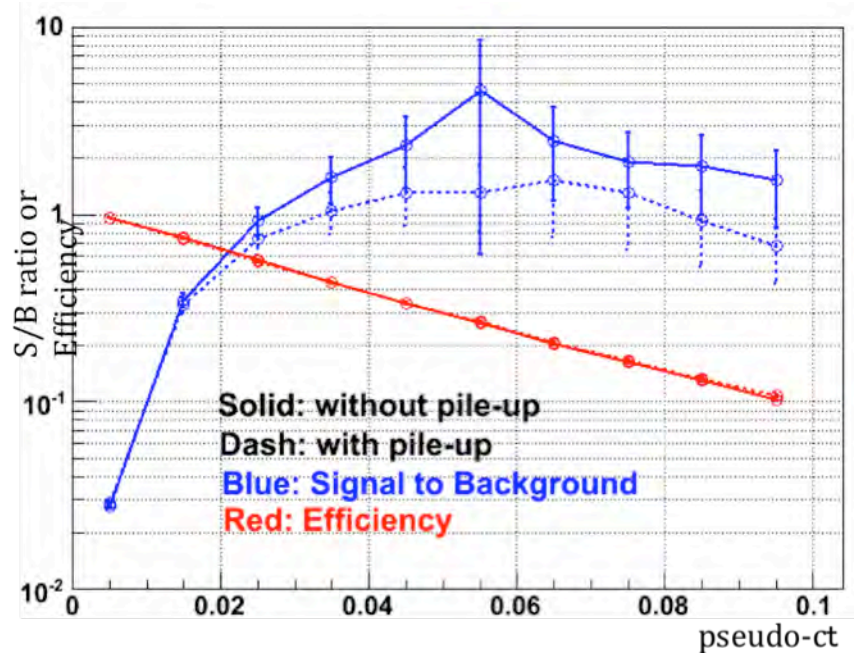
Figure 11: S/B ratio and efficiency as a function of pseudo-ct cut for B → J/ψ measurements in central Au+Au collisions. The dashed curves represent result including PIXEL pile-up effect in 1× RHIC-II luminosity. The red curves are efficiency and blue curves are S/B ratio. The error bars are statistical only.

We also studied the effect of PIXEL detector position resolution on the measurements. Figure 12 presents the results when PIXEL detector resolution is changed from 8 μm to 80 μm without including the pile-up effect. We changed the electron pair DCA cut from 50 μm to 200 μm to keep the efficiency unchanged. The left panel shows pseudo-cτ distributions for direct and B-decay J/ψ. Compared to the results in the left panel of Figure 10, the distribution for direct J/ψ becomes wider due to the worse resolution while the effect on B-decay J/ψ is not that obvious due to the much larger B meson cτ. The widened direct J/ψ distribution leads to five to ten times smaller S/B which is shown in

the right panel of the figure. The HFT PIXEL detector resolution is critical for this measurement.
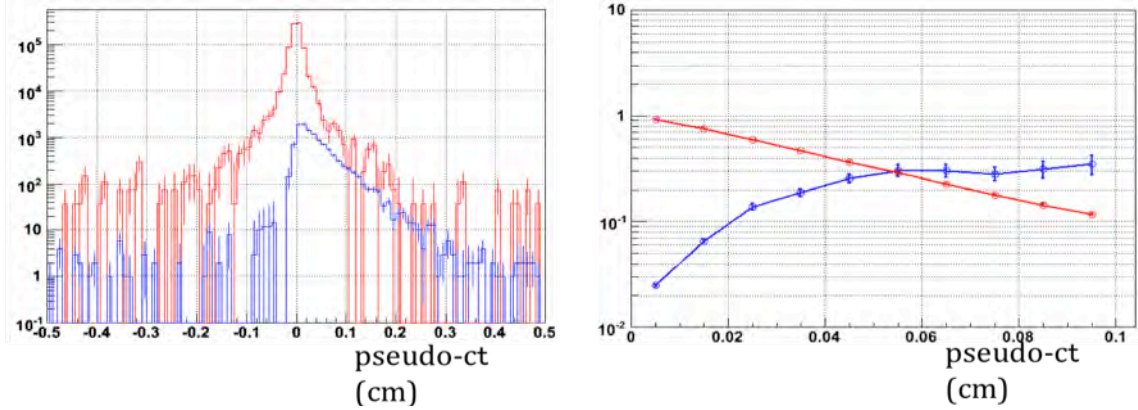
Figure 12: Results after changing the PIXEL detector position resolution from 8 μm to 80 μm; Left panel is pseudo-cτ distribution for direct J/ψ (red) and B-decay J/ψ (blue); right panel is the S/B (blue) and efficiency (red) as a function of pseudo-cτ cut.

A possible way to improve the S/B is to apply the cut on the distance of closest approach to a third charged particle (DCA3) pointing to the reconstructed J/ψ production point. A large fraction of particles from B → J/ψ + X are charged. In the large cτ region, ideally after applying a small DCA3 cut, most of the direct J/ψ which come from the collision point are expected to be rejected while a large fraction of B-decay J/ψ should be kept. It turns out that a small DCA3 cut can't improve the S/B ratio. When no pseudo-ct cut is applied, the direct J/ψ DCA3 distribution is much narrower than the B-decay J/ψ since at collision vertex thousands of charged particles can be used as a third particle to reconstruct DCA3 and it is very likely for a randomly associated third particle to be closer than the reconstructed position of the actual third partner. When the pseudo-cτ cut is larger, this probability becomes smaller and the distribution becomes wider. In the large ct region the results for direct and B-decay J/ψ become very similar. Therefore, cutting on DCA3 can't improve the S/B ratio. However, applying a large DCA3 cut (for example DCA3 > 20 μm) will enhance the S/B especially when a small pseudo-cτ cut is applied. Figure 13 shows the results after this cut without including the pile-up effect. The DCA3 cut dramatically improves the S/B ratio in the small pseudo-cτ cut region but has little effect in the large pseudo-cτ region. At the same time, the B-decay J/ψ suffers significant efficiency loss. It is not obvious, which method delivers the better result, but the two analyses methods can be used to cross check each other and to understand systematic uncertainties.
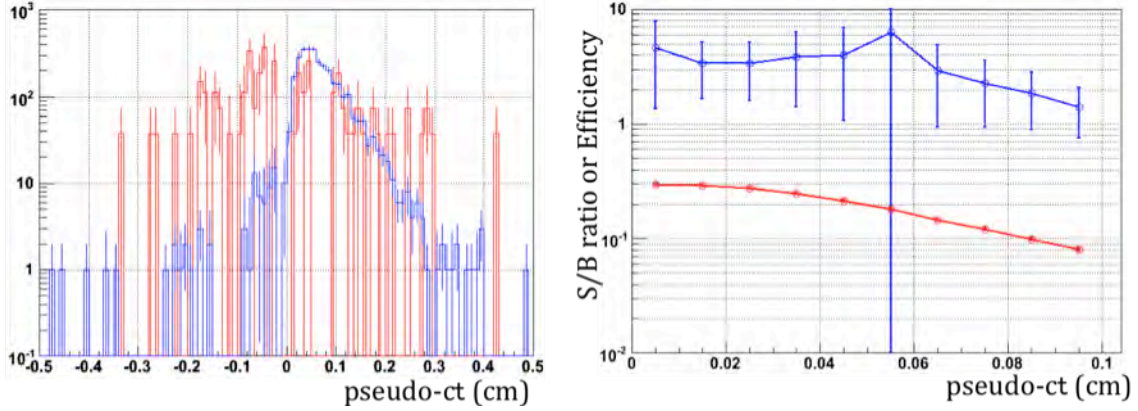
Figure 13: Results after applying the DCA3 cut; Left panel is pseudo-cτ distribution for direct J/ψ (red) and B-decay J/ψ (blue); right panel is the S/B (blue) and efficiency (red) as a function of pseudo-cτ cut.

We also confirmed that our results are consistent with the CDF measurements on B → J/ψ.

The number of B-decay J/ψ recorded in STAR during each RHIC-II week without including the trigger efficiency is:

$$N(B \to J/\psi) = \sigma(B) \cdot BR(B \to J/\psi) \cdot BR(J/\psi \to e^+e^-) \cdot AccpEff(recon)$$
$$\cdot eff(p_T \ cut) \cdot eff(c\tau \ cut) \cdot eff(analysis \ cut) \cdot dutyFactor$$
$$\cdot luminosity(RHIC - II)$$

where $\sigma(B)$ is the B meson cross section; $BR(B \to J/\psi)$ and $BR(J/\psi \to e^+e^-)$ are branching ratios for each of the decay channels; $AccpEff(recon)$ is the product of J/ψ acceptance and reconstruction efficiency in full phase space; $eff(p_T \ cut)$ is the efficiency due to the $p_T > 1.25$ GeV cut; $eff(c\tau \ cut)$ is the efficiency due to pseudo-cτ cut; $eff(analysis \ cut)$ is the efficiency for all the analysis cuts including track quality, electron pair DCA and J/ψ mass window, etc; $dutyFactor$ is the expected STAR duty factor during the run; $luminosity(RHIC - II)$ is the expected delivered luminosity in a 12-week RHIC-II run in 2013.[31]

The total number of B → J/ψ → e⁺e⁻ per RHIC-II 12-week run recorded at STAR *assuming 100% trigger efficiency* and neglecting TPC pile-up effect in high collision rates:

- In p+p collisions,
  - Maximum: 2858±93 J/ψ at $p_T \geq 1.25$ GeV/c
  - Minimum: 365±33 J/ψ at $p_T \geq 1.25$ GeV/c
- In Au+Au collisions
  - Maximum: 4066±486 J/ψ at $p_T \geq 1.25$ GeV/c
  - Minimum: 706±202 J/ψ at $p_T \geq 1.25$ GeV/c

Based on these numbers, we then calculated the number of J/ψ recorded at |Z vertex| < 5 cm by multiplying the efficiency (13.2%) of the vertex cut estimated from a Gaussian distribution with σ = 30 cm and *assuming 100% trigger efficiency:*.

- In p+p collisions
  - Maximum: 2084±79 J/ψ at $p_T \geq 1.25$ GeV/c.
  - Minimum: 266±28 J/ψ at $p_T \geq 1.25$ GeV/c.
- In Au+Au collisions
  - Maximum: 2926±412 J/ψ at $p_T \geq 1.25$ GeV/c
  - Minimum: 508±172 J/ψ at $p_T \geq 1.25$ GeV/c.

Therefore, about 70% of the observed J/ψ are from $|Z_{vertex}|$<5cm due to the configuration of the PIXEL detector.

However, the J/ψ trigger performance in STAR will have to be significantly improved to make it possible to measure B → J/ψ. In p+p collisions, the current J/ψ trigger efficiency based on an estimate from the 2006 p+p run is only about 10% at p_T(J/ψ) > 6 GeV/c. If the trigger performance persist at RHIC-II, the maximum number of observed B → J/ψ → ee per 12-week run is ~2858*10%*3% = 9, where 3% is the fraction of J/ψ at p_T > 6 GeV/c relative to the number of J/ψ at p_T > 1.25 GeV/c. This means the B → J/ψ → ee channel cannot be used to measure B mesons without improved trigger. In Au+Au collisions, the expected collision rate is ~50 kHz. Considering the 1 kHz STAR DAQ bandwidth, we will also need a very good J/ψ trigger to carry on this measurement. With the TOF and DAQ1000 upgrade, the J/ψ trigger is expected to be significantly improved. New studies are needed to estimate the improvement. One the other hand, when the Muon Telescope Detector (MTD) upgrade is accomplished, we can study B mesons using the B → J/ψ → $\mu^+\mu^-$ channel with a high performance MTD trigger with a very high rejection power.

3. Functional Requirements

3.1. General Design Considerations

STAR is a large acceptance experiment with full azimuthal coverage at mid-rapidity in the pseudo-rapidity range |η| < 1. With the TPC as a central detector and a current read-out speed of about 100 Hz STAR is considered to be a "slow" detector as far as single particle observables are concerned. Even after the DAQ upgrade to 1000 Hz in 2009 the read-out speed will be limiting the single particle capabilities of STAR. The real strength of STAR, good particle identification and full azimuthal coverage, come into play when correlations or multi-particle final states are studied. Good particle identification and full azimuthal coverage have been the bases for the enormous success of the STAR physics program.

It is obvious that when it comes to identifying rare processes, like heavy flavor production with multi-particle final states, full azimuthal coverage will be of utmost importance. Thus, full azimuthal coverage is a prime design requirement for the HFT.

Another important requirement is to keep a very low overall material budget in order to limit the effects of multiple scattering and of conversions. Our goal is to overall reduce the radiation length of the inner tracking and support system compared to the status when the SVT was the STAR inner tracking detector.

The performance requirements listed below are selected so that if those requirements are met by the detector, the detector will be able to achieve the physics requirements. Fulfillment of the performance requirements can be completely determined shortly after the installation of the HFT.

3.2. Pointing Resolution

Heavy flavor hadrons have extremely short life times ($c\tau \sim 50$ μm). Identifying such a short displaced vertex requires extremely good pointing resolution. This is especially important for the identification of low transverse momentum decays where small gains in pointing resolution lead to large gains in detection efficiency. The pointing resolution in $r\varphi$ and in z-direction are shown in Figure 14 as a function of p_T.
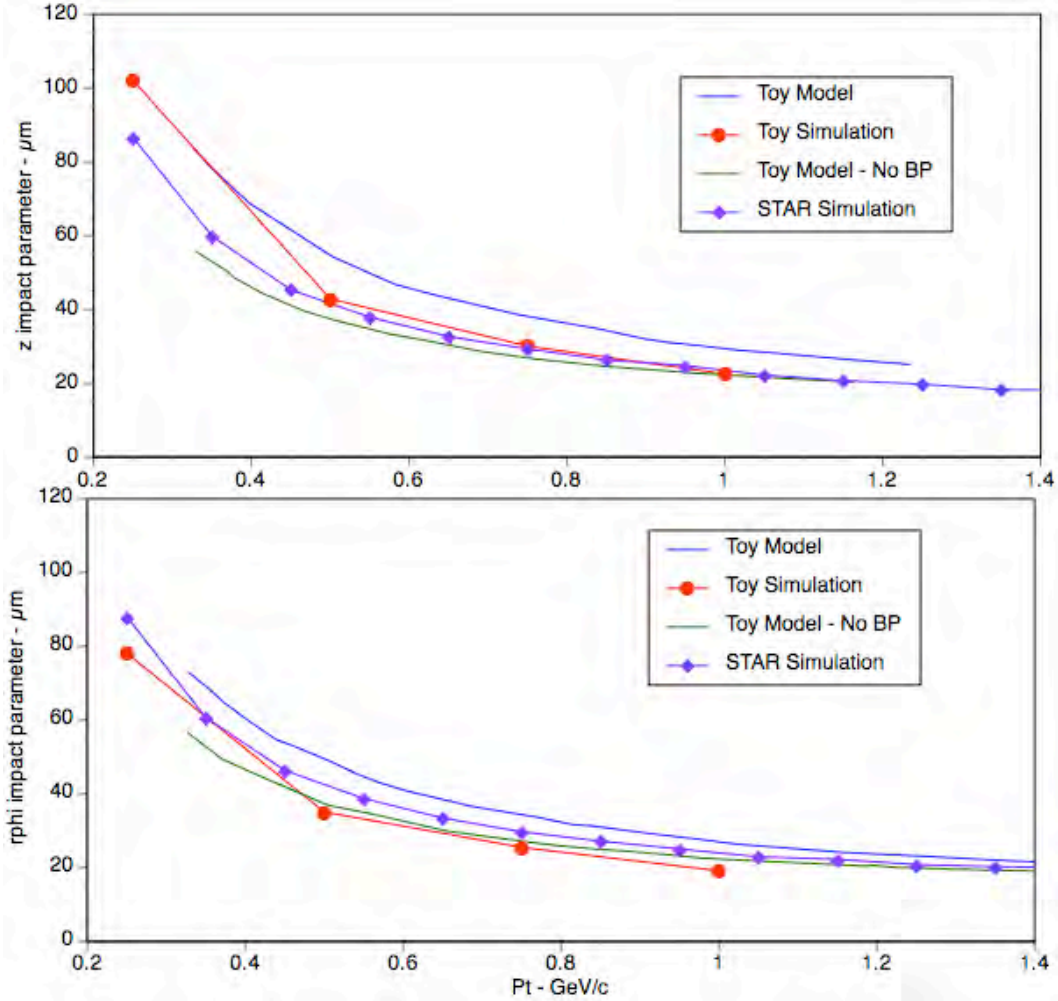
Figure 14: Comparison of three different types of simulations to determine the pointing resolution in rφ and in the z-direction at the vertex. The three methods are the Toy Model, a Toy Simulation, and the full STAR Simulation. Each method has different assumptions and slightly different parameters but overall, the agreement is good. In the figure's legend, BP is short hand for "beam pipe". From Reference [1].

We require a pointing resolution of better than 50 μm for kaons of 750 MeV/c. 750 MeV/c is the mean momentum of the decay kaonskanos from D mesons of 1 GeV/c transverse momentum, the peak of the D meson distribution.

The pointing resolution that will be achieved by the HFT can be calculated from the design parameters.

3.3. Multiple Scattering in the Inner Layers

The precision with which we can point to the interaction vertex is determined by the position resolution of the pixel detector layers and by the effects of multiple scattering in the material the particles have to traverse. The beam pipe and the first pixel layer are the

two elements that have the most adverse effect on pointing resolution. Therefore, it is crucial to make those layers as thin as possible and to build them as close as possible to the interaction point.

We have chosen a radius of 2 cm for a new beam pipe. Making this radius even smaller would make the STAR beam pipe the limiting aperture of the RHIC ring. This is not a desirable situation. The central section of the beam pipe will be fabricated from Beryllium. Such a beam pipe can have a minimal wall thickness of 500 μm, equivalent to 0.xx % of a radiation length.

The two pixel layers will be at a radius of 2.5 cm and 8 cm, respectively. The sensors will be thinned down to 50 μm and the ladders will be fabricated in ultra-light carbon fibre technology. The total thickness of the beam pipe and the fist pixel layer will be the equivalent of 0.xx % of a radiation length. With those parameters, the contributions to the pointing resolution from multiple scattering and from detector resolution will be about equal.

The radiation lengths of the two innermost structures, the beam pipe and the first pixel layer, are design parameters.

3.4.   Internal Alignment and Stability

The Pixel and the IST positions need to be known and need to be stable over a long time period in order not to have a negativean effect on the pointing resolution. The quality of the data will depend on alignment and long term stability. This is especially important for the Pixel detector that needs to be installed and removed on a short time scale.

The alignment and stability need to be better than 300 μm for the IST and better than 20 μm for the Pixel.

Those parameters can be determined from a survey.

3.5.   Pixel Integration Time

Compared to the strip detectors, the Pixel is a slow device with a long integration time. All events that occur during the integration or life time of the Pixel will be recorded. This makes assigning Pixel hits to a particular track in the TPC a difficult pattern recognition problem.

From detailed simulations we have concluded that at RHIC II luminosities the detection and reconstruction efficiency for D-mesons is not appreciably degraded due to multiple events and tracks in the Pixel if the integration time of the detector is smaller than 200 μs.

The Pixel integration time is a design parameter.

3.6.   Read-out Speed and Dead Time

In the absence of a good trigger for D-mesons it is imperative for the measurement of rare processes to record as many events as possible and as required by the physics processes. In STAR the speed of the DAQ is the limiting factor for the number of events recorded.

In order not to slow down the STAR DAQ, the HFT read-out speed needs to be compatible with the STAR DAQ speed and the HFT needs to be dead time free.

Read-out speed and dead time are design parameters.

3.7.   Detector Hit Efficiency

The hit efficiency of the Pixel and IST detectors is essential for good detection efficiency. In the case of secondary decay reconstruction, the hit inefficiency of each detector layer enters with the power of the number of reconstructed decay particles into the total inefficiency.

In order to keep inefficiency low, we request that each individual detector layer has a hit efficiency of better than 95%.

The hit efficiency of each detector layer can be measured on the bench before installation.

3.8.   Life Channels

Dead channels in the Pixel and IST will cause missing hits on tracks and thus lead to inefficiencies in the reconstruction of decay tracks. Therefore, the number of dead channels needs to be as low as possible.

The impact of dead channels on the overall performance will be minimal if more than 97% of all channels are alive at any time.

The number of dead channels can be determined immediately after installation of the detectors.

4.　Technical Design

4.1.　Requirements and Detector Design

The HFT will extend the STAR physics capabilities to the identification of short-lived particles containing heavy quarks through reconstruction and identification of the displaced vertex at mid-rapidity. STAR has 2π azimuthal coverage and to match this, the HFT is required to have 2π azimuthal coverage.

In order to identify short displaced vertices the HFT is required to have excellent pointing resolution of the order of 50 µm. Good pointing resolution is achieved by a two-layer high-resolution vertex detector close to the interaction vertex. In the high-multiplicity environment of heavy ion collisions, the HFT also needs to provide excellent tracking resolution in order to connect tracks identified in the TPC with the corresponding hits in the vertex detector. The resolution of the TPC is not good enough to assign hits in the vertex detector to identified particles with high efficiency. Thus the HFT needs to provide intermediate tracking in the region between the TPC and the vertex detector. We also require redundancy in this design.
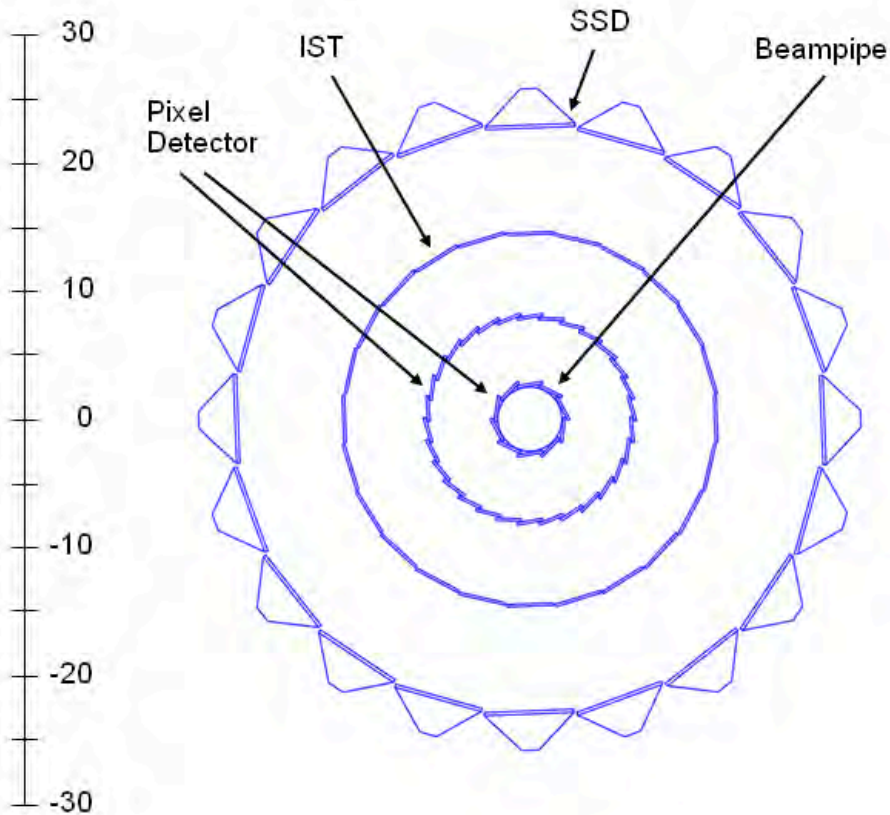
Figure 15: A schematic view of the Si detectors that surround the beam pipe. The SSD is an existing detector and it is the outmost detector shown in the diagram. The IST lies inside the SSD and the PIXEL lies closest to the beam pipe.

These requirements lead to the HFT design of 4 layers of silicon detectors distributed in radius between the interaction point and the TPC. Figure 15 shows the radial distribution of the four layers. The inner two layers, the PIXEL, lay at 2.5 and 8 cm, the IST lays at 14 cm and the SSD at 23 cm. A schematic view of the different HFT layers between the beam pipe and the inner field cage of the TPC is shown in Figure 16.
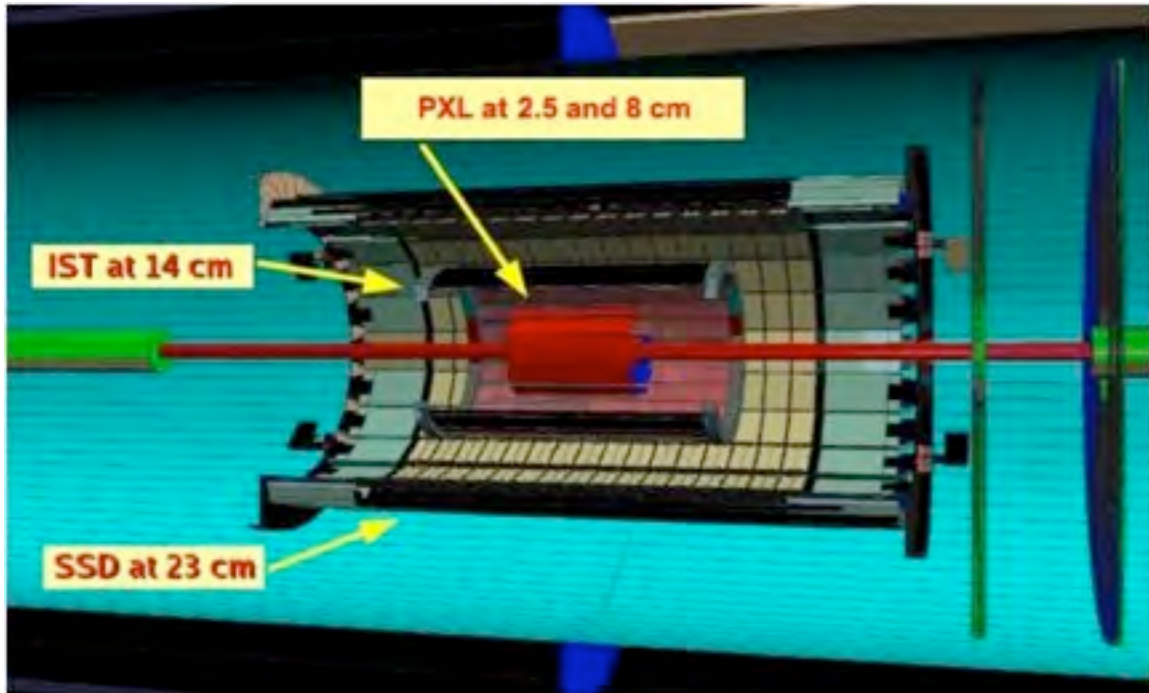
Figure 16: Schematic view of the different layers of the HFT.

The pointing resolution that can be achieved with a given system has two components, a contribution from detector resolution and a contribution from the effects of multiple scattering. Multiple scattering can be minimized by using low radiation length material, in particular between the interaction point and the second layer of detectors. The HFT requirements are that the PIXEL and the beam pipe be as thin as technically possible and that the first detector layer be as close to the interaction point as technically feasible.

In order to meet those requirements, STAR needs a new beryllium beam pipe with a radius of 2 cm. The integrated radiation length from the interaction point to the outside of the PIXEL detector is 0.75 % of a radiation length. The total radiation length of the HFT including beam pipe and mounting structure is x % of a radiation length.

Table 3 gives an overview of the pointing resolution at intermediate points along the path of a 750 MeV kaon as it travels from the TPC to the vertex. Good graded resolution at the intermediate points is necessary to resolve ambiguous hits on the next layer of the tracking system with high efficiency.

Graded Resolution from the Outside - In		Resolution(σ)
TPC pointing at the SSD	(23 cm radius)	~ 1 mm
SSD pointing at IST	(14 cm radius)	~ 400 μm
IST pointing at PIXEL-2	(8 cm radius)	~ 400 μm
PIXEL-2 pointing at PIXEL-1	(2.5 cm radius)	~ 125 μm
PIXEL-1 pointing at the vertex		~ 40 μm

Table 3: Pointing resolution of the TPC and HFT detectors at intermediate points along the path of a 750 MeV kaon as it is tracked from the outside – in. Good resolution at the intermediate points is needed to resolve ambiguous hits on the next layer of the tracking system.

Good pointing resolution can overall only be achieved if the individual detectors guarantee a long-term mechanical stability and reproducibility that is of the order of the resolution for the detector. Those numbers for the subsystems of the HFT are:

- PIXEL   20 μm
- IST   300 μm
- SSD   300 μm

An important requirement is that the HFT be able to be read with a frequency that is compatible with STAR DAQ, i. e. 1000 Hz. All sub-detectors are read out individually and their readout needs to fulfill this condition. The IST and the SSD are fast detectors and achieving this is trivial. However, the existing readout chain for the SSD is designed for a slower readout speed and thus needs to be redesigned and built to fulfill the readout specification. The sensors of the PIXEL detector on the other hand have a slow readout time of the order of 100 μs. The individual pixels are always life and the sensors keep a memory of all tracks that pass during one readout cycle. This leads to pile-up of tracks that do not belong to a triggered event. Pile-up is unavoidable in this technique. With extensive simulations we have shown that even at RHIC II luminosities the effects of pile-up are minimal if the readout time of the PIXEL sensors is smaller than 200 μs. This leads to the requirement that the readout time of the PIXEL sensors be smaller than 200 μs.

The first pixel layer of the HFT lies very close to the interaction vertex in a very high radiation field. The pixel sensors will be built in a technology that is not radiation hard. We require that the innermost sensors can operate during an entire RHIC year at highest RHIC II luminosities without a noticeable drop in efficiency. The location close to the beam is also prone to potentially catastrophic failure of the silicon in case of unintended and uncontrolled excursions of the beam from its nominal orbit. For the case of catastrophic failure or diminished efficiency due to high radiation, we want to be able to replace the PIXEL detector with a new, fully functioning copy of the detector. We require that the PIXEL detector can be exchanged within one day.

Calibration of a micro-vertex detector is very elaborate and time-consuming. The concept of replacing a detector within the short time span required for the HFT can only work, if the new detector is calibrated internally on the bench and if this calibration can

be transferred to the inserted detector. This is a very important requirement for the PIXEL sub-detector.

The HFT needs to operate under RHIC II conditions and luminosities. The outer layers (IST, SSD) are required to operate for 10 years in this radiation field without depreciation of performance in terms of efficiency. The pixel layers of the HFT are retractable and can be replaced in case of damage. The PIXEL layers need to operate for one year under highest RIC II luminosities without appreciable deterioration of the detection efficiency.

4.2. Pixel

Here a short introduction with all the right numbers

The PIXEL detector is a low mass detector that will be located very close to the beam pipe. It will be built with two layers of silicon pixel detectors: one layer at 2.5 cm average radius and the other at 8.0 cm average radius. The outer layer will have 30 ladders and the inner layer will have 10 ladders; for a total of 40. Each ladder contains a row of 10 monolithic CMOS detector chips and each ladder has an active area of ~19.2 cm × ~1.92 cm. The CMOS chips contain a ~1000 × ~1000 array of 18.4 μm square pixels and will be thinned down to a thickness of 50 μm to minimize Multiple Coulomb Scattering (MCS) in the detector. The effective thickness of each ladder is 0.37% of a radiation length.

The relevant performance parameters for the Pixel detector are shown in Table 4.

Pointing resolution	(13 ⊕ 22GeV/p·c) μm
Layers	Layer 1 at 2.5 cm radius Layer 2 at 8 cm radius
Pixel size	18.4 μm ✕ 18.4 μm
Hit resolution	10 μm rms
Position stability	6 μm (20 μm envelope)
Radiation thickness per layer	X/X0 = 0.37%
Number of pixels	~436 M
Integration time (affects pileup)	0.2 ms
Radiation tolerance	300 kRad
Rapid installation and replacement to cover rad damage and other detector failure	Installation and reproducible positioning in a shift

Table 4: Performance parameters for the pixel detector.

4.2.1. Sensors and Readout

Development and Deployment Plan

We intend to approach the completion of the Pixel detector for STAR as a two stage development process with the readout system requirements tied to the stages of sensor development effort. The sensor development is taking place at the Institut Pluridisciplinaire Hubert Curien (IPHC) in Strasbourg, France where we are working in collaboration with Marc Winter's group. In the current development path, the first set of prototype sensors to be used at STAR will have digital outputs and a 640 μs integration time. We will use these sensor prototypes to construct a limited prototype detector system for deployment at the STAR detector during the summer of 2010. This prototype system will employ the mechanical design to be used for the final Pixel detector as well as a readout system that is designed to be a prototype for the expected final readout system to be deployed with the final Pixel sensors in a complete detector in the 2012 time frame.

Monolithic Active Pixel Sensor (MAPS) Development at IPHC

The sensor development path for the Pixel detector sensors is tailored to follow the development path of the technology as it was set by the IPHC group. In this path, MAPS sensors with multiplexed serial analog outputs in a rolling shutter configuration are

envisioned as the first generation of sensors followed by a more advanced final or ultimate sensor that had a digital output(s). The analog MAPS have been produced and tested and our sensor development path moves to digital binary readout from MAPS with fine grained threshold discrimination, on chip correlated double sampling (CDS) and a fast serial LVDS readout. A diagram showing the current development path and with the attendant evolution of the processing and readout requirements is shown in Figure 17.
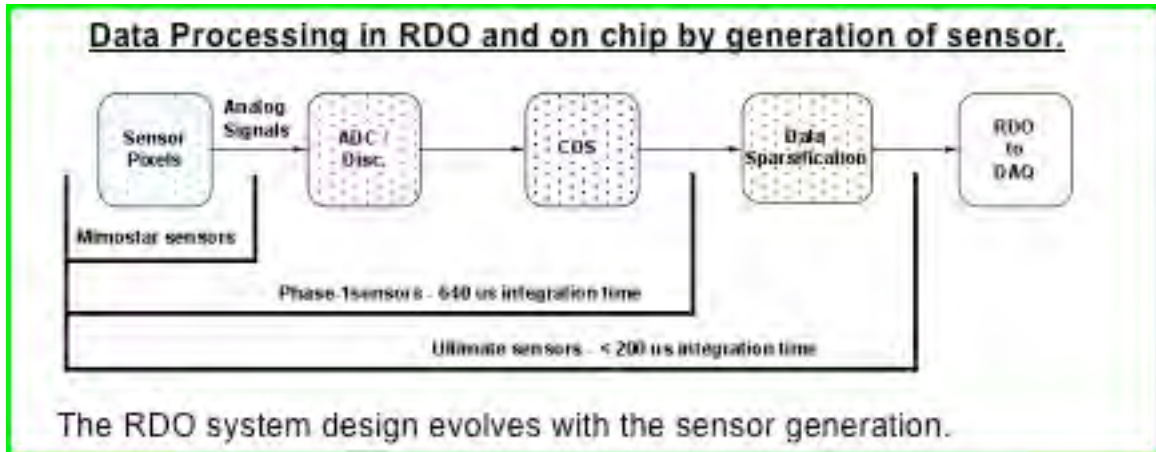
Figure 17: Diagram showing the sensor development path of sensors for the STAR Pixel detector at IPHC in Strasbourg, France. The readout data processing required is shown as a function of sensor generation. The first generation Mimostar sensors are read out via a rolling shutter type analog output. The next generation Phase-1 sensor integrates CDS and a column level discriminator to give a rolling shutter binary readout with a 640 μs integration time. The final generation Ultimate sensor integrates data sparsification and lowers the readout time to < 200 μs.

The Mimostar series sensors are the generation of sensors that have been fabricated and tested. These are 50 MHz multiplexed analog readout sensors with 30μm × 30μm pixels in variously sized arrays depending on generation. This generation has been tested and characterized and, with the exception of some yield issues, appears to be well understood. Testing with these sensors is well described in a NIM paper reference.

The next generation is named "Phase-1". This sensor will be based on the Mimosa-8 and Mimosa-16 sensors and will contain on-chip correlated double sampling and column level discriminators providing digital outputs in a rolling shutter configuration. The Phase-1 will be a full sized 640 × 640 array resulting in a full 2 cm × 2 cm sensor size. In order to achieve a 640 μs integration time, the Phase-1 sensor will be equipped with four LVDS outputs running at 160 MHz. The first delivery of wafers of this sensor design is expected in late 2008.

The final sensor is named "Ultimate". The Ultimate sensor includes all of the attributes of the Phase-1 sensor with the pixel sub-arrays clocked faster to give a <200 μs integration time and the integration of a run length encoding based data sparsification and zero suppression circuit. The pixel size has been reduced to 18.4 μm × 18.4 μm to increase the sensor radiation tolerance in the higher luminosity RHIC II environment. There are two data output lines from the sensor and the data rates are low thanks to the

newly included data sparsification circuitry. The first prototypes of this design are expected to be delivered in the 2010 time frame.

Sensor Series Specifications

The specifications of the sensors under development are shown in Table 5.

	Phase -1	Ultimate
Pixel Size	30 μm × 30 μm	18.4 μm × 18.4 μm
Array size	640 × 640	1024 × 1088
Active area	~ 2 × 2 cm	~ 2 × 2 cm
Frame integration time	640 μs	100 – 200 μs
Noise after CDS	10 e-	10 e-
Readout time / sensor	640 μs	100 – 200 μs
Outputs / sensor	4	2
Operating mode	Column parallel readout with all pixels read out serially.	Column parallel readout with integrated serial data sparsification.
Output type	Digital binary pixel based on threshold crossing.	Digital addresses of hit pixels with run length encoding and zero suppression. Frame boundary marker is also included.

Table 5: Specifications of the Phase-1 and Ultimate sensors.

The Phase-1 is a fully functional design prototype for the Ultimate sensor which results in the Phase-1 and Ultimate sensors having very similar physical characteristics. After successful development and production of the Phase-1 sensors, a data sparsification system currently under development at IPHC will be integrated with the Phase-1 design. With the additional enhancement of design changes allowing for faster clocking of the sub-arrays, the resulting sensor is expected to be used in the final Pixel detector. In addition to the specifications listed above, both sensors will have the following additional characteristics;

- Marker for first pixel
- Register based test output pattern JTAG selectable for binary readout troubleshooting.
- JTAG selectable automated testing mode that provides for testing pixels in automatically incremented masked window to allow for testing within the overflow limits of the zero suppression system.
- Independent JTAG settable thresholds
- Radiation tolerant pixel design.

- Minimum of 3 fiducial marks / sensor for optical survey purposes.
- All bonding pads located along 1 side of sensor
- Two bonding pads per I/O of the sensor to facilitate probe testing before sensor mounting.

Architecture for the Phase-1 Sensor System

The requirements for the Phase-1 prototype and final readout systems are very similar. They include;

- Triggered detector system fitting into existing STAR infrastructure and to interface to the existing Trigger and DAQ systems.
- Deliver full frame events to STAR DAQ for event building at approximately the same rate as the TPC (~ 1 KHz for the STAR DAQ1K upgrade).
- Reduce the total data rate of the detector to a manageable level (< TPC rate)

We have designed the prototype data acquisition system to read out the large body of data from the Phase-1 sensors at high speed, to perform data compression, and to deliver the sparsified data to an event building and storage device.

The proposed architecture for the readout of the Phase-1 prototype system is shown in with the physical location and separation of the system blocks shown in Figure 18 and Figure 19.
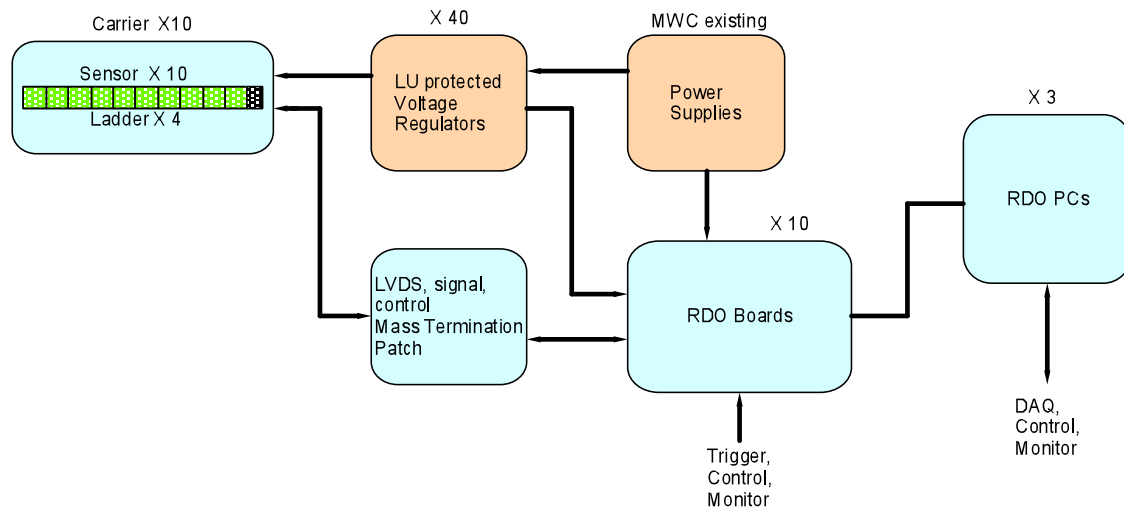
Figure 18: Functional block schematic for the readout for the Phase-1 prototype system. The detector ladders and accompanying readout system have a highly parallel architecture. One system unit of sensor array / readout chain is shown. There are ten parallel sensor array / readout chain units in the full system.
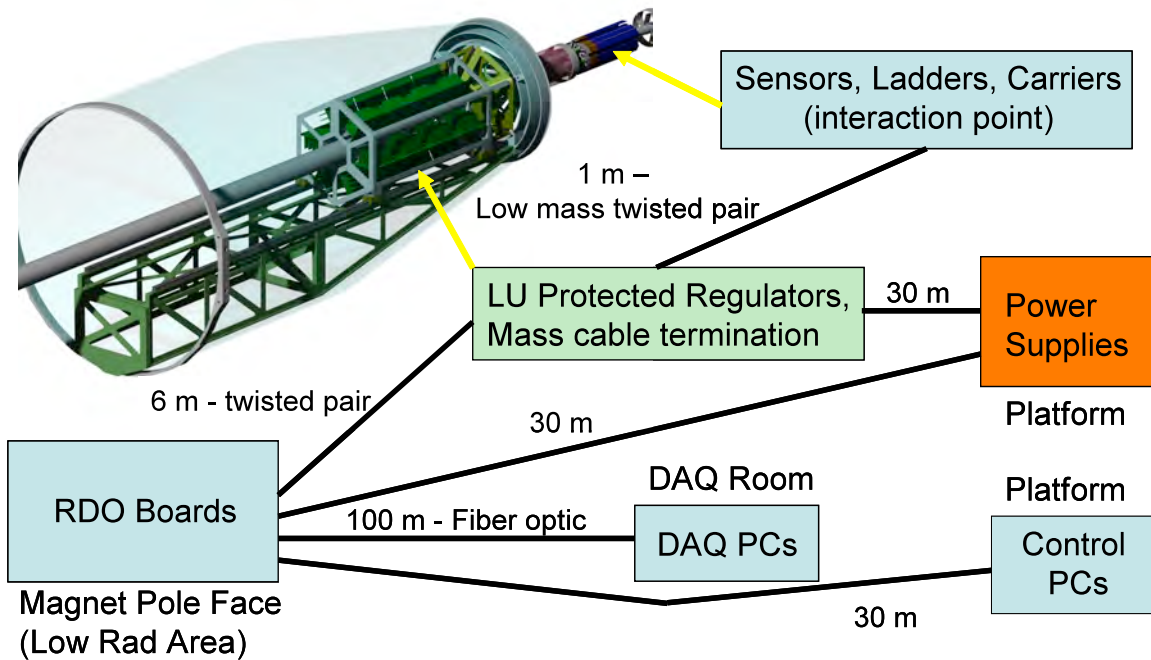
Figure 19: Physical layout of the readout system blocks. This layout will be the same for both the Phase-1 based patch and the final Pixel detector system.

The architecture of the readout system is highly parallel. Each independent readout chain consists of a four ladders mechanical carrier unit with each ladder containing ten Phase-1 sensors. The current plan is to install a patch of Phase-1 sensors consisting of at least two carrier units mounted with the final mechanical positioning structure and positioned with a 120 degree separation. The readout system will be described as if all carriers will be installed since this architecture also extends to the final Pixel system.

The basic flow of a ladder data path starts with the APS sensors. A Pixel ladder contains 10 Phase-1 APS sensors, each with a 640 × 640 pixel array. Each sensor contains four separate digital LVDS outputs. The sensors are clocked continuously at 160 MHz and the digital data containing the pixel threshold crossing information is read out, running serially through all the pixels in the sub-array. This operation is continuous during the operation of the Phase-1 detectors on the Pixel ladder. The LVDS digital data is carried from the four 160 MHz outputs in each sensor in parallel on a low mass flex printed circuit board to discrete LVDS buffers located at the end of the ladder and out of the low mass detector region. This electronics portion of the ladder also contains the buffers and drivers for the clocks and other control signals needed for ladder operation.

Each Phase-1 sensor requires a JTAG connection for register based configuration, power, ground, a 160 MHz readout clock and a synchronization signal to begin the readout. These signals and latch-up protected power as well as the LVDS outputs and synchronization and marker signals from the detectors are carried via low mass twisted pair cables from the discrete electronics at the end of the ladder to a power / mass termination board located approximately 1 meter from the Pixel ladders. There is one readout board per Pixel carrier (40 sensors). A diagram of a ladder is shown in Figure 20.

41
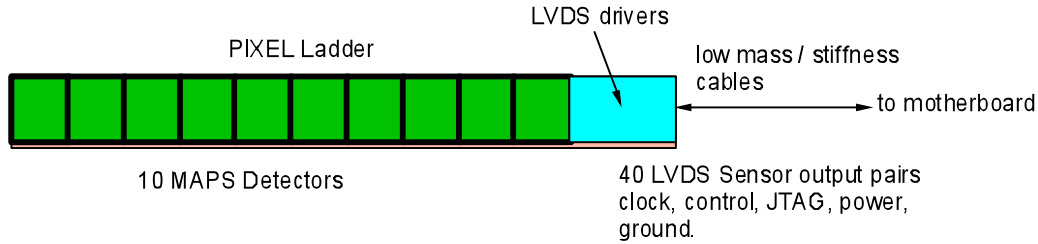
Figure 20: **Assembly of sensors on a low radiation length kapton flex cable with aluminum conductors. The sensors are connected to the cable with bond wires along one edge of the ladder.**

The flex cable parameters are shown below;

- 4 layer - 150 micron thickness
- Aluminum Conductors
- Radiation Length ~ 0.1 %
- 40 LVDS pair signal traces
- Clock, JTAG, sync, marker traces.

The connection to the driver end of the ladders will be made with very fine 150 μm diameter twisted pair wire soldered to the cable ends. These wires are also very low stiffness to avoid introducing stresses and distortions into the mechanical structure. The other ends of these fine twisted pair wires will be mass terminated to allow connection to the Power / Mass-termination (PM) board located approximately 1 meter away.

Latch-up protected power is provided to the sensors from the PM boards. Each ladder has independently regulated power with latch up detection circuitry provided by a power daughter card that plugs into the PM board. There are four regulation and latch-up daughter cards per PM board and a total of ten PM boards are needed for the complete detector system readout. A block diagram for the PM board is shown in Figure 21.

mass termination connectors to RDO Board

mass termination connector to Main Board

1 ladder of 10 sensors signal, pwr, gnd, clk, etc. Signal + misc. 150 micron dia wire power, gnd = larger dia.

Main Board

Cable to RDO Board

Power Reg. LU detection

Power Reg. LU detection

Power Reg. LU detection

Power Reg. LU detection

Molex type Power connection

Connector to Main Board

soldered connection

Figure 21: Power and mass-termination board block diagram. The digital signals to and from the sensors are routed through the main board and carried to mass termination connectors for routing to the readout boards. Latch-up protected power regulation is provided to each ladder by a power daughter card mounted to the main board. The main power supplies are located in the STAR racks.

The digital sensor output signals are carried with a 160 MHz clock to from the PM board to the readout boards (RDO) which are mounted either on the magnet iron of the STAR magnet structure or in a movable electronics rack located on the cave floor. Each location is approximately 6 meters away from the MTBs. A diagram describing the attributes of the two PCBs that make up the RDO system can be seen in Figure 22. A functional block diagram of the RDO can be seen in Figure 23.

Two board System – Virtex-5 Development board mated to a new HFT motherboard

Xilinx Virtex-5 Development Board

New motherboard

+

•Digital I/O LVDS Drivers
•4 X >80 MHz ADCs
•PMC connectors for SIU
•Cypress USB chipset
•Fast SRAM
•Serial interface
•Trigger / Control input

•FF1760 Package
•800 – 1200 I/O pins
•4.6 – 10.4 Mb block RAM
•550 MHz internal clock

Note – This board is designed for development and testing. Not all features will be loaded for production.

Figure 22: Readout board(s). The readout system consists of two boards per carrier of 40 sensors. A commercial Xilinx Virtex-5 development board is mated to a custom motherboard that provides all of the I/O functions including receiving and buffering the sensor data outputs, receiving the trigger from STAR and sending the built events to a STAR DAQ receiver PC via fiber optic connection.
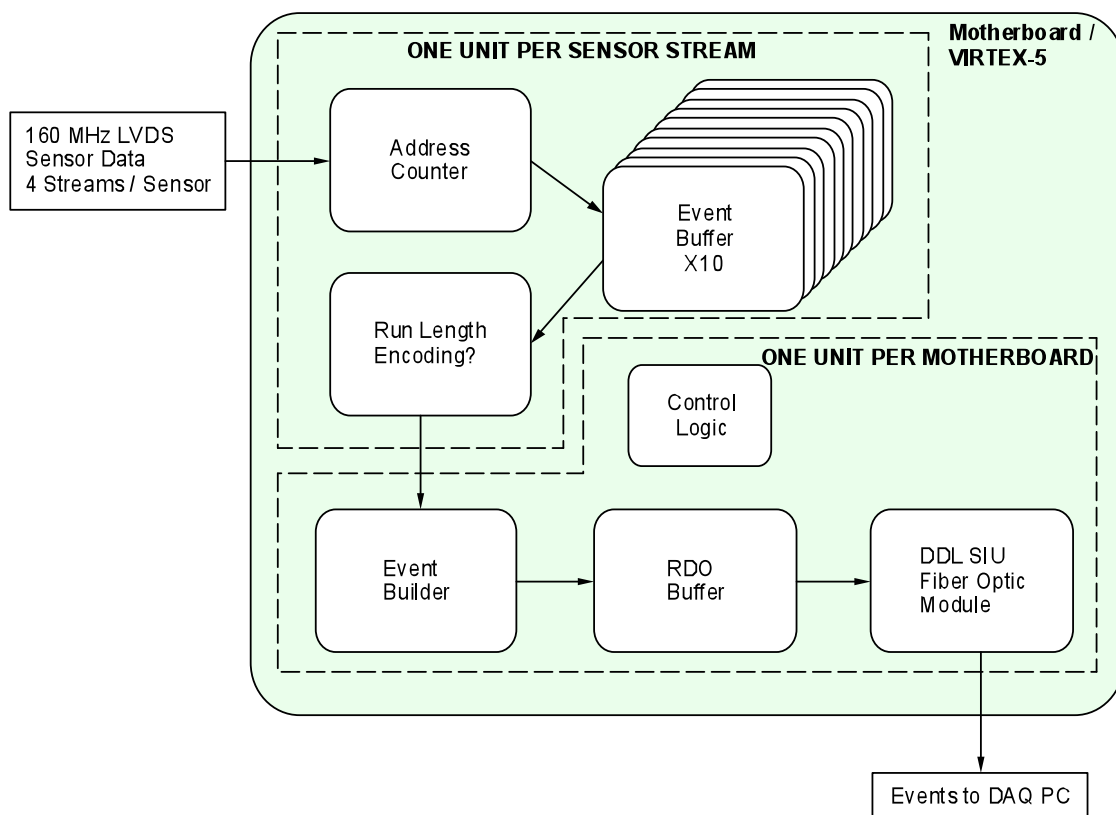
Figure 23: Functional block diagram of the data flow on the RDO boards.

The RDO boards are based on a fast Xilinx Virtex-5 FPGA development board which is mated to a custom motherboard that provides LVDS buffering into the FPGA, the STAR trigger input, PMC connectors for mounting the CERN developed fiber optic Detector Data Link (DDL), SRAM, and various ADCs and I/O to be used in testing. The data processing path is as follows. The sensor output signals are buffered and then fed into the FPGA. In the FPGA the data is resorted to give a raster scan, after which hits registered on pixels are converted to pixel addresses using an address counter. This mechanism of zero suppression, the conversion of hits to addresses in a relatively low multiplicity environment, is the main mechanism for data reduction used in this readout system. The efficiency and accidental rate of a simple threshold on pixel signal is shown in Figure 24.
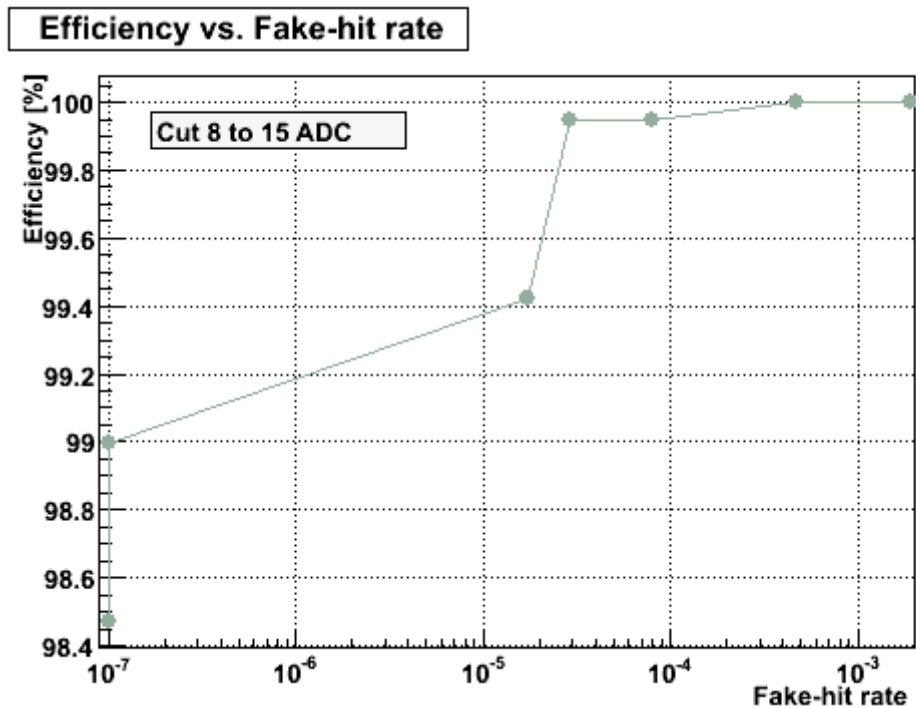
Figure 24: Efficiency and fake hit rate for a simple threshold cut on pixel signal level. This figure is obtained from beam data taken with Mimostar-2 sensors.

When a trigger is received, one of a bank of event buffers is enabled for one frame (409,600 pixels). After the frame has been recorded in the event buffer, the results of that frame are sent to an event builder. The event builder gathers all of the addresses on the RDO from that trigger and builds them into an event which is then passed via fiber optic links to the STAR DAQ receiver PCs. We intend to use the Source Interface Unit (SIU) and Readout Receiver Cards (RORC) developed for ALICE as our optical link hardware to transfer data to and from the STAR DAQ system. These links have been chosen as the primary readout connections for the new STAR TPC FEE. Leveraging existing hardware and expertise in STAR allows for a faster and more reliable design than developing our own custom solution. The complete system consists of a parallel set of carrier (4 ladder /

carrier) readouts consisting of 10 separate chains. A system level functionality block diagram is shown in Figure 25.
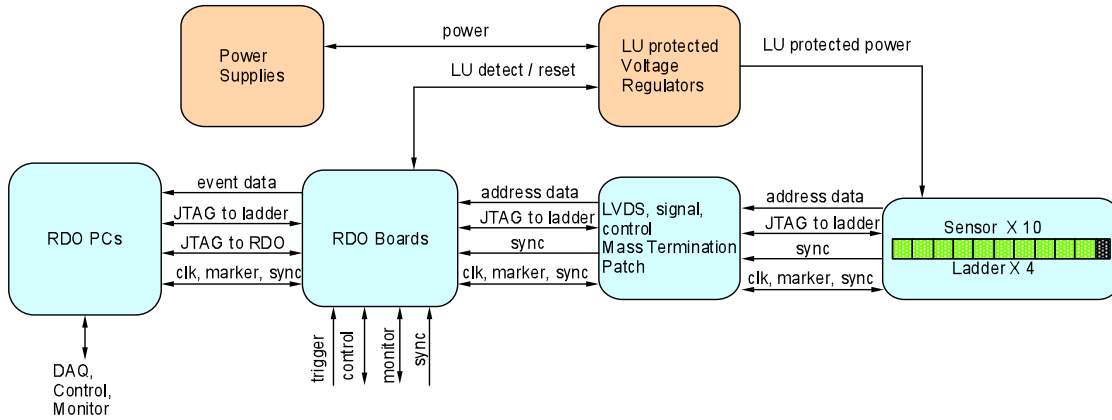
Figure 25: System level functionality diagram of the readout of the Pixel sensors. One of the ten parallel readout chains is shown.

Data Synchronization, Readout and Latency

The readout of the prototype Phase-1 Pixel sensors is continuous and hit-to-address processing is always in operation during the normal running of the detector. The receipt of a trigger initiates the saving of the found hit addresses into an event buffer for 1 frame (409,600 pixels). The Pixel detector as a whole will be triggered via the standard STAR Trigger Clock Distribution (TCD) module. Since 640 μs are required to read out the complete frame of interest, the data will be passed to DAQ for event building ~ 640 μs after the trigger is received. We will provide for multiple buffers that will allow the capture of temporally overlapping complete frames. This will allow us to service multiple triggers within the 640 μs readout time of the sensor. In this system, the hit address data is fanned out to 10 event buffers. A separate event buffer is enabled for the duration of one frame upon the receipt of a trigger from the TCD. Subsequent triggers enable additional event buffer until all of the event buffers are full and the system goes busy. The resulting separate complete frames are then passed to the event builder as they are completed in the event buffers. This multiple stream buffering gives a system that can be triggered at a rate above the expected average rate of the STAR TPC (approximately 1 kHz) after the DAQ1K upgrade. Furthermore, since the addition of buffers is external to the sensors, the capability for the addition of large amounts of fast SRAM will be included in the RDO board design allowing for flexibility in our readout system configuration. This multiple event buffer architecture will result in the duplication of some data in frames that overlap in time, but our data rate is low and the duplication of some data allows for contiguous event building in the STAR DAQ, which greatly eases the offline analysis. In addition, synchronization between the ladders/boards must be maintained. The Pixel will receive triggers and the STAR clock via the standard STAR Trigger and Clock Distribution module (TCD). We will provide functionality to allow the motherboards to be synchronized at startup and any point thereafter.

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Triggering Considerations

The primary tracking detector of the STAR experiment is the TPC with the Heavy Flavor Tracker upgrade designed to add high resolution vertex information. The Pixel detector is part of a larger group of detectors that make up the HFT upgrade at STAR. The other tracking detector components of the HFT include the Silicon Strip Detector (SSD) and the Intermediate Silicon Tracker (IST). Since the HFT is a system of detectors, in order to maximize efficiency, the trigger response and dead time characteristics of the each detector in the HFT system should be matched, as much as possible, to the others. As the main detector, the post DAQ-1K TPC sets the effective standard for the other detectors in the system. In the current understanding of the system, the Pixel detector information is only useful in conjunction with the external tracking detectors and thus the Pixel detector will only be triggered when the TPC is triggered.

The triggers in STAR are produced essentially randomly with a 110 ns crossing clock spacing. The behavior of the TPC is to go dead for 50 μs following the receipt of a trigger. This means that the TPC, and by extension the Pixel detector, will receive random triggers spaced by a minimum of 50 μs. An additional constraint is imposed by the fact that the DAQ 1K contains 8 buffers at the front end. This allows for the capability of the TPC to take a quick succession of 8 triggers (separated by 50 μs) but then the TPC will go busy until the data has been transferred and buffers cleared. The time required for this depends on the event size. (Some of these numbers can be found at http://drupal.star.bnl.gov/STAR/daq1000-capabilities others are private communication with the STAR DAQ group (Tonko Ljubicic)). This behavior provides the basis for the assessment of the trigger response characteristics of the detectors in the HFT system. In general, HFT detector readout systems should provide for the acquisition of up to 8 successive triggers separated by 50 μs with some, as yet uncharacterized, clearing time. The goal is to have the HFT detectors "live" whenever the TPC is "live". In appendix 1 we show some analysis of the trigger response characteristics of the Pixel detector.

System Performance for the Phase-1 Prototype Sensor System

The raw binary data rate from each Phase-1 sensor is 80 MB / s. For the 400 sensors that make up the Pixel detector this corresponds to 32GB / s. This raw data rate must clearly be reduced to allow integration into the overall STAR data flow. Zero suppression by saving only addresses of hit pixels is the main mechanism for data volume reduction. The parameters used to calculate the data rates are shown in Table 6.

Bits per address	20
Integration time	640 μs
Luminosity	3×10^{27}
Hits per frame on inner sensors (r=2.5cm)	295
Hits per frame on outer sensors (r=8.0cm)	29
Sensors inner ladders	100
Sensors outer ladders	300
Average pixels per cluster	2.5
Average trigger rate	1 kHz

Table 6: Parameters used to calculate data rates from a Phase-1 based system.

Based on the parameters given above, the average data rate (address only) from the sensors in the prototype Phase-1 detector is 237 kB / event which give an average data rate of 237 MB / s. It is possible to reduce the data rate further using a run length encoding scheme on the addresses as they are passed from the event buffer to the event builder as indicated in Table 6. We are currently investigating this option, though the data rate reduction from this approach is expected to be moderate. The raw data rate reduction from the hit pixel to address conversion is given graphically below as Figure 26.
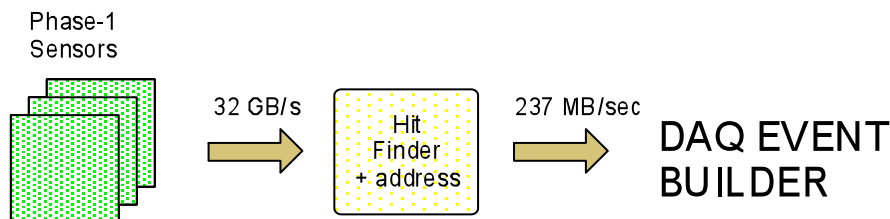
Figure 26: Data rate reduction in the Phase-1 readout system.

Architecture for the Ultimate Sensor System

The most significant difference between the Phase-1 and Ultimate sensors is the integration of zero suppression circuitry on the sensor. The ultimate sensors provide zero suppressed sparsified data with two LVDS output line per sensor. The pixel size for this final production sensor is reduced to 18.4 μm resulting in a larger array. This smaller pixel has a shorter charge collection time making it more radiation tolerant. In addition, the sub-frame arrays are clocked faster to give a <200 μs integration time and a frame boundary marker is added to the data stream to allow for the demarcation of frame boundaries in the absence of hits in the sensor and to allow for synchronization with the RDO system. The upgrade from the Phase-1 to the Ultimate sensors in the system is

expected to involve the fabrication of new sensor ladders using the same mechanical design used in Phase-1 but with the addition of new Ultimate series sensors and a redesign of the kapton readout cable. The Ultimate sensor kapton readout cable will require significantly fewer (20 LVDS pairs instead of 40) traces for readout and the new cable design should have a lower radiation length. The task of reading out the Ultimate series sensors is actually less challenging than the readout of the Phase-1 sensors since the data reduction functionality is included in the sensor. **The readout hardware described above for the Phase-1 readout system remains the same for the Ultimate readout system.** Some reconfiguration of the functionality in the FPGA is required for readout of the Ultimate sensor Pixel detector. A functional block diagram for the RDO boards is shown in Figure 27.
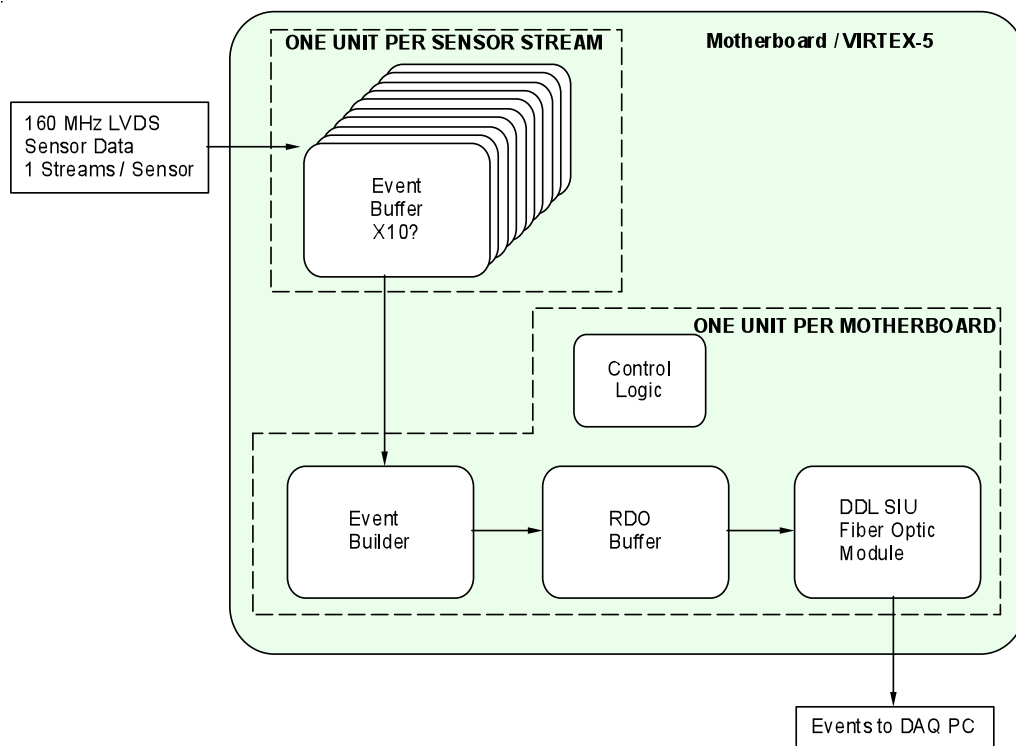
Figure 27: Functional block diagram of the RDO boards for the readout of the Ultimate detector based Pixel detector.

The Ultimate sensor operates in the same rolling shutter readout mode as the PHASE-1 sensor. The address data clocked out of the Ultimate chip has understood latencies that we will use to keep track of triggered frame boundaries and will be able to verify using synchronization markers from the sensors. The first pixel marker from the sensor corresponds to the actual scan of pixels through the sensor. The frame boundary marker delineates frame boundaries in the sparsification system on the sensor. Using this information and knowing the internal latencies in the sensor, we can generate the internal logic in the FPGA to implement the same multiple buffering technique that was previously described.

System Performance for the Ultimate Sensor System

The parameters used to calculate the data rates for the system are shown in Table 7.

Bits per address	20
Integration time	200 µs
Luminosity	8×10^{27}
Hits per frame on inner sensors (r=2.5cm)	246
Hits per frame on outer sensors (r=8.0cm)	24
Sensors inner ladders	100
Sensors outer ladders	300
Average pixels per cluster	2.5
Average trigger rate	1 kHz

Table 7: Parameters used to calculate data rates from a Ultimate sensor based system.

From these parameters, we calculate an average event size of 209 kB giving an address data rate of 209 MB / s from the Ultimate sensor based Pixel detector.

A more detailed analysis of the readout chain including parameters such as the size of buffers and the internal FPGA functions is included as appendix 1.

4.2.2.   Sensors and Readout Simulation and Prototyping

Mimostar-2 based telescope test at STAR

Using a preliminary system design for analog readout, we have taken data with a set of Mimostar-2 sensors at STAR. This system is an early prototype whose performance is evaluated as part of the overall vertex detector development effort. We have successfully implemented a continuous readout 50 MHz data acquisition system with on-the-fly data sparsification that gives near three orders of magnitude data reduction from the raw ADC rates. This readout system has been mated with prototype Mimostar2 sensors and configured as a telescope system to measure the charged particle environment in the STAR environment near the final detector position. This telescope is shown in Figure 28.

Figure 28: Three Mimostar-2 sensors in a telescope configuration used in a beam, test at STAR.

We find that the system works well, gives reasonable efficiency and accidental hit rates, and measures an angular distribution of tracks consistent with imaging the interaction diamond and with imaging beam-gas interaction type background. The prototype readout system integrated well into the existing STAR electronics and trigger infrastructure and functioned successfully as another STAR detector subsystem. This prototype readout system and the results obtained are described in a NIM paper.[32]

LVDS Data Path Readout test

The readout system architecture for the Phase-1 and Ultimate sensors to be used in the Pixel detector for the Heavy Flavor Tracker upgrade at STAR contains a high speed digital data path that is required to read out the sensor hits during the sensor integration time. The RDO sensor data interface path requires that LVDS data move over a total distance of 6 – 8 meters with a speed of 160 MHz for Phase-1 and 125 MHz for Ultimate. 1-2 meters of this distance is over high impedance fine twisted pair wire. Since this design is challenging, though it works on paper, it is prudent to make a prototype set of testing boards and check the performance of our design as a precursor to starting a production design for the final set of readout boards. We have completed making a complete set of test boards for one basic block of the highly parallel RDO system consisting of a functional ladder mockup, mass termination board prototype and a limited functionality RDO motherboard coupled to a Xilinx Virtex-5 Development board. The test was successful with bit error rates of approximately 10-15 for the configurations and clock speeds needed for the detector. A report on this test may be found as Appendix 2.
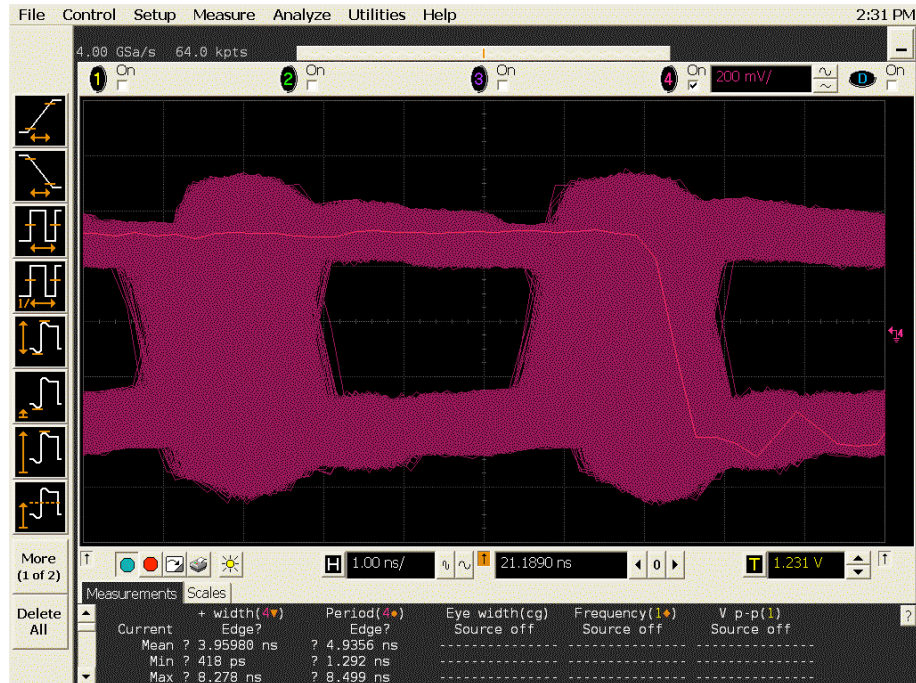
Figure 29: 200 MHz Data eye pattern measured at the RDO motherboard input to the FPGA (after all buffers) and triggered on the output data from the FPGA. Full width opening in system is ~ 2.3 ns.

4.2.3.   Mechanical Design

Design Overview

The mechanical design has been driven by the following design goals:

- Minimize multiple coulomb scattering, particularly at the inner most layer
- Locate the inner layer as close to the interaction region as possible
- Allow rapid detector replacement
- Provide complete spatial mapping of the pixels from the beginning

The first two goals, multiple coulomb scattering and minimum radius, set the limit on pointing accuracy to the vertex. This defines the efficiency of D and B mesons detection.

The third goal, rapid detector replacement, is motivated by recognition of difficulties encountered in previous experiments with unexpected detector failures. This third goal is also motivated by the need to replace detector that are radiation damaged from operating so close to the beam.

The fourth goal, complete spatial mapping, is important to achieve physics results in a timely fashion. The plan is to know at installation where the pixels are located with respect to each other to within 20 microns and to maintain the positions throughout the operation.

The pixel detector (see Figure 30) consists of two concentric barrels of detector ladders 20 cm long. The inner barrel has a radius of 2.5 cm and the outer barrel has an 8 cm radius. The barrels separate into two halves for assembly and removal. In the installed location both barrel halves are supported with their own 3 point precision kinematic mounts located at one end close to the detector barrel. During installation, support is provided by the hinge structures mounted on a railed carriage. Cooling is provided by air flowing in from one end between the two barrel surfaces and returning in the opposite direction over the outer barrel surface and along the inner barrel surface next to the beam pipe.
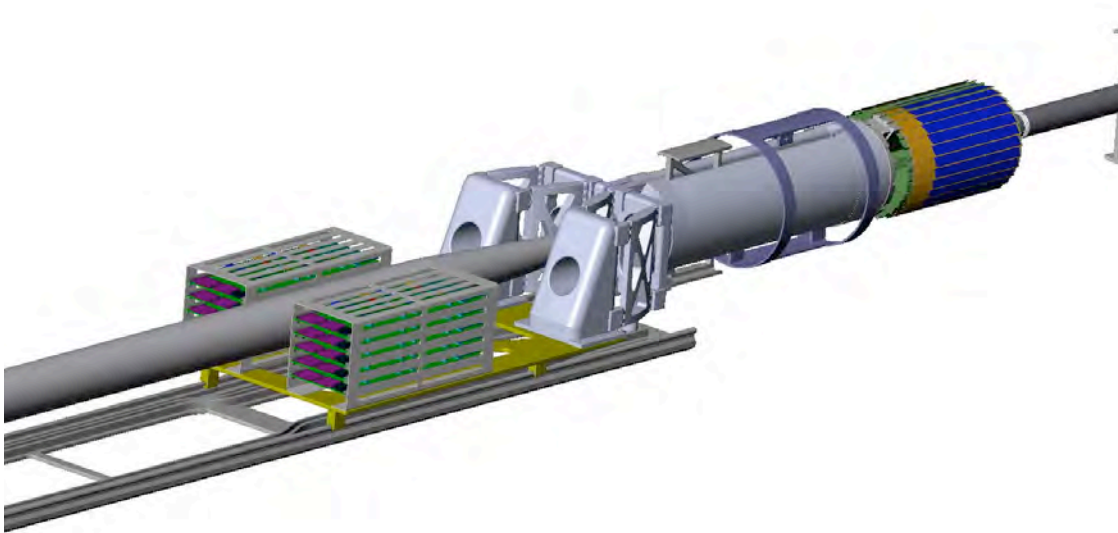
Figure 30: Pixel detector mechanics showing detector barrel, support structures and insertion parts plus interface electronics boards.

The design of the components is presented in the following section. Related structural and cooling analysis is covered in Appendix 2.

Detector ladder design

As previously mentioned (Section 4.2.1) the detector chips are arranged 10 in a row to form a ladder. An exploded view of the mechanical components is shown in Figure 31. The thinned silicon chips are bonded to a flex aluminum Kapton cable which is in turn bonded to a thin carbon composite structure. All electrical connections from the chips to the cable are done with a single row of wire bonds along one edge of the ladder. The carbon composite sheet which is quite thin will only be sufficient for handling and heat conduction. The primary stiffness and support of the ladder is provided by the support beam. This particular ladder structure has not been built yet, but it will utilize

construction methods that we have developed in our previous prototype designs which included gull wing and foam laminate designs. The assembly of the ladder and the attachment of ladders to the sectors is done with specialized vacuum tooling developed for this project.Parts are aligned and held in place with vacuum chuck tooling for bonding. Fifty micron soft, pressure sensitive acrylic adhesive 200MP by 3M is used to make the bonds. A method has been developed method has been developed which uses a 4 bar pressure chambervacuum bag and the pressure of an autoclave to remove bond voids and to stabilize the bond. The low elastic modulus of the adhesive is an important component in the design as it greatly reduces bi metal type deformations stemming from differential expansion caused by thermal changes and humidity changes. This will be discussed in more detail in Appendix 2.

The next step in the ladder development will be to build mechanical prototypes to verify the mechanical design both structurally and thermally.
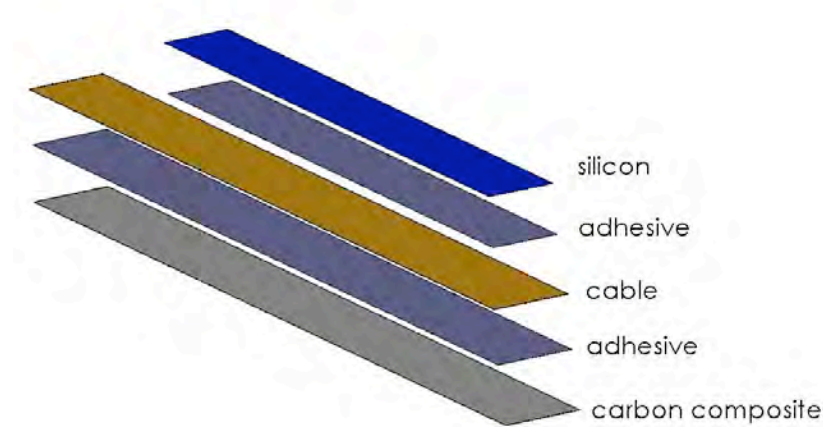
Figure 31: Exploded view of the ladder showing components. The silicon is composed of 10 ~square chips, bit it is shown hear as continuous piece of silicon as it has been modeled for analysis.

Ladder support system

A critical part of the ladder support is the thin carbon composite beam which carries one inner ladder and three outer ladders as shown in Figure 32. This beam which is an adaptation of the ALICE pixel detector design provides a very stiff support while minimizing the radiation length budget. Significant stiffness is required to control deformations from gravity, cooling air forces and differential expansion forces from both thermal and humidity variations. The composite beam carries a single inner ladder and three outer ladders. Ten of these modules form the two barrel layers. The beam in addition to its support function provides a duct for cooling air and adds cooling surface to increase heat transfer from the silicon chips. By making the beam from high strength and high thermal conductivity carbon fiber the wall thickness can be as thin as 200 microns and still satisfy strength and heat transfer requirements. The final thickness however, will probably be limited by fabrication challenges. Forming methods under consideration are a single male mandrel with vacuum bagging or alternatively nested male and female mandrels. We have constructed seven layer, 244 micron thick, carbon composite beams using a female mandrel which satisfy our requirements.
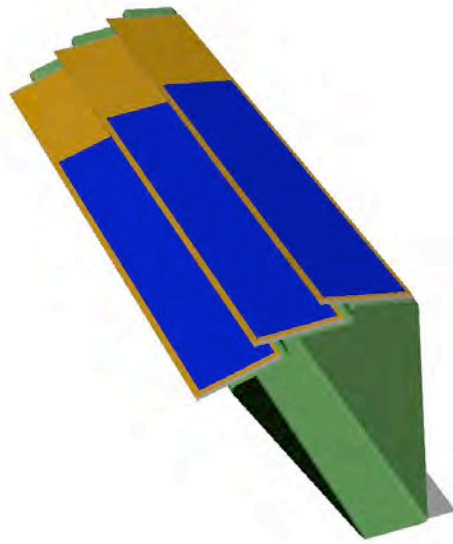
Figure 32: Thin wall carbon support beam (green) carrying a single inner barrel ladder and three outer barrel ladders. The beam in addition to supporting the ladders provides a duct for conducting cooling air and added surface area to improve heat transfer to the cooling air.

The ladders will be glued to the beam using a low strength silicon adhesive as was done in the ATLAS pixel design. This adhesive permits rework replacement of single ladders.

Support of the sectors (beam with ladders) is done in two halves with 5 sector beams per half module (see Figure 33). The sector beams are attached to carbon composite "D tube" with precision dove tail mounts for easy assembly and replacement.
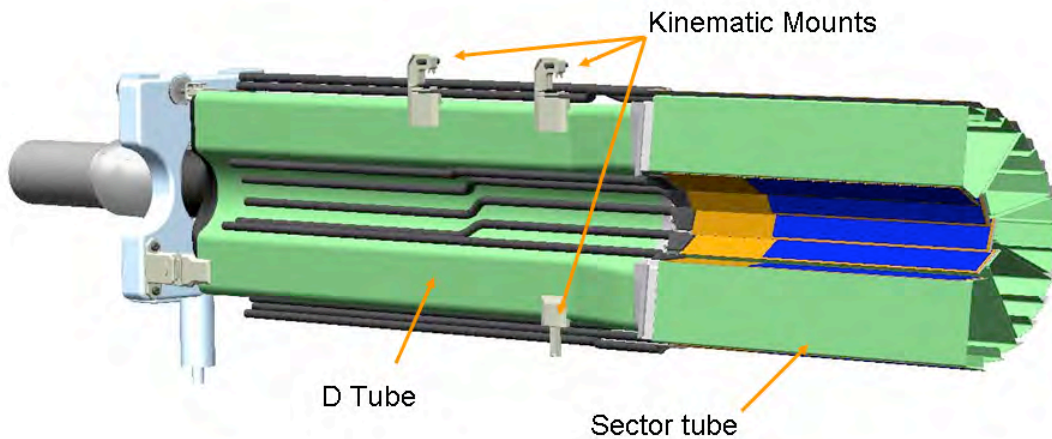
Figure 33: Half module consisting of 5 sector beam modules. The sector beam modules are secured to a carbon composite D tube using a dove tail structure which permits easy replacement of sector modules. Carbon composite parts are shown in green for greater visibility.

The "D tube" supports the 5 sector beams and conducts cooling air to the sectors.

Kinematic support and docking mechanism

When the pixel detector is in its final operating position it is secured at 3 points with precision reproducible kinematic mounts to the Inner Support Cylinder (ISC) as shown in Figure 34.
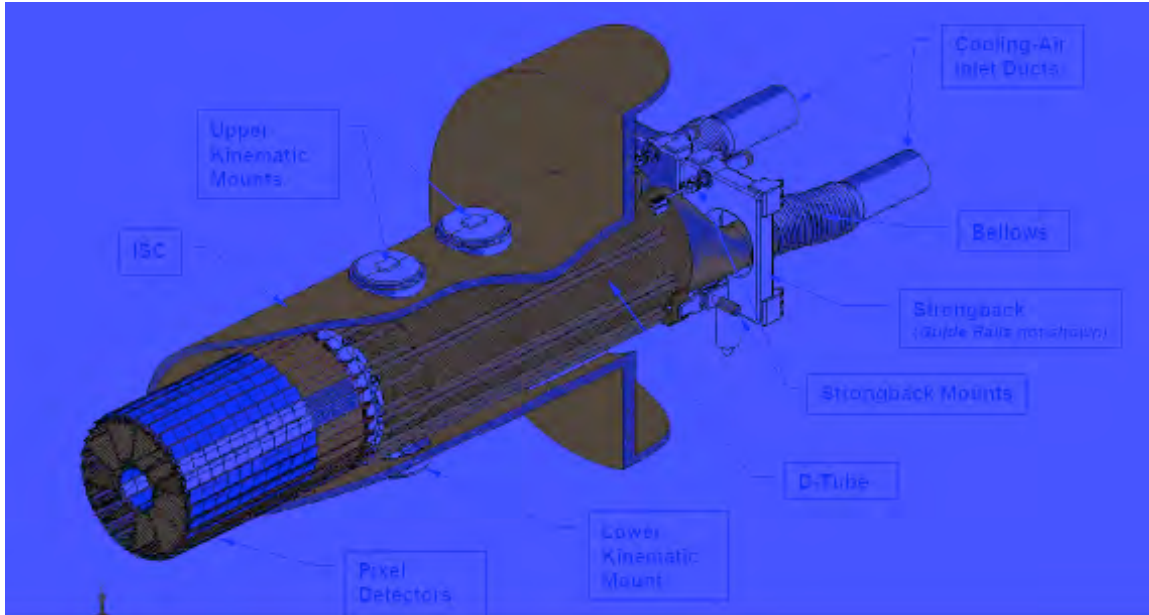
Figure 34: Detector assembly in the installed position supported with three kinematic mounts.

A more detailed view of the kinematic mounts is shown in Figure 35. The mounts provide a 3-2-1 constraint system which should allow repeatable installation to within a few microns.
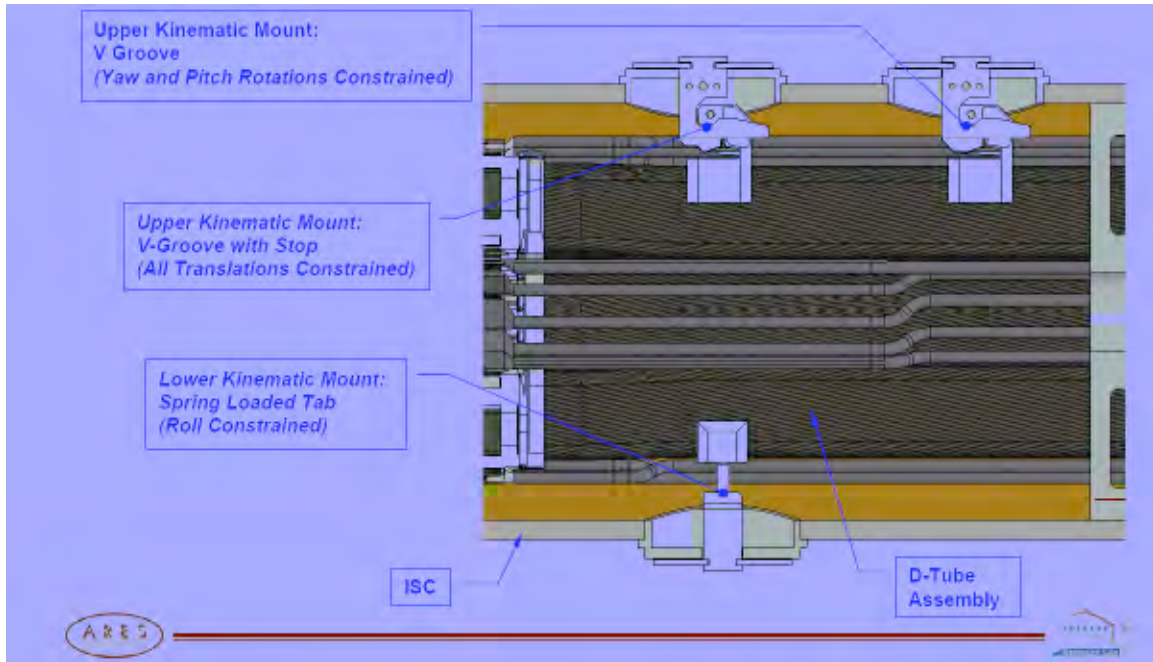
Figure 35: Detailed view of the kinematic docking mounts for the pixel detector. The mounts provide a fully constrained support and operate with a spring loaded over center lock down.

Insertion mechanism and Installation

The mechanics have been design for rapid installation and replacement. Instillation and removal of the pixel detector will be done from outside of the main STAR system with minimum disruption to other detectors systems. This will be done by assembling the two halves of the detector on either side of the beam pipe on rails outside of the STAR magnet iron. The detector carriage will be pushed into the center of STAR along the rails until it docks on the kinematic mounts. As shown in Figure 36 and Figure 37 the hinged support structure is guided by cam followers to track around the large diameter part of the beam pipe and close down at the center into the final operating position. Once the detector is docked in the kinematic mounts the hinged support from the carriage is decoupled allowing the kinematic mounts to carry the light weight detector system with a minimum of external forces affecting the position of the detector barrels. The external loads will be limited to the cables and the air cooling ducts. The cables are loosely bundled twisted pairs with 160 micron conductor plus insulation, so this load should be minimal. The two inch cooling ducts will be the greater load and may require additional design effort to isolate their effect so that the 20 micron position stability for the pixels can be maintained.
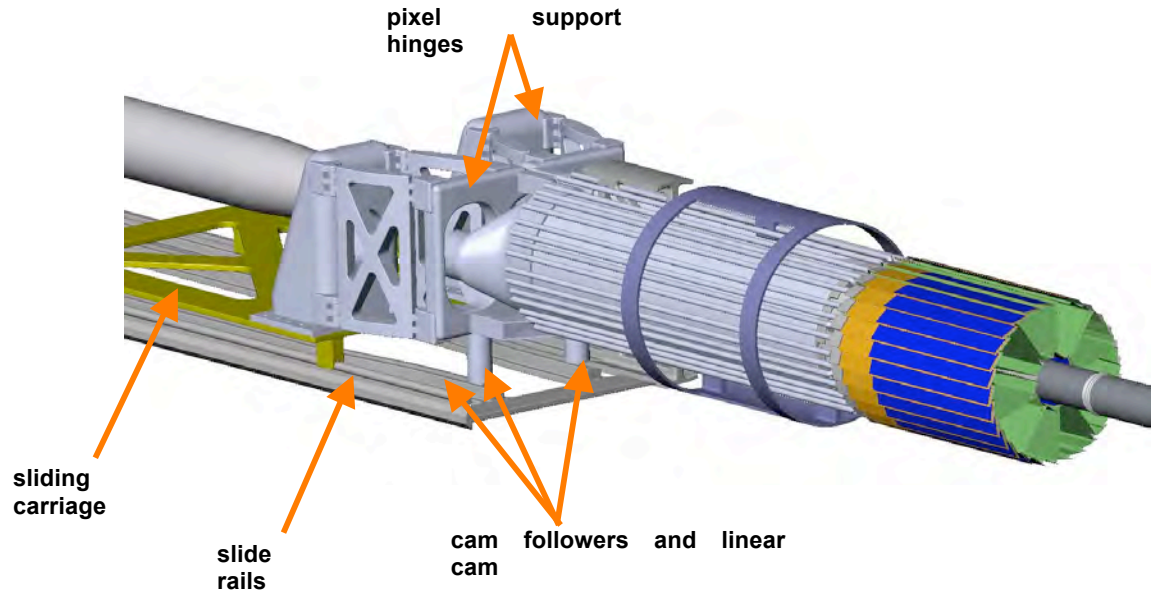
Figure 36: Track and cam guide system for inserting the detector.
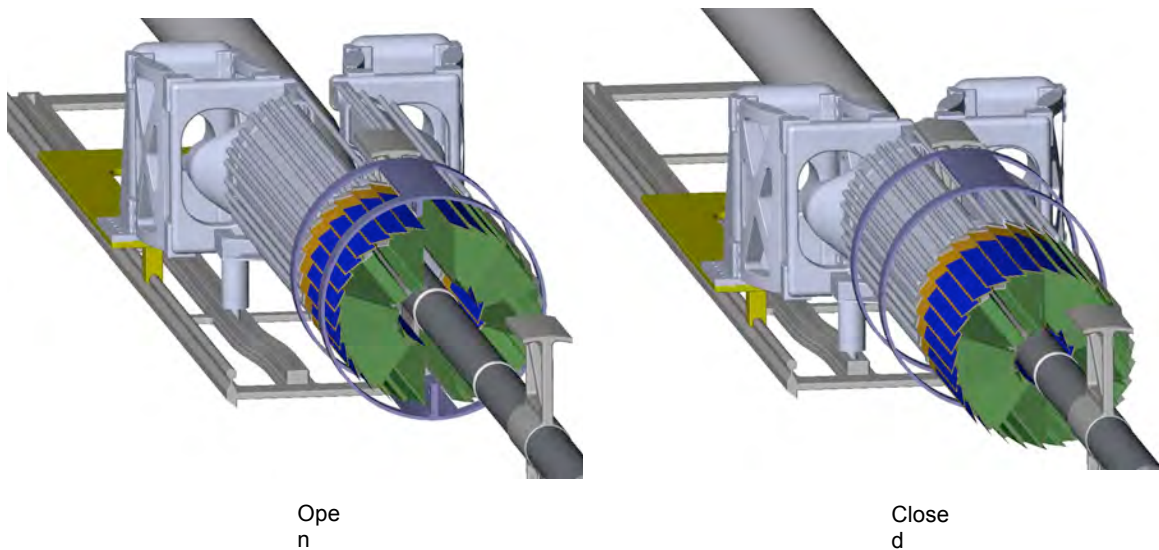
Open   Closed

Figure 37: Initially the detector halves have to be sufficiently open to clear the large diameter portion of the beam pipe. It then closes down sufficiently to fit inside the IFC while clearing the beam pipe supports and then finally it closes down to the final position with complete overlapping coverage of the barrels.

Cooling system

Cooling of the detector ladders with pixel chips and drivers is done with forced air. The pixel chips dissipate a total of 160 watts or 100 mW/cm^2 and an additional 80 watts is required for the drivers. In addition to the ladder total of 240 watts some fraction of this is required for voltage regulators and latch up electronics that are off the ladder but reside

in the air cooled volume. The temperature of operation is still under consideration. An optimum temperature for the detectors is around 0 deg C, but they can be operated at 34 deg C without too much noise degradation. The cooling system design is simplified if we can operate at 24 deg C, slightly above the STAR hall temperature, however if the cooler temperature is required the cooling system will be equipped with thermal isolation and condensation control when the system is shut down. In any case the design will include humidity and temperature control as well as filtration. Cooling studies (see Appendix 2) show that air velocities of 8 m/s are required over the detector surfaces and a total flow rate of 200 cfpm is sufficient to maintain silicon temperatures of less than 12 deg C above the air temperature.

The detector cooling path is shown in Figure 38. Air is pumped in through the support beam. A baffle in the ISC forces the air to return back over the detector surfaces both along the beam pipe and along the ISC.
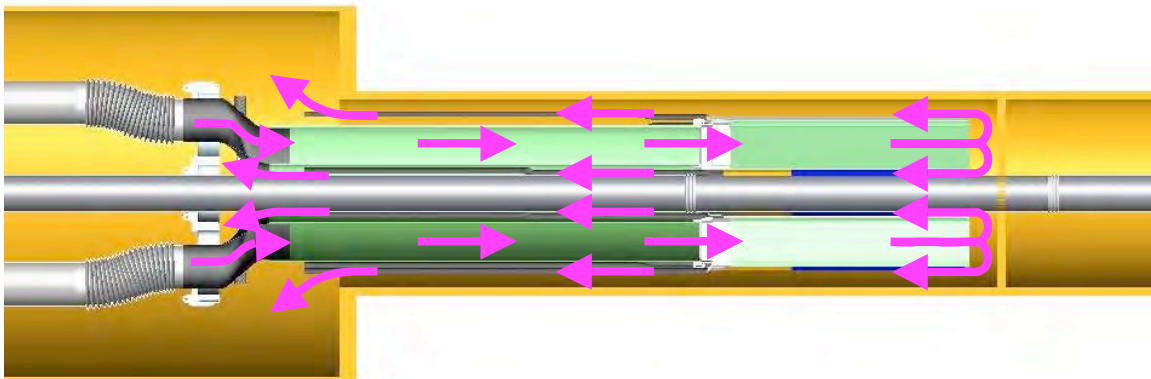
Figure 38: Pixel detector cooling air path. The air flows down the center of the sector modules and returns back over the detector ladders on the sector modules and into the larger ISC volume where it is ducted back to the air cooling unit.

The air chiller system providing the cooling air circulating through the pixel detector has not been completely specified yet, but sizing and ducting have been investigated for a system (see Figure 39) with 400 cfpm capacity (twice currently expected requirement). A commercially available centrifugal pump with a 5 horsepower motor is sufficient for this system. It is expected that the chiller would be located in the wide angle hall within 50 ft of the pixel enclosure and would be connected with 6 inch flexible ducts. An estimate of the required chiller heat capacity is given in Table 8.

Air flow: 400 SCFM

Total pressure drop: 22 inches water

Wide angle hall

ISC

external duct 6 in diameter X 50 ft

chiller

Internal duct 2 in diameter X 5 ft

pump

Internal duct 2 in diameter X 5 ft

external duct 6 in diameter X 50 ft
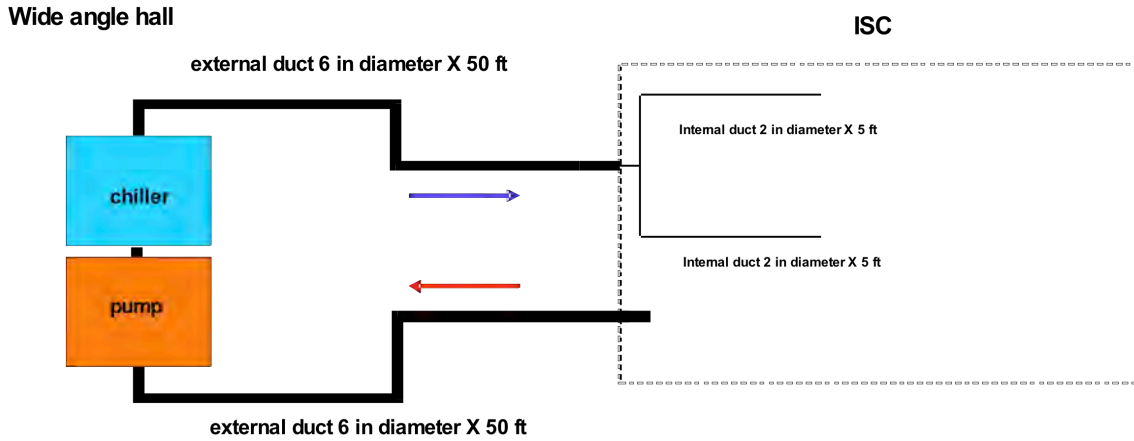
Figure 39: Schematic outline of air cooling system for the pixel detector.

Heat source	Power (watts)
detector silicon	160
on ladder signal drivers	80
voltage regulators in ISC	24
heat influx through ducting and ISC if 35 deg C below ambient	600 - 2000
pumping	1000
Total load on chiller	1900 - 3300

Table 8: Preliminary estimate of heat load on the chiller for the pixel air cooling system.

Cabling and Service system

The required wiring connections are identified in Figure 19. The 2 m fine wire twisted pair (pair diameter .32 mm) bundles leading from the ladders to the interface cards are designed to minimize mass, space and mechanical coupling forces that could disturb the pixel positions. The space envelope required for these bundles is illustrated in Figure 40.
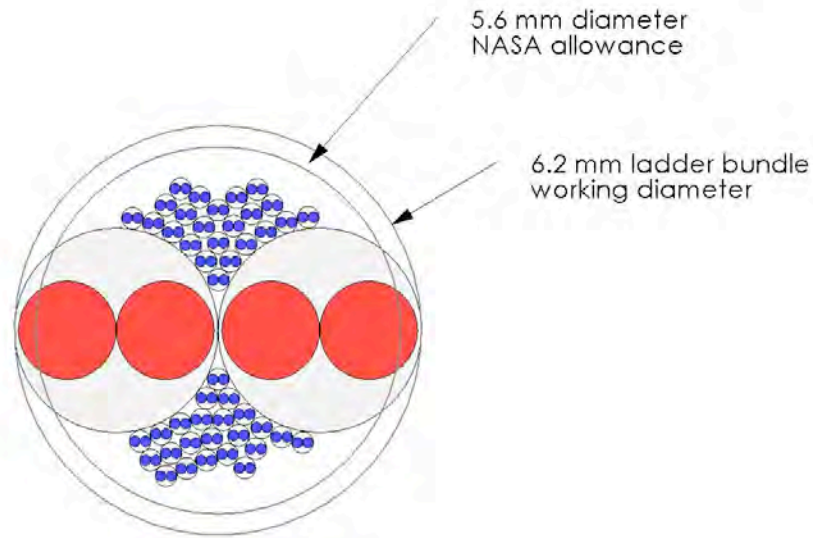
Figure 40: Cable bundle envelope for ladder connections. The blue pairs include 40 signal pairs, clock and trigger lines and JTAG communication. The red conductors are power.

There will be a 2'X2'X3' crate for the readout boards. This must be located outside of the main magnetic field and outside of the highest particle flux region. To achieve the required data transfer rates the LVDS signal cables running between this crate and drivers inside the ISC are limited to 6 meters. To meet these constraints the readout crate will a be located on the floor at the end of the magnet (there is no space on the magnet end ring for mounting the readout box). This will allow operation of the pixel system both with and without the pole tip in place (there is no space on the magnet end ring for mounting the readout box). The crate will be portable on wheels to accommodate end cap access requirements. Compared to the cables running to the detector the power and fiber optic cables from the readout crate to the outside are relatively small and provide little handling burden.Installation

Alignment and spatial mapping

The pixel system is being designed to have full pixel to pixel spatial mapping at installation with a 3D tolerance envelope of 20 microns. This will eliminate the need for spatial calibration with tracking other than determining the 6 parameters defining the pixel detector unit location relative to the outer tracking detectors. Tracking, however, can used with the pixel detector to spatially map the outer detectors if required.

The mapping and alignment will be done by using a vision coordinate machine to determine the detector locations on the fully constructed 20 ladder half modules. A full 3D map of the ladders is necessary since the manufactured ladder flatness will exceed the 20 micron envelope. After mapping the half modules will be installed in STAR without disturbing the relative positions of the pixels.

Addressing this in more detail, a support fixture for the half modules will be used in the vision coordinate machine which has kinematic mounts identical to the kinematic mounts in the ISC for securing the half module. The pixel chips will be manufactured with

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reference targets in the top metal layer that can be picked up by the vision coordinate machine and the ladders will be mounted such that there is an unobstructed view. The fixture will be rotated for each ladder measurement. Full 3D measurements of the chips on the ladder are required since the ladder flatness will lie outside of the 20 micron envelope. The fixture will have precision reference targets on each ladder plane so that the ladder points can be tied together into a single coordinate frame. The map of the fixture targets can be measured once with a touch probe measuring machine and thus avoid extreme machining tolerance requirements for the fixture. Precision machining, however, will be required, for the kinematic mounts and their placement tool.

For this approach to work the ladders must hold to their mapped position within 20 microns independent of changes in temperature, humidity and gravity direction.

The detector ladders have 1 mm overlapping active regions with their neighbors, so a check of the mapping accuracy will be done with tracking.

Information on Mechanical Design Simulation and Prototyping may be found in Appendix 2.

4.3.   The Intermediate STAR Tracker

Overview

The IST must meet a number of tracking requirements and should also be able to cope with the experimental constraints.

The best figure of merit for the tracking capabilities is the final D0 reconstruction efficiency. However, determining this efficiency involves extensive GEANT simulations and analysis. The choices that are presented here to meet the requirements are based on a much more simplified tracking code which has successfully been checked against the full calculations in a number of major cases. This simplified code was used to determine the optimum radius of the IST barrel and the internal geometry of the silicon pad sensors.

The most important of the experimental constraints are data taking rate capabilities, radiation levels and the material budget. The data rate and radiation levels are constrained by the RHIC environment and have to be taken into account in the sensor and readout chip choice. The material budget is connected to the tracking capabilities of the inner tracking system, but has also a large impact on the capabilities of more outward located detectors and their associated physics programs. To produce a low mass IST with enough mechanical rigidity has led to the choice of state-of-the-art materials.

Figure 41 shows the IST as it has been implemented in SolidWorks. Part of the red readout cables have been removed to give a view of the ladders, sensors and readout chips.
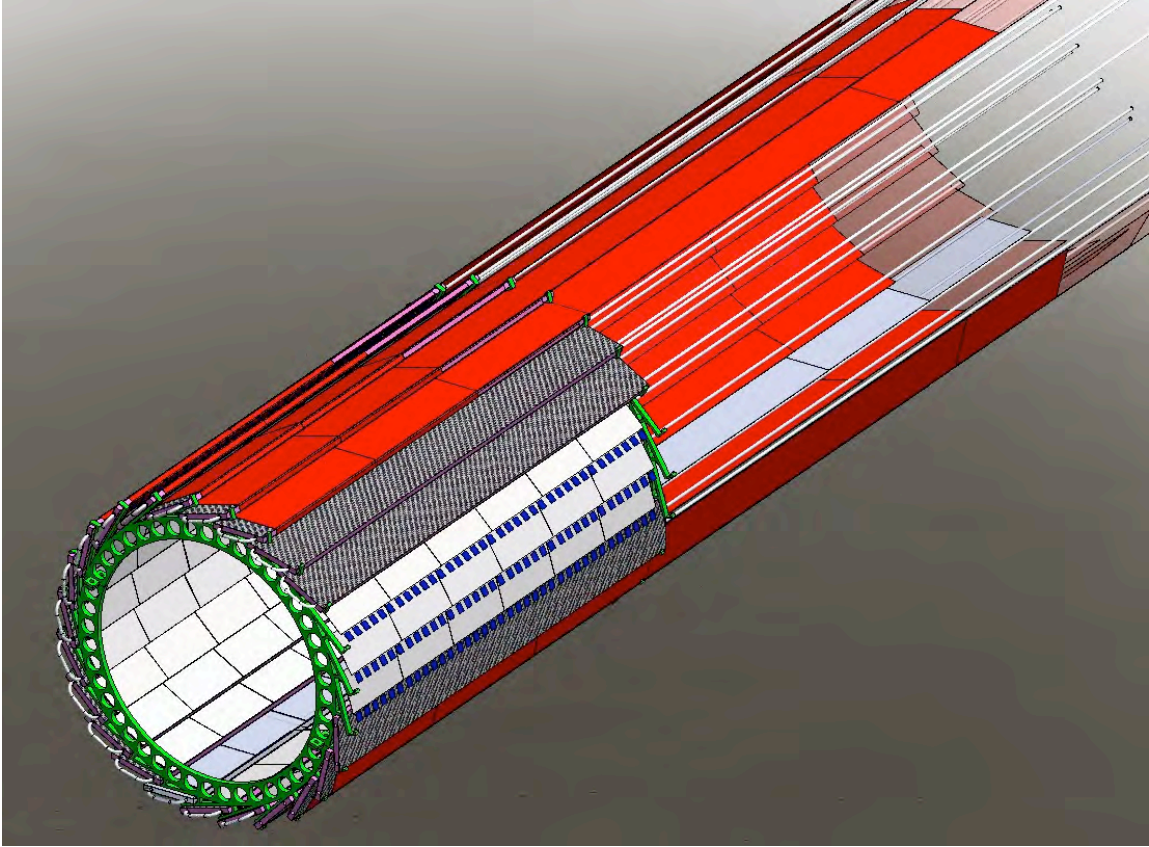
Figure 41: SolidWorks model of the IST

Tracking efficiency

The tracking efficiency is defined as the percentage of correct single tracks found by the inner tracking system when presented with events with only one track. This efficiency can be found by a full simulation with GEANT and the STAR tracking analysis. A faster MC code which includes the basic STAR tracking and multiple scattering calculates the efficiencies for 750 MeV/c kaons, which is important because these are the particles that need to be tracked for D0 reconstruction. To achieve the desired physics goals within one or two RHIC runs, the whole inner tracking system should have a single track efficiency of better than 80%. If the SSD or the IST is not able to provide a proper space point for the track, because of less than 100% coverage or broken channels, then the efficiency should still be above 70%.

Data taking rate

The IST should be able to operate without significant event pile-up for 200 GeV Au+Au collisions. Therefore, the IST has to be able to resolve interactions from each beam bunch crossing which are occurring every 116 ns. The spin program at RHIC relies on individual beam bunch crossings to set and determine the relative spin orientations in the proton beams. Also here the IST should be able to resolve individual beam bunches.

Radiation environment

Extrapolating the radiation doses received by the RHIC experiments during the past RHIC operations, it is expected that the total radiation dose for the IST barrel will not exceed 30 kRad per year. Both the silicon sensors and the readout chips on the hybrids are required to be fully operational after 10 years of operation.

Low mass and mechanical stability

The mass requirements for the IST are defined by the heavy ion physics requirements in the mid-rapidity region and by the W−boson spin physics program for more forward rapidities. To make the multiple Coulomb scattering comparable to the detector resolution the thickness of the IST layer should be less than or equal to 1.5% of a radiation length.

4.3.1. Design Choices

IST radius and silicon sensor geometry

The Intermediate Silicon Tracker is located between the outer layer of the PIXEL detector and the SSD. Taking mechanical constraints into account a possible radius range is from 12 to 20 cm. This radius has to be optimized for reconstruction efficiency while keeping SSD and IST redundancy in mind. The IST barrel should cover the full acceptance of the STAR TPC, i.e. 2π coverage for $-1 < \eta < +1$. In addition the IST should also be able to accommodate some of the z-range of the interaction point.

At the highest RHIC energy of 200 GeV for Au+Au collisions the charged particle density at a radius of 12 cm can easily exceed 1 per cm^2. The silicon sensors need to be divided into pads such that the occupancy of the individual pads do not exceed the few percent level. However, the occupancy is fully determined by the number of active elements and can be reached by different sensor geometries. What has to be taken into account is the double-hit probability within the search area on the IST sensors resulting from the pointing resolution of the TPC and SSD. Figure 42 shows the occupancy of a sensor with 768 active elements and the fraction of hits that are accompanied by 1 or more hits in the search area. In the case of a silicon strip detector the search area is defined by the width of the search area and the length of the strips. At the proposed radius of 14 cm more than 10% of the tracks would result in ambiguous IST hits. For the proposed silicon pad sensors this drops to around 1%. Finally, the number of active elements is mostly determined by the density with which the readout chips can be packed on the hybrids.
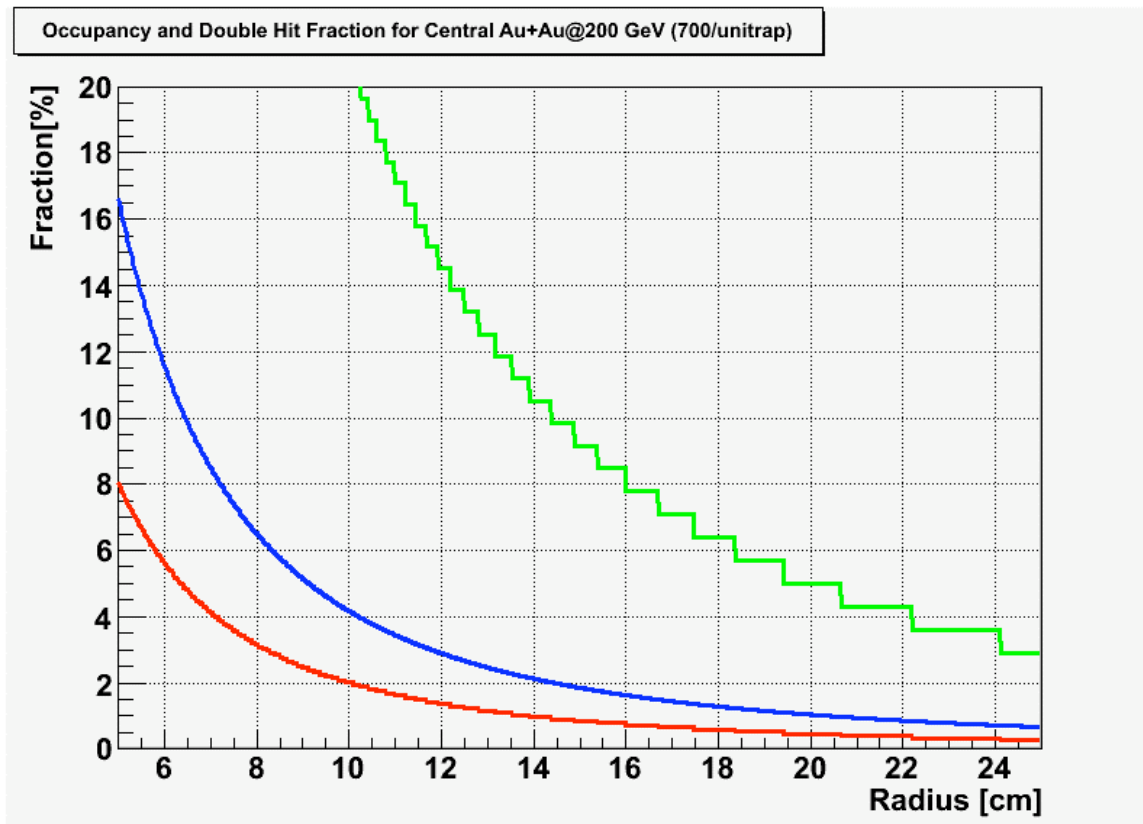
Figure 42: Occupancy [blue curve] and double-hit fraction for a silicon strip detector [green curve] and a silicon pad sensor [red curve].

Silicon pad sensors are very well suited to the RHIC environment and proved their suitability in the Phobos experiment. Figure 43 shows a study of the single track finding efficiency of the whole HFT as a function of the pad layout of the IST sensors. The better resolution (the size of the pads on the y-axis) is in r-phi, the bending plane. From these studies it was determined that 512 channels arranged in strips of roughly 600 μm x 6000 μm give an acceptable efficiency of about 83%. Going to more channels could give a slightly better efficiency but would lead to space problems when trying to mount more readout chips on the hybrids. The left plot shows the efficiency when hits from the SSD are not included in the tracking. This could happen because of small gaps in the SSD acceptance or broken channels. This study shows that the single track finding efficiency increases to 73%. This has to be compared to 50% if the IST would not be there and only the TPC would provide tracking to the PIXEL. The IST greatly adds to the redundancy of the inner tracking system.
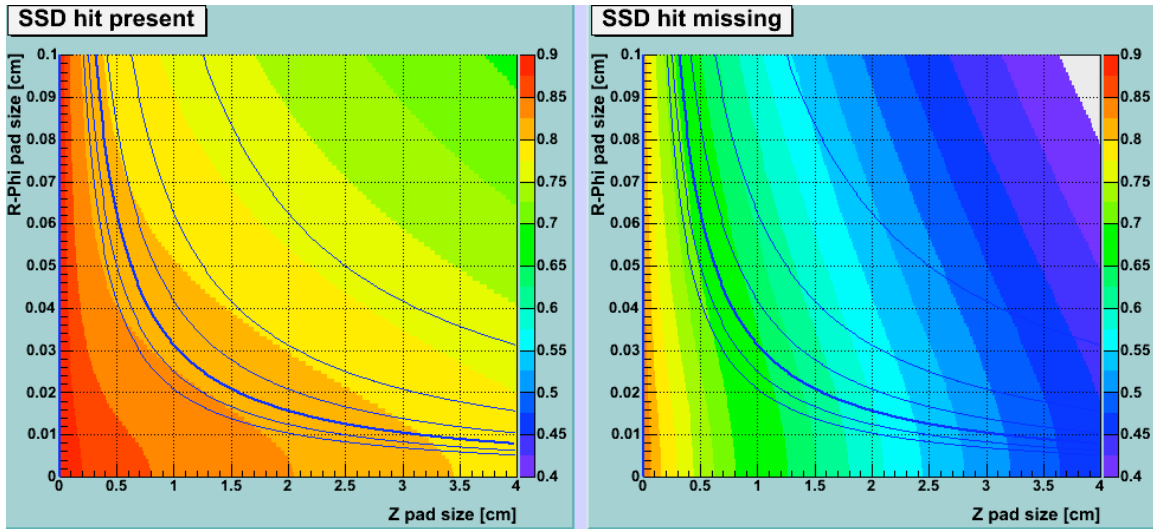
Figure 43: Single track finding efficiency for different r-phi and z pad sizes of the IST. The solid lines show the iso-lines for a certain number of channels (1=128ch, 2=256ch, 3 = 384ch, 4 = 512ch, 5 = 640ch). The left panel shows the efficiency when no hits from the SSD are included, in the right panel the SSD hits are included in the track. Particles tracked are kaons at 750 MeV/c.

The efficiency of the whole inner tracking system is determined by an intricate interplay of the detector layer radii, resolutions and thicknesses. Since these characteristics are mostly fixed for PIXEL and SSD, varying the radius of the IST barrel for a certain internal sensor geometry makes it possible to optimize the radius with respect to the single track efficiency quickly. Figure 44: Single track efficiency as a function of the IST barrel radius. The assumed internal sensor geometry was 600 μm in r-phi and 6000 μm in z. shows a calculation for a promising internal geometry. Although the dependence is rather weak it is clear that 14 cm will give the best efficiency. Not too surprising is that this is roughly halfway between the outer layer of PIXEL and the SSD.
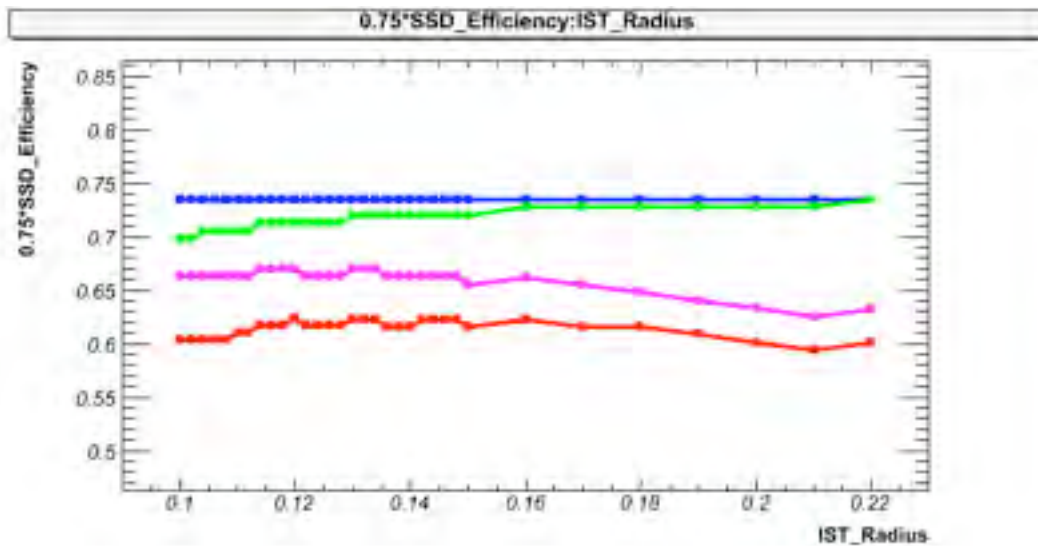
Figure 44: Single track efficiency as a function of the IST barrel radius. The assumed internal sensor geometry was 600 μm in r-phi and 6000 μm in z.

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Readout chips

The APV25-S1 chip was chosen for reading out the IST sensors because it met the requirements and was readily available. This readout chip was developed for the CMS silicon tracker which is using about 75,000 of these chips. The radiation hard production process of the APV25-S1 will enable it to withstand at least 2 orders of magnitude more radiation than is expected to be accumulated during the lifetime of the IST. The chip is fast enough to handle the RHIC interaction clock, even with multiple interactions during p+p running. Moreover, the chip was already used successfully for reading out the COMPASS triple GEM detectors and will also be used to read out the STAR Forward GEM Tracker.

Hybrids and ladders

To meet the requirement of the IST not being thicker on average than 1.5% Xo special attention has to be paid to the choice of materials for the hybrids, cables and ladders. For the cables Kapton with copper conductors was chosen. Although aluminum conductors would make the cables even lighter, they also would make them more difficult to produce and much more fragile. The radiation length requirement makes it not desirable to use a ceramic substrate, like AlN, for the hybrid. A 500 μm thick AlN substrate would already contribute 0.6% Xo while being extremely fragile. A 250 μm thick G10 substrate would only add 0.13% Xo, but still the Kapton cable would have to be connected to this hybrid. Manufacturing the hybrid and cable out of one piece of Kapton circumvents connection problems and was chosen as the most elegant solution. Since the 50 μm thick Kapton is not self-supporting a proper backing material is necessary. Using 250um thick carbon fiber would lead to a 0.11 %Xo while providing the required mechanical rigidity.

A honeycomb carbon fiber structure with carbon fiber skins was chosen for the IST ladders. These use the same construction techniques and facilities as are being used for the ATLAS silicon tracker upgrade and add about 0.4 %Xo to the IST layer, including liquid cooling. Copying the ATLAS design in the same facility greatly reduces the engineering effort and cost of the ladders. Also, since the IST ladders are only half the length (50 cm) of the ATLAS ladders, the design has become really conservative with respect to strength and gravitational sag.

Cooling

The expected heat dissipation for the IST is 12 watt per laddder, 288 watt for the whole system. Although an air cooling system probably would be able to cool the IST, it is felt that a liquid cooling system would be able to do this in a more consistent way. A liquid cooling system would add at most 0.2% Xo to the system. An air cooling duct would probably add about 0.1% Xo, but would be much less conservative in its ability to cool down the system than a liquid cooling system.

Readout system

The Forward GEM Tracker is also using APV25-S1 readout chips. However, this system will be operational 2 years before the IST. For this reason, to reduce electronic

engineering effort and to unify as many STAR readout systems as possible, the IST will try and use as much as possible of the FGT readout system. An effort is being made to design the FGT readout system such that it can be used also for the IST with as few alterations as possible.

4.3.2. The silicon pad sensors

The manufacturing techniques for silicon sensors are well established and are mastered by several manufacturers. The preference is to produce single sided devices with p-implants on n-bulk silicon and poly-silicon biased. They are relatively easy to produce with high yields and can also be handled without much difficulty in a standard semi-conductor lab. In contrast, double-sided devices have lower yields (thus more expensive) and need special equipment to handle them.

Figure 45 shows the internal layout of the IST silicon pad sensors. The active elements are arranged in such a way that the best resolution is in the bending direction, i.e. r-phi. Along the beam direction the resolution will be ten times larger. The sensors will be roughly 10 cm x 4 cm with 1024 channels. All channels are AC coupled and connected through a second metal layer to bonding pads on one long edge of the sensor. From the manufacturing point of view this design is reasonably standard. Preliminary discussions with Hamamatsu showed that they are able to produce the proposed sensors within the proposed budget.

Hamamatsu is the preferred vendor because of their excellent track record with respect to the quality of their produced sensors. This will greatly reduce the amount of quality control that has to be performed for these sensors. It will be sufficient to fully measure the characteristics of one or two samples per produced batch of about 20 sensors. Moreover, Hamamatsu uses design rules which make their sensors relatively radiation hard. Therefore, we foresee no serious performance degradation during the expected IST lifetime.
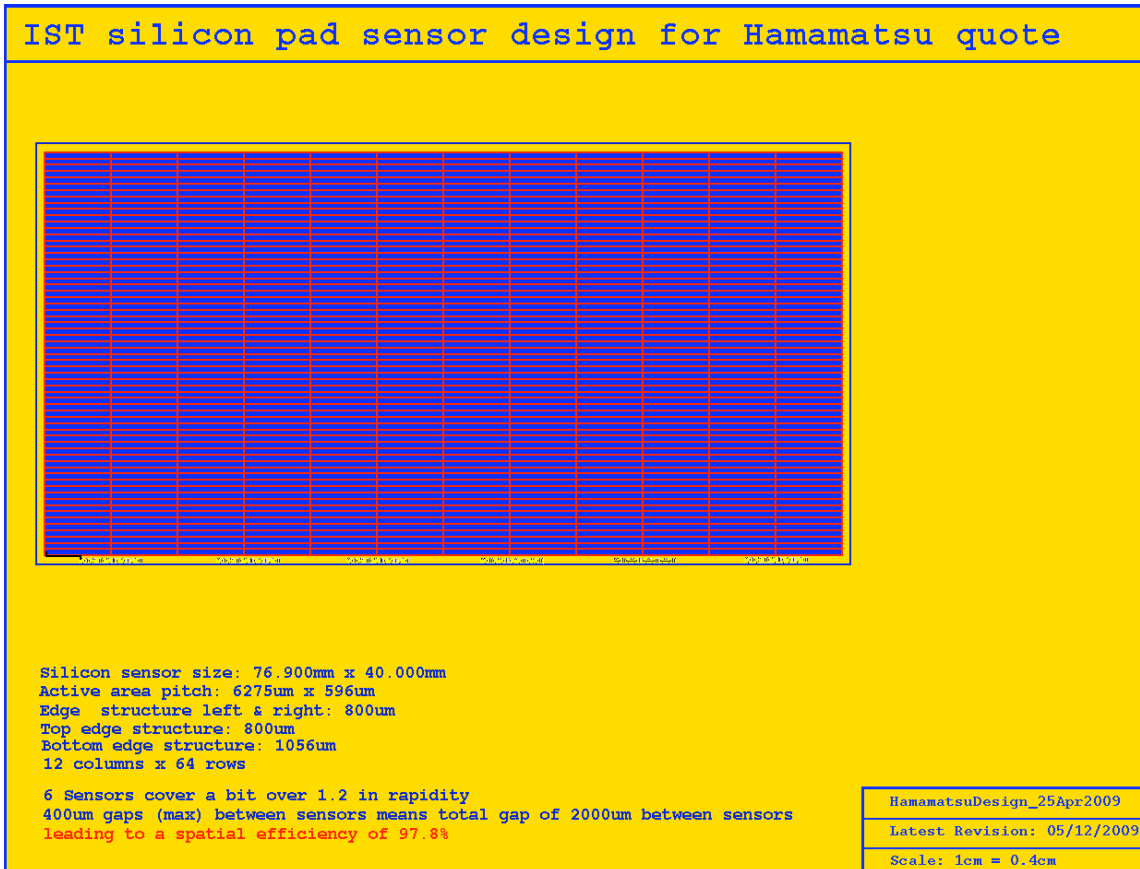
Figure 45: The silicon pad sensor internal layout.

The readout chips

About 150,000 channels will be read out in the IST. Readout chips with the necessary requirements for this system are already being used for similar purposes by other experiments. We chose the APV25-S1 readout chip which was designed for the CMS silicon tracker and of which about 75,000 will be used in CMS. Each channel of the APV25-S1 chip consists of a charge sensitive amplifier whose output signal is sampled at 40 MHz which accounts for the LHC interaction rate. The samples are stored in a 4 μs deep analog pipeline. Following the trigger the data in the pipeline can be processed by an analog circuit, mainly de-convoluting the amplifier response from the actual signal and associating the signal with a certain interaction (or rather beam crossing at LHC). The resulting analog data can then be multiplexed and sent to digitizer boards. Although the analog data lead to higher data volumes at the front-end, it is an enormous advantage that charge sharing between strips and common mode noise can be studied in detail, which greatly improves the understanding and performance of the detector. The equivalent noise charge (ENC) of the APV25-S1 depends on the capacitance of the strips and the de-convolution algorithm used, but, for our purposes, it is better than 2000 electrons. With 300 μm thick silicon sensors this will give a signal-to-noise ratio of better than 11:1 when we take the most probable energy deposition by a minimum ionizing particle (MIP). The nominal power consumption of the APV25-S1 is 2.31

mW/channel, i.e. about 0.3 watt/chip. The chips are fabricated in the radiation hard deep sub-micron (0.25 μm) process. Figure 46 shows a close-up view of the APV25-S1 chip.
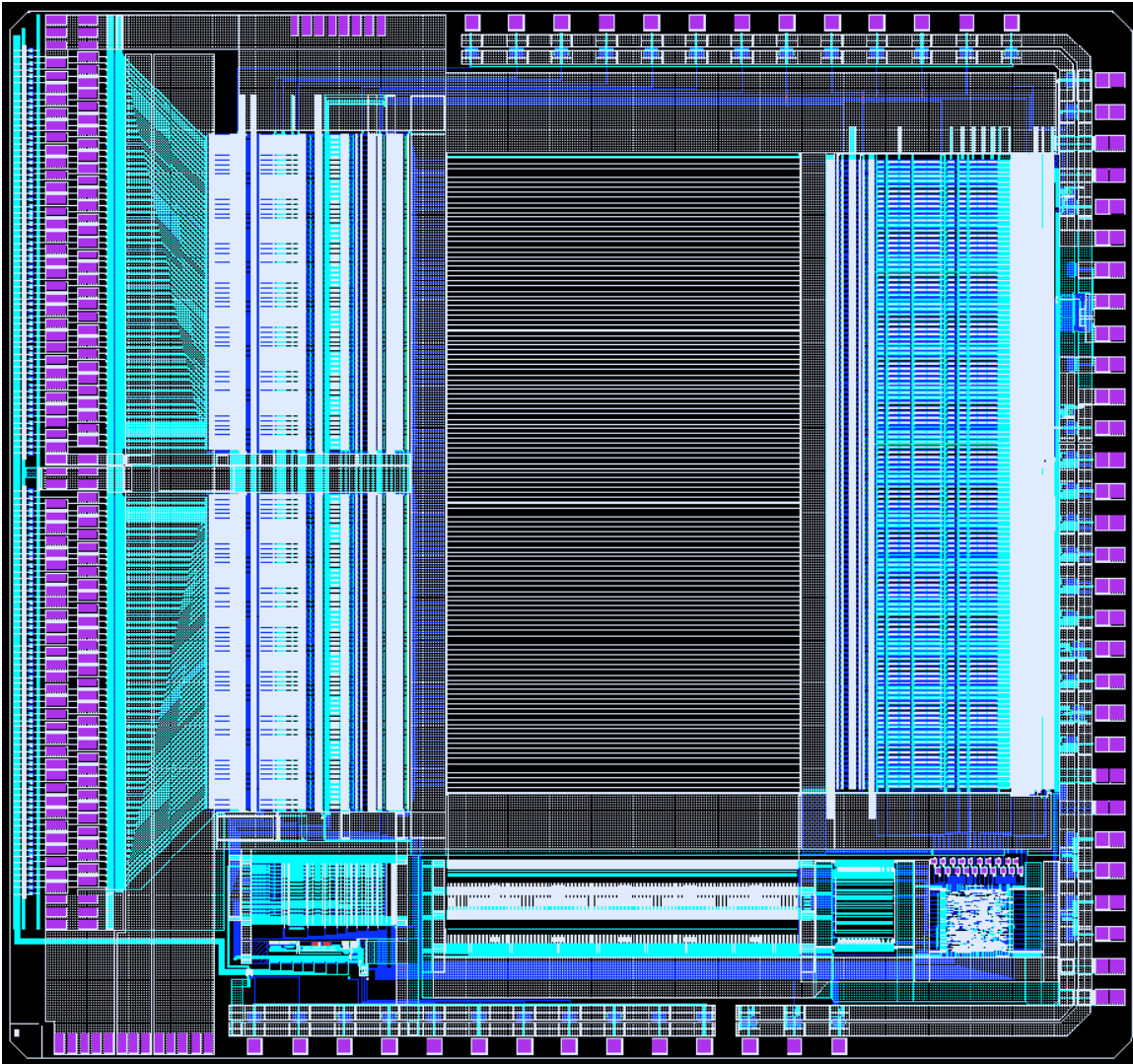
Figure 46: Close-up of the APV25-S1 chip of which the IST will use about 1200.

Hybrids and modules

To keep the material budget low the IST hybrids and modules have to constructed from low mass materials. Figure 47 shows a promising prototype Kapton hybrid design with integrated long Kapton cable. Both hybrid and cable are about 100 μm thick. The hybrid will have to be laminated onto a proper substrate material to achieve enough mechanical rigidity. Carbon-carbon and carbon fiber are being prototyped to study their mechanical and thermal properties. In the final design the flexible cable will be long enough to reach a connection to more standard cables outside the active areas which are sensitive to too much material (~100 cm). The hybrid in Figure 47 has been produced successfully and used for a prototype module, as shown in Figure 48.

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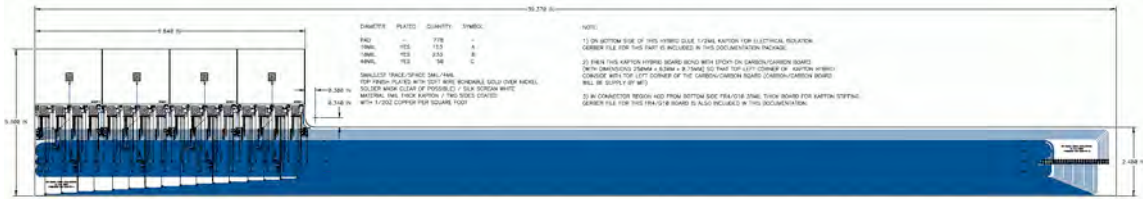
Figure 47:   IST hybrid (left) and cable (right) assembly.
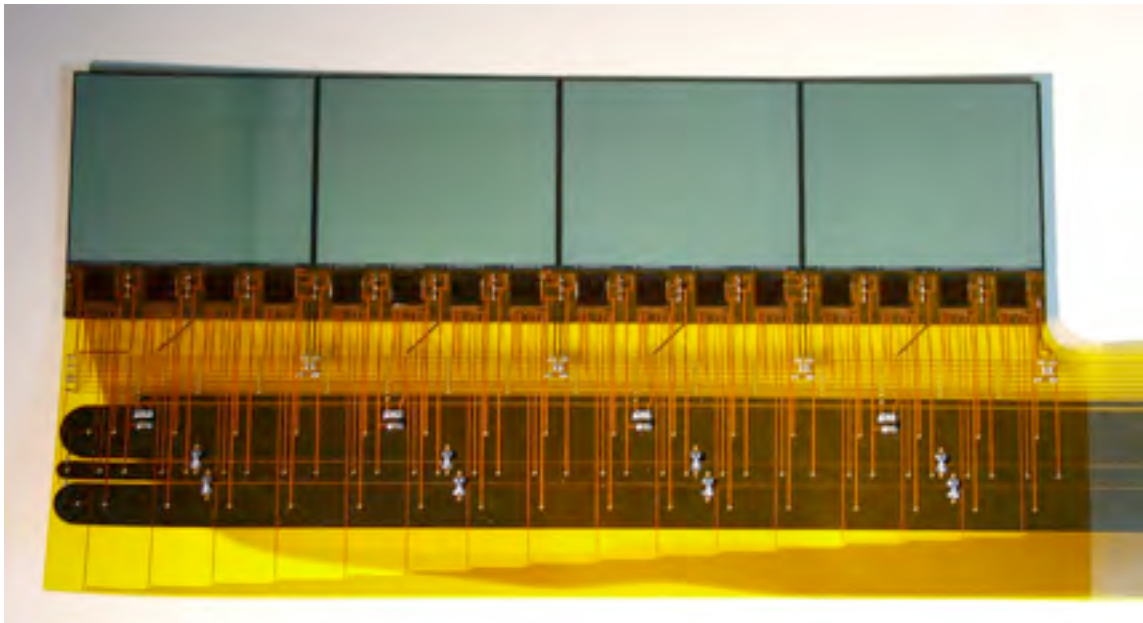
Figure 48: IST prototype with 4 Phobos IV sensors and 16 APV25-S1 readout chips.

For this prototype 4 Phobos Inner Vertex sensors were used because there were no IST prototype sensors produced yet and because the Phobos sensors are very close to the sensors which will be used in the IST. They are silicon pad sensors with 512 active elements per sensor, the elements are AC coupled to the 2nd metal signal traces that connect to the bonding pads. The Kapton hybrid was laminated to a 500 μm thick carbon-carbon substrate. All readout chips power, control and readout connections were wire bonded to the hybrid. As a first test only ¼ of the sensor elements were wire bonded to the readout chips. First tests show that the chips are functional and that the sensors are being read out as expected, as shown in Figure 49.
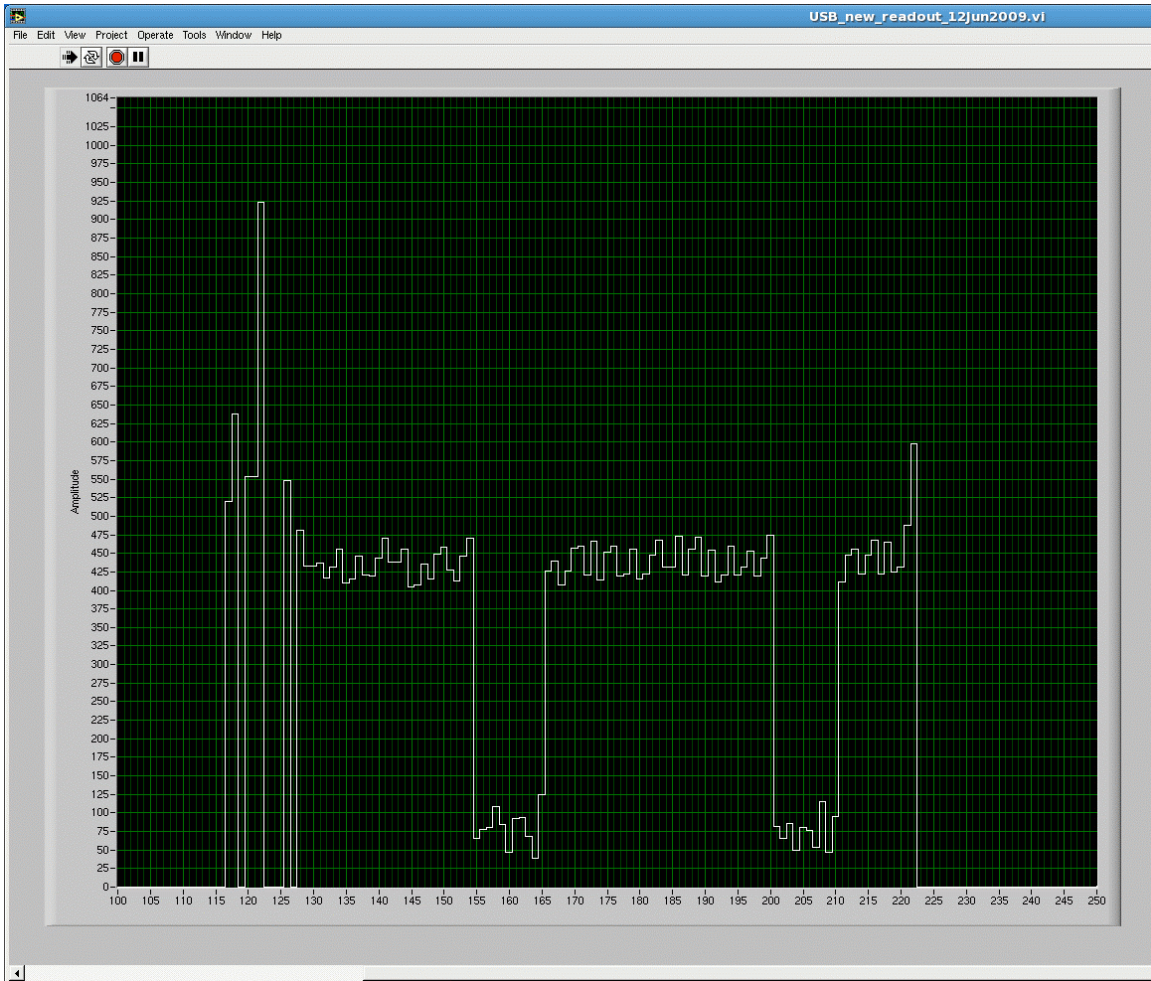
Figure 49: First readout test of the IST prototype. This plot shows the digitized output signal of an APV readout chip. The 2 'dips' are the channels connected to the silicon pad sensor.

The layout of an IST module can be seen in Figure 50. The hybrid carries 2 sensors of the type shown in Figure 54 and 12 readout chips. There will be a gap of 400 μm between the sensors. Overlapping the sensors would lead to too many assembly complications. These acceptance gaps will be compensated because of the redundancy between SSD and IST. An interesting feature, which is not visible in this picture, is that the cable will be folded over to the backside of the ladder on which this module will be mounted. In this way the cables are neatly tucked away and do not obscure visual access to the modules, which is needed for spatial survey purposes and inspection.
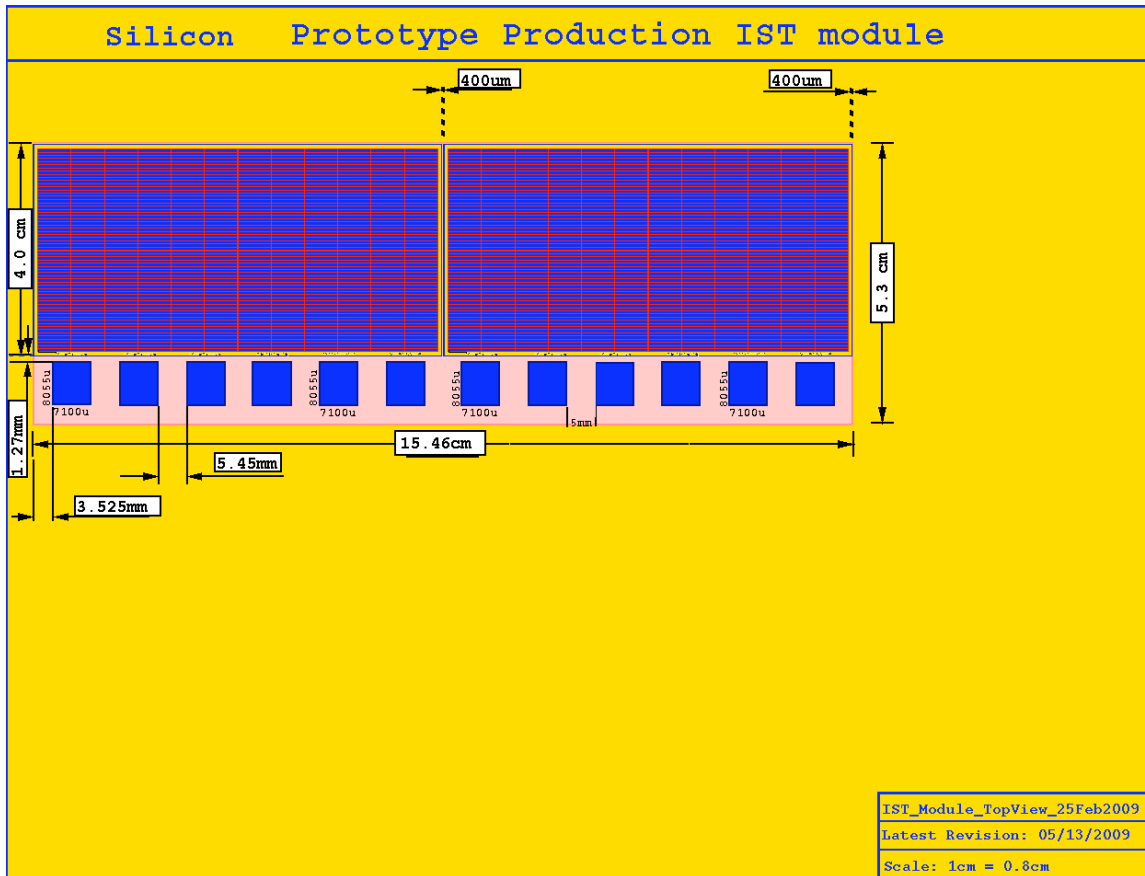
Figure 50: Layout of an IST module

Mechanical support structure

The IST barrel will consist of 24 ladders which are then mounted on a carbon fiber support cylinder. This Middle Support Cylinder (MSC) is described elsewhere in this document and has not been taken into account in the material budget.

This ladder is a shorter version of the staves which are under development for the ATLAS tracking upgrade. Because they are shorter they are even more rigid than the ATLAS staves and it is expected that their midpoint sag will be less than 100 μm when only end supports are used. A prototype ladder has been produced, as shown in Figure 51, which is being tested.

Figure 51: Long IST prototype ladder made out of carbon fiber honeycomb and carbon fiber skins. This prototype has one cooling channel.

A more detailed cross section of the ladder and mounted modules can be found in Figure 52. This design shows the 300 μm thick silicon sensor, the 300 μm thick APV25-S1 readout chip, the 100 μm thick Kapton hybrid-cable, the 500 μm thick carbon-carbon substrate and the 5 mm thick carbon fiber ladder with cooling tube. It also shows nicely how the Kapton folds over to the backside of the ladder where it is routed out to the readout system. The carbon-carbon substrate not only gives mechanical rigidity to the module, but also acts as a heat sink to transport heat from the readout chips to the cooling tube in the ladder.
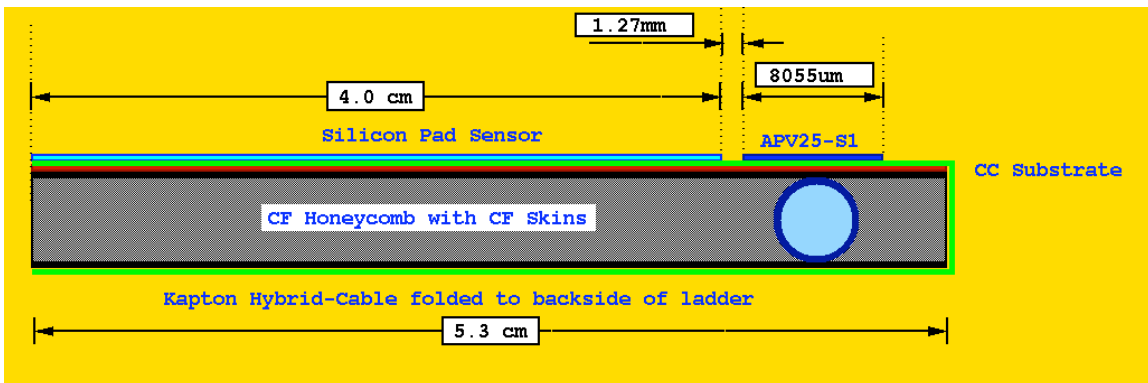
Figure 52: Cross section of the ladder and modules. Especially note the Kapton hybrid which gets folded over to the other side.

The options for mounting the ladders on the Inner Support Cylinder are still under investigation. Again it would be beneficial to profit from the extensive research that the ATLAS upgrade group has done for the upgrade staves and support. Figure 53 shows a schematic impression of one of the more promising designs. Here the ladders would be mounted with clips on the MSC. Because of the shorter length of the IST ladders it is probably sufficient to use endpoint supports only. One end of the ladder would be kept fixed while the other end allows thermal expansion. Most likely there will have to be a clamshell interface on which the ladders are mounted first. This clamshell can then be optically surveyed to determine the sensor positions before it gets mounted on the ISC.
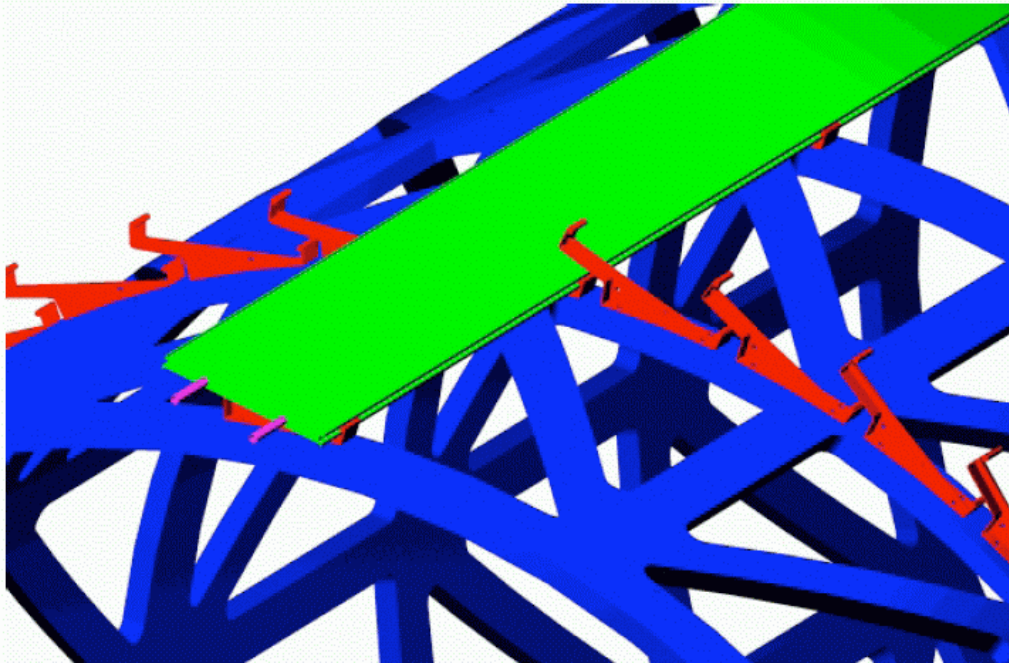
Figure 53: Ladder 'clip' mounting of the IST ladders onto the supporting cylinder (ISC).

The clip-on design has been rapid prototyped, as shown in Figure 54, and is currently under investigation.

Figure 54: Rapid prototype of the IST ladder mounting structure.

The mechanical support structure will be manufactured with an overall accuracy of 100 μm. Locally, the structure supporting the IST requires an accuracy of less than 100 μm. For instance, the mounting surfaces of the sensor modules will have to be flat to within 50 μm to avoid stress, and possibly breakage, of the sensors.
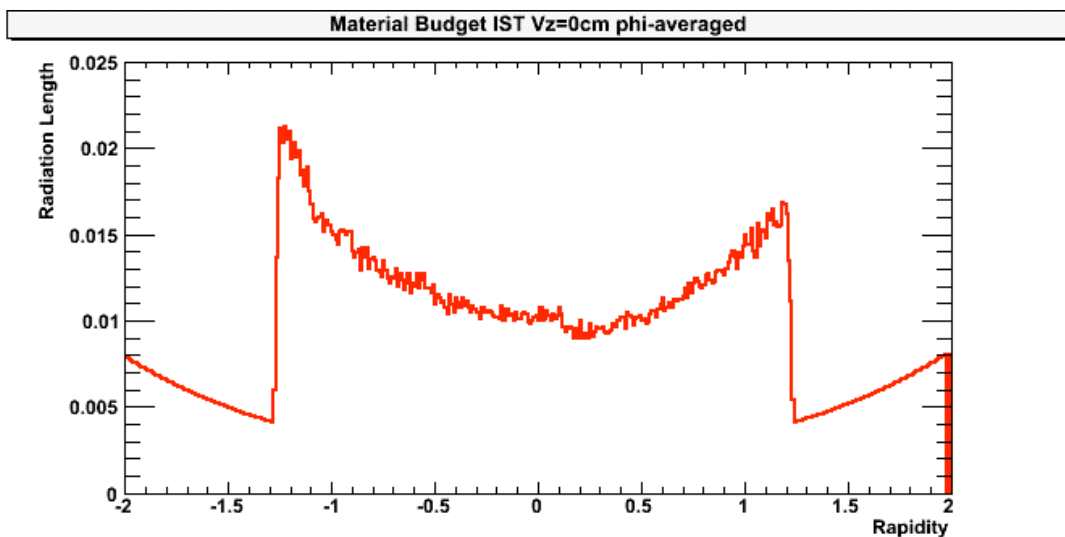
Figure 55: Phi averaged material budget for the IST as a function of rapidity.

Figure 55 gives a realistic estimate of the IST material budget by describing ladder and module designs in a GEANT geometry. These results were obtained by propagating 100,000 geantino events through the IST geometry using GEANT 3.21/08. The material budget at mid rapidity is well below the required 1.5% Xo. The MSC and support clips where not included in this calculation. The asymmetry in the material budget is caused by the Kapton readout cables only running in negative rapidity direction.

Cooling

The only source of dissipation on the ladders is the 36 APV25-S1 readout chips. Although the nominal power consumption is about 300mW per chip, the final power consumption depends on the capacitance of the attached sensor channels and the optimal settings of the chip parameters. For safety margin a maximum dissipation of 400 mW per chip is assumed. This leads to a dissipation of about 15 watt per ladder, 360 watt for the whole IST barrel. Trying to cool this with air only was considered too daunting and liquid cooling channels were incorporated in the ladder design. The 15 watt per ladder leads to about 0.6 mW per mm^2 dissipation if the heat would spread out isotropically. The placement of the cooling tube directly under the readout chips and the use of high thermal conductive material like carbon foam should make the cooling of the ladders manageable with a room temperature cooling system. Calculations making use of FloWorks and SolidWorks are underway to determine the optimal cooling configuration. Figure 56 shows a simulation for a freon cooled IST ladder incorporating a flattened cooling tube. In this picture the color coded temperature is displayed: it shows that the APV25-S1 readout chips heat up to about 89 °F (32 °C). Most of the ladder remains at about 25 °C.
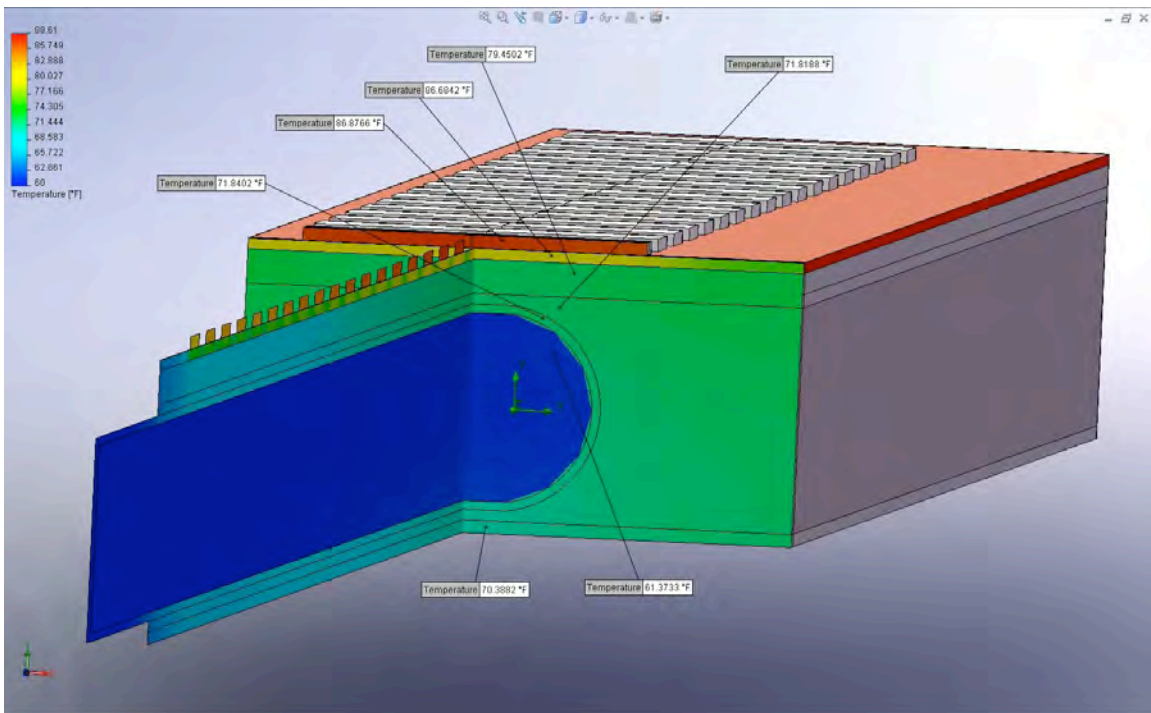
Figure 56: FloWorks simulation of a liquid cooled IST ladder.

4.3.3. Readout system and Slow Controls

Readout system and DAQ interfacing

Three modified Wiener MPOD readout crates will house the 36 read-out boards (RDO) and 6 crate controller boards (RCM). These crates, 6U in size and powered by remote supplies, will be mounted on the electronics platform next to the STAR detector. Each RDO handles two detector cables (24 APV chips), providing an ADC, some data buffering and control of APV chip triggering and readout sequencing. The RDO also operates the I2C slow controls interface to the detector. The RCM interfaces to the STAR trigger and DAQ via the ALICE detector data link (DDL) source interface units (SIU), the standard for all new STAR DAQ-connected developments for the DAQ1000, Time of Flight (TOF), Barrel (BTOW), Forward GEM Tracker (FGT) and Endcap (ETOW) tower level 2 upgrade. The readout system, as designed, will be able to transmit data to L2 following the same plans as for TOF, ETOW, FGT and BTOW. A Linux box will be located in the STAR DAQ room and fitted with the ALICE DDL receiver board and a Myrinet interface to the event builder computer. A schematic detailing these connections is shown in Figure 57.
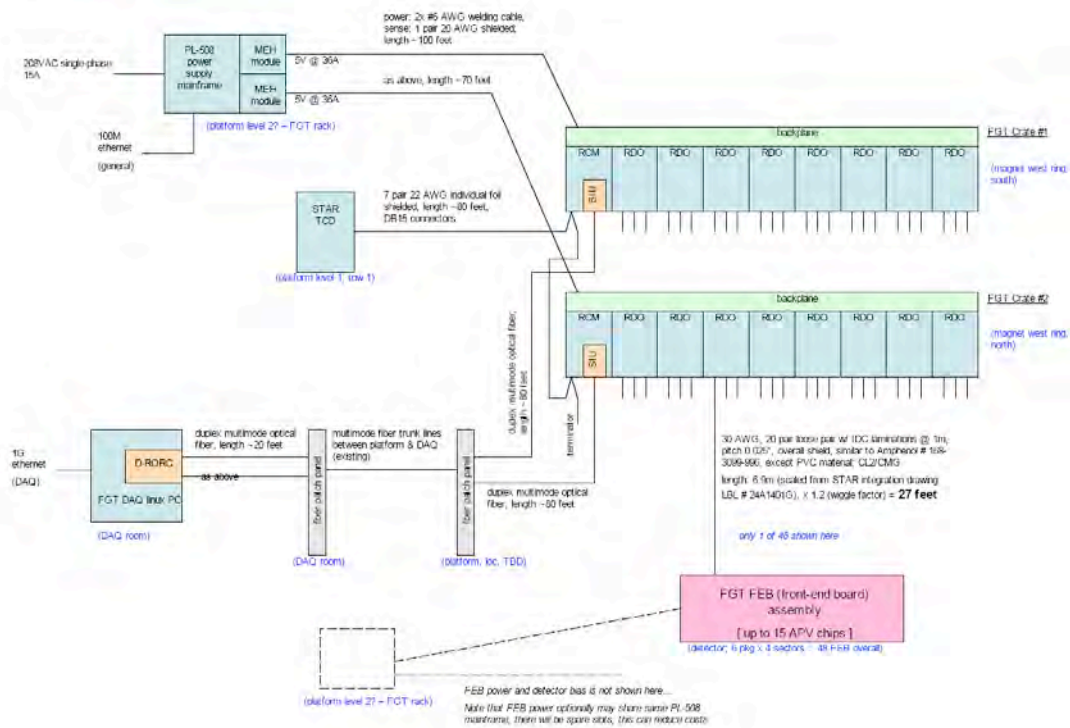
Figure 57: IST DAQ block diagram.

Slow controls system

The slow controls system will serve as the primary means for controlling and monitoring the working parameters of the IST. These parameters, such as the hybrid temperature, component currents, voltages and gas flow rates, will be interfaced with the standard STAR alarm system. The alarm system logs the parameter history and alerts the shift

crew if operating limits are exceeded. The black dashed lines in Figure 58 show the communication flow between the slow controls computer and the hardware being controlled. The red solid lines represent the actual hardware connections which allow this communication. The slow controls for the IST detector and readout crates will be handled exclusively by Ethernet traffic to the IST Linux box, through the ALICE DDL link to the readout crates, and then finally through the RDOs to the APV's via the local I2C link. There will be no other hardware needed for slow controls. All power supplies will be fitted with an Ethernet controls interface.

Although STAR is using EPICS as its standard slow control system there is a slight preference to use LabView instead. LabView provides the user with virtually any instrument driver and a very convenient user interface. LabView runs on both Windows and Linux. It is relatively simple to interface LabView and EPICS. However, at the moment, both options are still open.
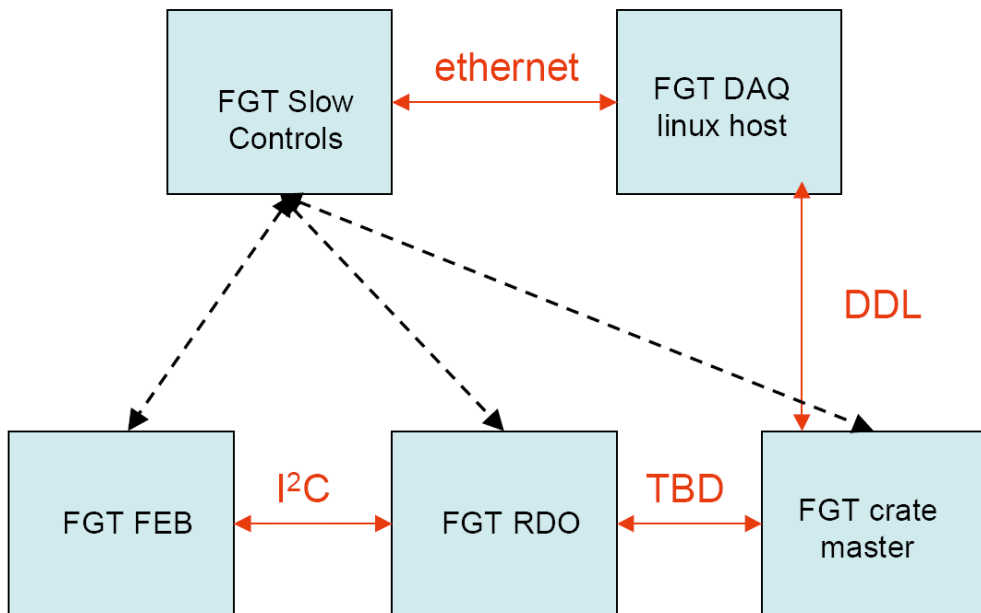
Figure 58: IST slow controls flow diagram.

4.3.4. Spatial survey and alignment

The IST will have to be aligned with respect to the other detector in the inner tracking upgrade, PIXEL and SSD. The final alignment will be done with tracks through an iterative residual method. However, for this method to be successful it is important that the positions of the active elements are known in advance with an accuracy comparable to the resolution of the detectors. For the IST the following 5-step plan can achieve this:

The positions of the sensors on the module have to be determined. Internally the structure of the sensors will be well known with an accuracy of about 1-2 μm. This information is obtained through the production mask drawings of the sensors and

accessed through alignment marks on the sensors. The modules will be build on an assembly machine under control of an operator checking the process under a microscope. The expected placing accuracy is 5 μm. After the modules have been assembled they can be surveyed with an optical survey machine at MIT. The accuracy of this machine is about 10 μm in-plane. An out-of-plane contrast measurement leads to an accuracy of 50 to 100 μm.

The same methods used for the module will be used for the ladders. Three modules will be glued to one ladder with an accuracy of about 5um. Then the ladder will be optically surveyed with an in-plane accuracy of 10 μm and an out-of-plane accuracy of 50 to 100 μm. After the ladder is approved it will be shipped to BNL where an additional survey can take place. There is a possibility to do this on a coordinate measuring machine and/or by the BNL surveying group using state-of-the-art optical survey equipment.

At BNL the ladders will probably be put together in 2 clamshell cylinders which can be measured on a coordinate measuring machine or by the BNL survey group. After the clamshells have been put together on the ISC to form the IST barrel another survey needs to take place. Up to this point it should be possible to survey the silicon sensors themselves. The sensors have the highest internal accuracy (1-2 μm) and in the end it is their position which should be known with the best accuracy. However, after the clamshell has been closed visual access to the sensors will become impossible, especially after the ISC gets integrated with the rest of the inner tracking system. It is important to have survey points on the ladders, the clamshell structure and the ISC which are visible to the BNL survey group. These survey points then 'anchor' the IST inside the inner tracking system and finally to the whole STAR detector. It is extremely important that the BNL survey group is involved from the beginning in planning the whole survey process.

Finally, the inner tracking system (PIXEL, IST and SSD) will be mounted inside the STAR TPC. Its location will be determined by the BNL surveyors through optical survey.

All the information which has been gathered in the previous steps will be used to do a least squares fit for the positions of the IST silicon sensors. Since there are only 144 sensors it will be possible to do some hand checking and possible correction of the results. These positions will then go into the STAR tracking geometry and act as a starting point for software alignment with tracks. This final process can easily take a couple of person-months to achieve the desired level of confidence. Therefore, every effort should be made to have a sufficiently rigid construction. Removal of the detector will set a physics analysis back by months and should not be undertaken lightly.

4.4.   The Silicon Strip Detector

The STAR Silicon Strip Detector, SSD,[33] is a high resolution silicon detector that is mounted inside the inner field cage wall of the STAR TPC at a radius of 23 cm. Its radial location puts it midway between the event vertex and the first active row of the TPC.

Thus, it is ideally suited for the purpose of improving the TPC's pointing and momentum resolution.

The SSD was designed to work with the TPC and the STAR Silicon Vertex Tracker (SVT). The design read-out frequency of the SSD is 300 Hz. This does not meet the HFT read-out frequency requirement of at least 1 kHz. Therefore, the read-out electronics needs to be upgraded. The existing silicon detector wafers and the ladder structure will be kept and the read-out cards will be replaced. The upgrade also will require new cabling, cooling, and mounts.

This chapter describes the existing detector ladders and the plans to build new read-out electronics, a new mount, and services for the SSD.

4.4.1.   The SSD Barrel

The SSD barrel is composed of 20 individual ladders. The ladders are made of carbon fiber and each ladder supports 16 detector modules (see Figure 59). Each of these modules is composed of one double-sided silicon strip detector and two hybrid circuits equipped with analogue readout electronics. On both ends of a ladder, two electronics boards are used to control the detector modules and convert the analog signal from the Si wafers into a digital signal, which is then sent to readout boards that are located on the STAR south platform.
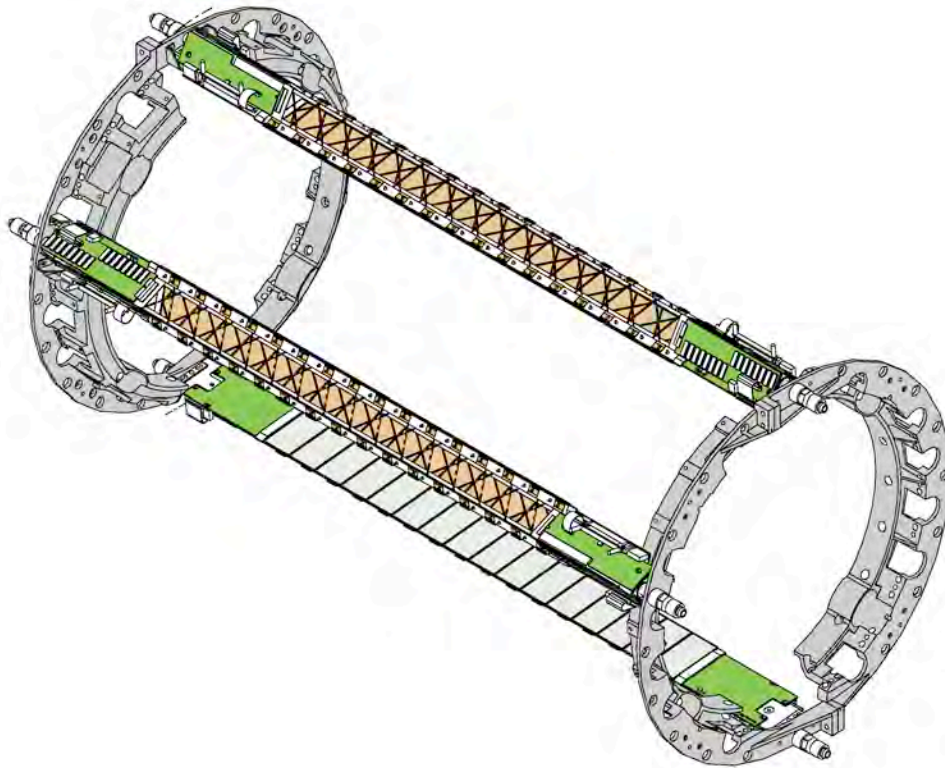
Figure 59: Three ladders shown attached to the old SSD support rings.

One ladder is shown, in detail, in Figure 60. In the new electronics, two cable busses (one per side of the Si wafers) will transport the analog signals along the ladder to a pair

of ADC boards, where the signals from the 16 wafers will be digitized concurrently. After digitization, the signals are sent via optical fiber links to the Readout Boards, which are in turn linked to the DAQ system through Giga-link optical fibers.
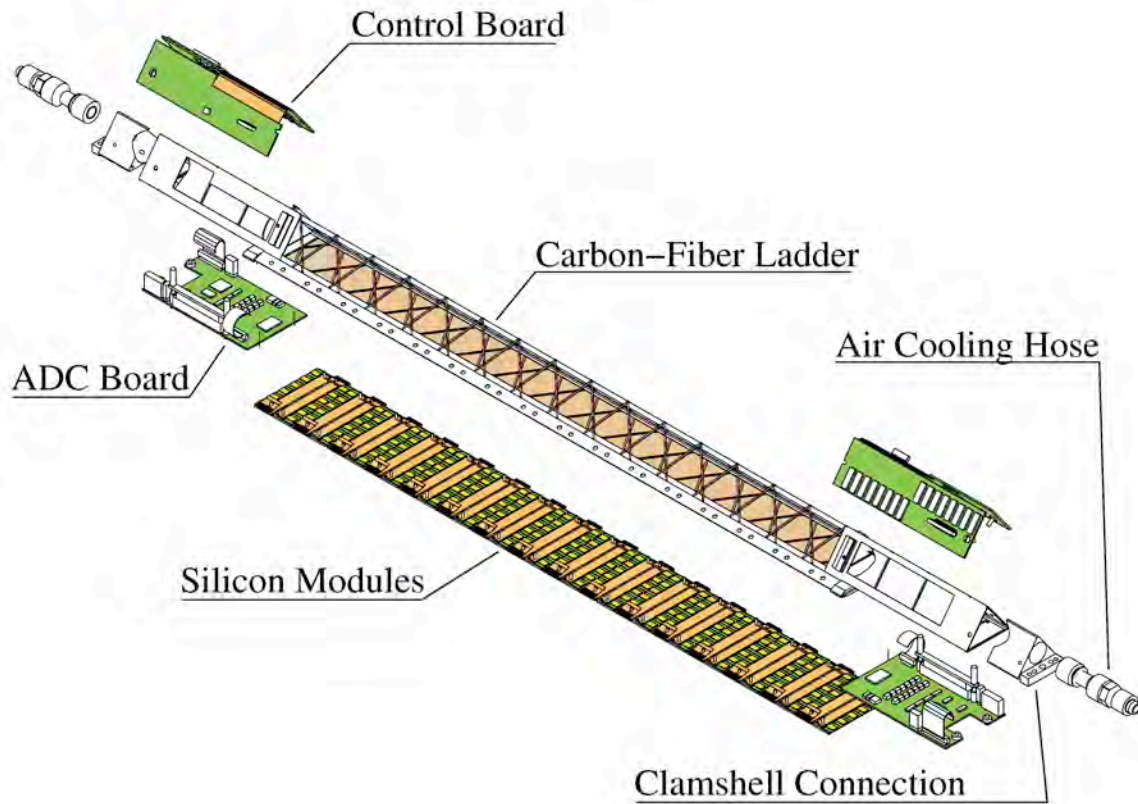
Figure 60: A SSD ladder showing its various components.

A detector module is the basic element of the SSD and it integrates a silicon wafer with its front-end electronics. One detector module is shown in Figure 61. Each module is composed of a silicon detector and two hybrid circuits. A silicon strip detector measures 42 mm by 75 mm and it is doubled sides with 768 strips on each side of the detector. The strips have a pitch of 95 mm, and are crossed with a 35 mrad stereo angle between the strips on the P and N side of the silicon.

The two hybrid circuits are built on top of a flexible circuit made of Kapton and copper, which are, in turn, glued to a carbon fiber stiffener. The circuitry includes 6 analog readout chips (the ALICE 128C) and approximately 50 SMD components (resistors and capacitors).
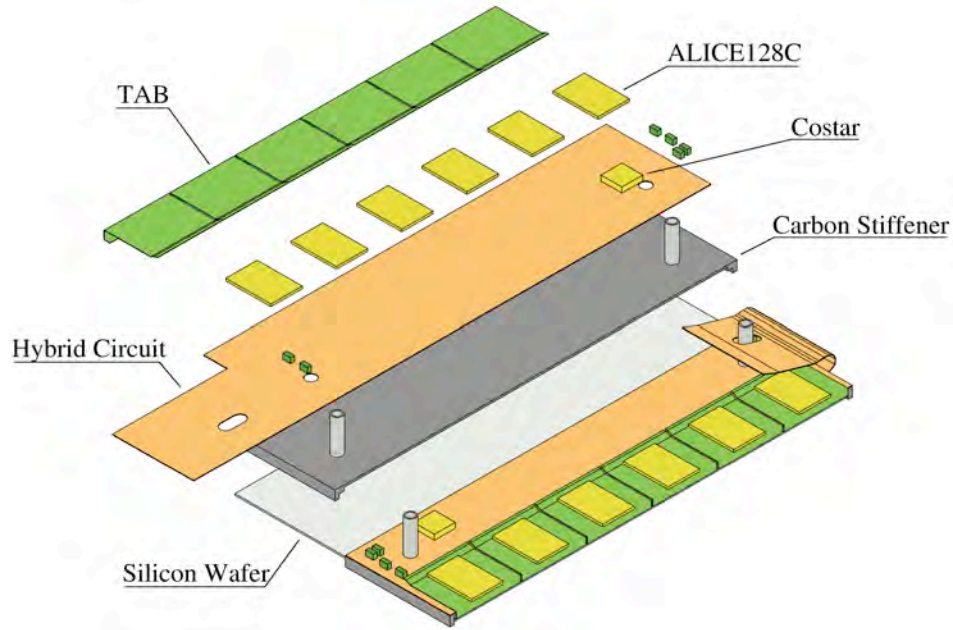
Figure 61: Exploded view of one detector module. It takes 16 modules to fill a ladder. The module is read out on each end by a Ladder Board

4.4.2.   SSD electronic upgrade

A Ladder Board reads each detector modules in parallel. Figure 62 shows the block diagram of the ladder board and the RDO. The optical connection is bidirectional; the second fiber runs at a reduced clock rate, as its purpose is to provide slow control information to the FPGA on the ladder board, which manages the analog circuitry on the ladder.
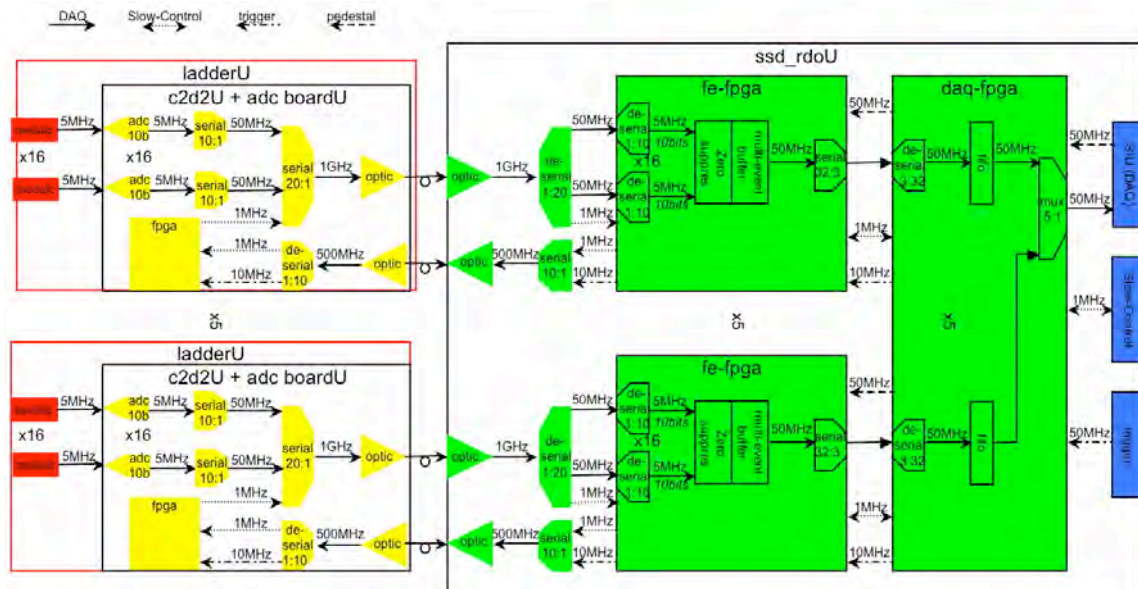
Figure 62: A schematic of the interconnection between the ladder electronics and the RDO card, Each RDO handles 5 ladders. The connection between the ladder electronics and the corresponding RDO card is a dual optical fiber.

Ladder Board

Every module on the SSD ladder will have its own ADC, so 16 ADC channels are needed. We will use 8 Analog Devices AD7356 dual ADC chips. Each chip contains two independent ADCs with 5 MHz sampling rate and a bit-serial output. The serial output produces a 14-bit pulse train, of which only 10 bits are used in this application. The outputs of these 16 ADC channels are sent to the inputs of a parallel-serial converter, along with the slow control output of the FPGA. The parallel signals are clocked in to the serial converter at a 40 MHz rate, resulting in a 1.4 Gbps pulse train, which is converted to optical and transmitted to one of the 5 inputs of the RDO board. The optical nature of this connection allows the RDO crate to be relocated outside the STAR magnet.

RDO Board

Each readout card accepts the fiber link from five ladders. A readout card is connected to the DAQ SSD PC by a DDL fiber link (50 MHz × 32 bit = 1.6 Gb/s or 40 MHz × 32 bit = 1.28 Gb/s) identical to those in use in the TPX. Eight readout cards (four for each SSD side) reside in a 6U VME crate; there are, therefore, 8 fibers connecting the readout crates to the DAQ computer. The DDL links, together with their source interface to the SSD RDO (SIU board) and the PCI-X card residing in the SSD DAQ PC (D-RORC board), are readily available for purchase.

At the RDO card, the 1.4 Gbps bit train is converted by a deserializer to a 20-bit wide data path, which is updated at a 40 MHz rate. Twenty of the 24 bits produced by the deserializer are reshaped into a 50 MHz stream of 16 bits width and delivered to a second bank of 16 1:10 deserializers, resulting in 16 10-bit wide replicas of the original ADC values produced on the ADC card. (The remaining 4 bits are used for the slow control

function.) This second bank of deserializers is contained in an array of 5 FPGAs, each one dedicated to the data delivered by the fiber from a single ADC card. These FE-FPGAs perform zero suppression and multi-event buffering on the 16 data streams produced in the last bank of deserializers.

The multi-event buffers and zero suppression both provide a means to reduce dead time due to data burden on the DDL optical fiber. Zero suppression is carried out in the simplest possible way – the ADC value for each strip is compared with a stored pedestal value corresponding to that strip. If the ADC value exceeds the pedestal, the strip number and ADC value are encoded into a 32-bit word and entered into the multi-event buffer.

The multi-event buffers are provided as a second means of reducing dead time. Simulation has shown that for randomly spaced triggers 4 buffers can keep the dead time to about 7 per cent for a trigger rate of 1 kHz. We expect about 3% of the strips to be hit in a central Au-Au event.

There is sufficient on-chip RAM storage in the FE-FPGAs to implement buffers for 4 events that have not been zero-suppressed. In zero-suppressed mode, these buffers can be coalesced into a single event buffer large enough to handle largest zero-suppressed event. It is expected that the operator will monitor ladder occupancy. When a ladder is observed to be producing large zero-suppressed events, the offending module will be masked off.

The ladders are read out by passing a token to the chain of 6 ALICE128 analog multiplexers handling the analog signals corresponding to the 768 strips of a single module. Once this process has started, it must continue until the token reappears, at the end of 768 clock cycles. In the event of an abort arrival, the clock speed will be doubled in order to minimize the time consumed by this process.

Services

The electronics will be located on the South platform, where space is readily available. A VME crate will contain both the RDO cards and the Slow Control communication interface.

The 8 SSD readout cards require 8 DDL fiber links to DAQ PCs. Each DDL receiver card (DRORC) handles two fibers; thus, 4 DRORC cards are required to provide the necessary interface. This is best implemented in 2 PCs, each with 2 DRORCs. Each PC will be responsible for one-half of the SSD.

The Slow-Control information to and from the ladders travels over the optical fibers to the readout cards The SSD Slow-Control interface consist of two independent JTAG chains: the Slow-Control chain and the FPGA configuration chain. To minimize the changes in the Slow-Control system software, we will have 2 RDO boards connected to each Slow-Control cable. The transport on optical fiber between RDO and ADC boards is completely transparent to all the components that have to decode and answer to the JTAG orders.

Each of the 8 readout cards has its interface to the SSD trigger TCD. The interface will reflect the updated definition of the TCD (still in progress), if this definition is finalized in time. The functionality of the trigger interface remains unchanged from the present system except that it will use both the 10 MHz and the 50 MHz clocks instead of creating the 50 MHz onboard.

4.4.3. Cooling System – Requirements, Status and Upgrade

The evacuation of heat produced by the electronics in the SSD is critical in order to establish stable behavior with the sensors and the associated electronics. The power consumption of the different components of the SSD ladders can be separated into two independent parts: The first part is due to the Front End Electronics (Alice 128C) chips, and the second part to the Ladder Boards. (The Si detector modules do not contribute substantially to the power consumption budget.)

The ADC chips selected for the ladders consume very little power (14 mA @ 2.5 V). Taking into account the remaining components: including the FPGA, the serializer, deserializer, and optical transmitter and receiver, each ladder's end electronics is expected to consume less than 2W. The existing ADC and Connection boards dissipate approximately 5 W per ladder end, with an additional 10 W dissipated by the Si modules, hybrid, and costar chip. So the estimated dissipation for a full ladder is expected to be 14 W compared with 20 W for the existing system.

Table 9 shows an initial estimate, and the final measurement, of the power used by the FEE.

FEE POWER	Number of elements	Predicted Power	Measured Power
Alice 128	12 per module	44 mW	
COSTAR	2 per module	44 mW	
Detection Module	16 per ladder	616 mW	
TOTAL FEE		**9.8 W**	**10 W**

Table 9: Estimated and measured power used by the FEE for the previous SSD electronics.

Table 10 presents power consumption estimates for the electronics and results of measurements for the existing electronics for the Ladder Boards.

Electronics Boards	Number of elements	Predicted power (old)	Predicted power	Measured power (old)
Ladder Board	2/Ladder	5 W/card	2 W/card	
Total from Boards		**10 W**	**4 W**	**10 W**

Table 10: Estimated and measured power for the new Ladder Board.

Table 11 summarizes the power consumed by the FEE electronics and the electronics boards on both ends of each ladder.

	Old	New
Total FEE	10 W	10 W
Total Electronic Boards	10 W	4 W
Total per ladder	**20 W**	**14 W**

Table 11: Estimated power consumption for a ladder

Given the low power dissipation per unit area in the detection surface (~20 mW/cm^2), a cooling system using air was developed and designed for the SSD. For the two ends of a ladder (Ladder Board) the problem is different: the density of released energy per unit area is 4 times bigger than for the FEE. Fortunately, this zone is not in direct view of the silicon modules.

The air path in the ladders

Each ladder is cooled by air circulating throughout the carbon fiber structure and, in effect, the ladder functions as an air pipe. So each ladder is wrapped in a thin Mylar film to guide the air. The electronic boards are installed on the ladder ends with the components pointing inwards and 'seeing' the inside of the triangular section. Deflectors inserted inside the ladder help guide the air to the warmest components.

The flow of air is driven by an external vacuum system so that air is pulled through the ladders and the heated air is removed from the central part of the STAR detector. The input air comes from IFC, which contains the free volume between the SSD and the TPC. The warm air is then evacuated to the outside of STAR through a flexible hose of approximately 10-mm diameter.

Requirements and Functionality Tests

Cooling the electronics is an essential task to maintain the performance of the detector. The Si detectors and the ADC boards become unstable when they get too hot. For example, during RHIC Runs 6 and 7, the SSD ladders routinely shutdown when they reached a temperature between 45°C and 50°C. The exact temperature that the modules shutdown depended on the location and ladder number, but the primary reason for the shutdown was that the noise on the chip increased as it got hotter. As the noise went up, the HV had to be raised to get a bigger signal. Increasing the HV caused higher leakage currents and eventually the leakage current went above the limit of the HV power supply and the system tripped off. So experience has shown that the SSD electronics should be maintained at 35°C to 40°C; and pushing above 40°C is very dangerous.

The SSD design team has done a series of thermal tests on a ladder to see how it will perform under various conditions. Table 12 shows the temperature inside the ladder at a few critical points when the cooling system is off. The maximum temperature measured was 46.5°C. These tests were done at an ambient temperature of 19°C whereas the average temperature inside the IFC of the TPC during Runs 6 and 7 was 24°C. Thus, you would expect a global shift of 5°C in the actual STAR Environment.

	SIDE P (°C)	SIDE N (°C)
ADC	42.8	46.5
Control Board FPGA	34.8	36.5
Connection Board	45.2	45.4

Table 12: Mean electronics temperatures measured on the test ladders with cooling off. The ambient air temperature was 19°C.

Table 13 shows the temperature distribution at the critical points with the cooling 'on'. Once again, it is worth noting that these temperatures were recorded using input air at 19°C. In the actual STAR environment, the input air is drawn from the IFC and the air in this region typically has a temperature of 24°C. It would be highly desirable to lower the IFC air temperature to 20°C to 22°C in order to provide a small safety margin for the SSD and the other silicon detectors.

	SIDE P (°C)	SIDE N (°C)
ADC	33.1	33.2
Control Board FPGA	33.7	30.7
Connection Board	27.6	24.5

Table 13: Mean electronics temperatures measured on the test ladder with cooling on. The ambient air temperature and input air temperature was 19°C.

Additional temperature measurements were performed at various points along the ladder and these results are shown in Table 14. Between modules 8 and 11 (in the middle of the ladder), the temperature goes above 37°C' even when the cooling system is on.

Module	Si Temperature (°C)	COSTAR Temperature (°C)
3P	27.8	35.3
5P	32.9	32.5
8P	30.9	37
11P	30.2	37.5
14P	28.7	34.9
16P	25.1	32.3

Table 14: Mean Temperatures measured at various points along the test ladder with the cooling system turned on. The column on the left identifies the wafer number (1-16).

Cooling System Summary and Upgrade Plans

A vacuum driven cooling system can maintain the temperature on the SSD ladders to between 32°C and 37°C if the input air temperature is kept below 20°C. The silicon detector temperatures are held below 31°C under these conditions and the wafer leakage currents are reasonable. The leakage currents increase with the wafer temperature but this has a minor impact in terms of electronic noise if we stay out of the danger zone above 40°C.

However, these tests were made with the incoming air held at 19°C while in STAR the IFC air temperature is around 24°C. This means that we should expect a global temperature shift of the same order for these tests results and this is consistent with our observations in Runs 6 and 7. It is highly desirable to lower the IFC temperature to 20°C to 22°C in order to provide a large margin of safety for the Si detectors.

We will engineer a new system that uses hard-covered hoses or alternatively a hard covered plenum to deliver the air to the SSD. In addition, the source of vacuum also needs an upgrade because the existing Vortex system is complex, prone to failure, and expensive. It consumes 76 kW of power.

A cheaper and more reliable system is available. The wood working industry needs high volume vacuum sources to clear wood chips from around saws and lathes. Thus, there is a commercial line of vacuum supplies that provide vacuum with the flow and pressures that we need. These vacuum supplies can be purchased, off the shelf, and run on 120 VAC or 240 VAC. Specifications for a suitable choice can be found in Table 15.

Specifications	RP-212-EL	RP-426-QL	RP-546-QL
Input Voltage	230 VAC 1	230/460 VAC 3	230/460 VAC 3
Power Consumption	1.2 kW	2.6 kW	4.6 kW
Maximum Airflow	100 CFM	150 CFM	225 CFM
Max Static Pressure	110 in. H_2O	105 in. H_2O	130 in. H_2O
Tank Capacity	15 Gal	12 Gal	30 Gal

Table 15: A typical vacuum system from *Dust Collection and Vacuum Systems, Inc.*

A three-phase system is highly desirable because a 3-phase motor does not require brushes and so is capable of continuous operation over a very long period of time. We will mount the vacuum system on the North Platform (dirty power side) and provide vacuum to the SSD via non-conducting plastic pipes. The precise details on how to route the pipe, and divide the airflow so that it reaches each ladder are still to be determined.

4.4.4. SSD Ladder Status

The SSD detector was used last during Run 7. At the beginning of the run, several ladders were known to be inoperable. Due to hardware issues, two ladders did not provide useful data and were turned off at the beginning of the run. Four other ladders were not stable when they were operated at the nominal HV configuration. They needed to be operated at a lower voltage and therefore were less efficient. During the run, it was determined that there was inadequate cooling to several ladders. Upon inspection after the run, several bent cooling hoses were found and are the probable cause of the ladder's overheating and instabilities. When the SSD is upgraded, the cooling system will be re-designed so that this problem cannot reoccur.

After Run 7, the SSD was removed and returned to Subatech Laboratory in Nantes. There the engineers tested each ladder and made a few repairs.

Among the 22 ladders (the 20 ladders that compose the SSD and 2 spare ladders), there are 6 perfect ladders; the others have flaws of various kinds. Eleven ladders have a few hybrid circuits that cannot be fully tested with the Subatech test bench. However the data acquired with these hybrid circuits may be completely usable. It was observed during the last data taking at STAR, that most of them produce good data. Nevertheless, due to some cooling failures and to reduce the heat load, a few of the hybrid circuits were turned off.

At this time, it is not possible to give a definitive status of these hybrid circuits. However, a software upgrade is planned to enable testing of these circuits. For a conservative estimate, we assume these hybrid circuits are bad. Using these assumptions, we obtain:

- 7 ladders with one hybrid circuit (out of 32 per ladder) not fully tested,

- 1 ladder with 2 hybrid circuits not fully tested,

- 2 ladders with 3 hybrid circuits not fully tested, and

- 1 ladder with 8 hybrid circuits not fully tested. (This was the first ladder produced so assembly techniques evolved during its assembly.)

In addition, a few inoperable hybrid circuits have been identified in five ladders. During data acquisition, these hybrids circuits had to be bypassed and thus did not provide data.

- One ladder had two partially damaged hybrids. One hybrid circuit had one chip (out of 6) dead. The other chip had 5 out of 6 chips damaged. This results in an effective inactive area of one hybrid.

- One ladder with 1 dead hybrid circuit and 2 not fully tested hybrid circuits. If the 2 not fully tested hybrids are considered as bad, this leads to an electronic coverage of 91% and for data use 81%. It is worthwhile to mention that the two hybrids could provide good data but have not been checked yet.

- Three ladders, known to have frequent HV trip during data taking, have been diagnosed to have some of the modules/hybrid circuits that cause a high leakage current. In that state, the culprit hybrid circuits are disconnected. This means we can use 1 ladder with 2 hybrid circuits off, another ladder can also be used with 4 hybrid circuits turned off, and the last ladder is operational with 2 modules turned off. In addition, some chips are missing (5 in total) and 1 hybrid circuit is not operational.

A repair of the four ladders with excess HV was studied. Thermal images of a hybrid circuit with high leakage current found one of the capacitors hotter than the others. The capacitor was then carefully removed from the circuit. When the ladders was retested, the leakage current returned to their nominal current. After the success of the first repair, this procedure was repeated with the other three high current ladders. All of the repairs were a success and now all of these ladders are working.

Figure 63 shows a summary of the current status of the best twenty-one ladders. It assumes that the hybrid circuits that cannot be fully tested are bad. This figure shows the *lower limit of the active coverage*. The red marker represents the electronic coverage for each ladder. Since the SSD tracking software has been designed to use both the p and n side to determine a particle's position, one single side hybrid failure will result in the whole module being declared unusable. The blue triangle marker in Figure 63 shows the active area taking into account this effect. The average coverage, 94%, is represented by the blue dotted line.

It is worthwhile to note that only one side of the module can detect a particle when the other hybrid of the module is not operational. This change would degrade the spatial resolution, but it would increase the spatial coverage to 99%. Preliminary studies indicate it is possible only to use one side of module for STAR tracking.
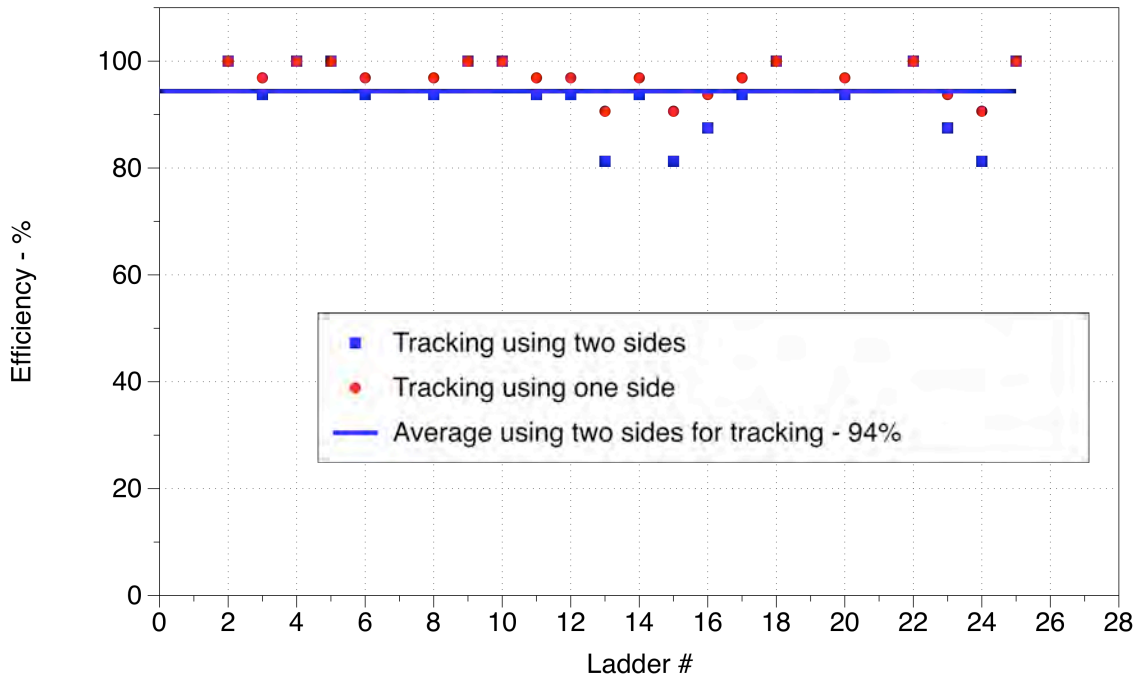
Figure 63: A plot of the efficiency for the existing 21 ladders. The blue points assume that both the n and p side are needed in tracking. The red points are for the case when either side is used.

4.4.5.   Alignment Mounts on the Cone

The SSD is attached to the existing cone by four mechanical pieces at each end of the barrel (Figure 64). Those parts allow a geometrical adjustment to position the SSD concentrically with the IST and PIXEL. These pieces are equipped with screws to adjust the SSD. The new cone will use the existing fixtures.
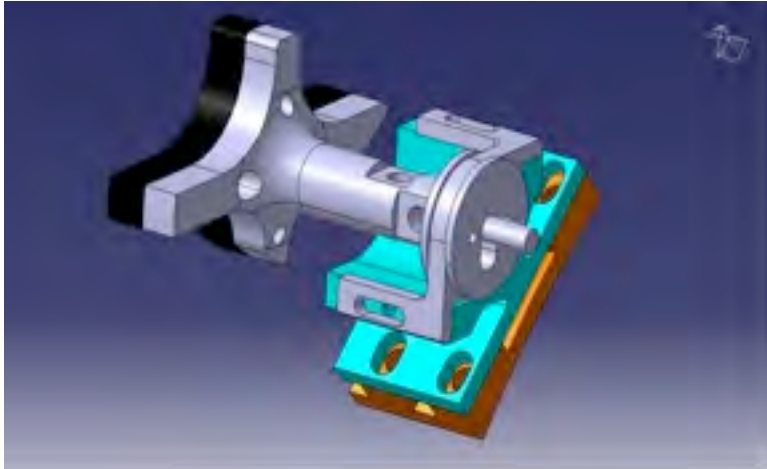
Figure 64: Detail of the interface between SSD and cone (the orange part is glued to the cone).

4.4.6. Cable Paths from the Cone to the Platform

We plan to use the existing power cables except on the cone where the path length is expected to be longer. There needs to be breakout on the end of each side of the cone so that detector can be moved inside the Assembly Hall without removing the connections to the ladders. Sufficient space must be allocated on the cone ends for the breakout boxes.

4.4.7. Cable Paths on the Cone

While there is space available for the cables on the STAR platform and the path to the DAQ room, there is limited area on the STAR cone. The FGT will be installed on the West cone and there are only limited access ports for passing cables. Therefore, we make a preliminary estimate of the space needed. This calculation uses the existing power cables and size for the cooling tubes and adds in the expected cable bundle from DAQ and Slow Control.

The SSD is readout separately on each side of STAR. Each ladder is a separate detector. Therefore there will be 20 cables of each type on both the East and West Cone. As each ladder requires only one HV bias cable, alternate ladders are fed from both the east and west side. An estimate of the size of the cables is given in Table 16. The power cables are the same size as the original design.

System	Cable Type	#	Diameter mm	Area Rectangular cm^2	Total Area Rectangular cm^2
DAQ and Slow Control	Optical Fiber (dual)	20	3.0	0.1	1.8
Ladder power	Sense (4x AWG 24)	20	6.4	0.4	8.1
	LV (6x AWG 18)	20	8.1	0.7	13.2
	HV Bias (2x AWG 24)	10	4.3	0.2	1.9
Air Cooling	Air cooling to end of cone	20	12.7	1.6	32.3
Contingency		0.15			8.6
				Total cm^2	65.8

Table 16: SSD Cable parameters. The area for the cable size is calculated assuming it is square.

In the current design of the SSD mount, the space for cable removal was around 10 cm. As that design had cables and air tubes spread all around the cone, it was relatively easy to work on the detector. This feature must be achieved in the new design. Now that the FGT wants to be situated as close as possible to the center of the interaction region, careful attention must be paid to the cone design so that there is adequate space for the installation and removal of the SSD cables and cooling tubes when the FGT is installed. Sufficient space on the cone must be allocated for these cables.

4.4.8. Rack space

The SSD currently occupies one rack on the South Platform. This rack contains a VME crate, two CAEN power supply crates, and two distributions boxes for the HV and power cables. This space will be maintained for the present CAEN supply or a replacement. The power supplies provides, +2 V, -2 V, and +5 V to the ladder.

4.5. Integration into STAR

The HFT is a highly integrated project. In addition to two new detectors, IST and Pixels, the HFT Project Deliverables share supports with the FGT, and directly supports the SSD, and a new Beam Pipe for STAR. Additionally, HFT must be compatible, thus 'integrated' with any/all future STAR physics programs which might interface to or be impacted by it.

The supports for HFT and FGT will replace the current support cone structure in its entirety. This new structure, called the IDS (Inner Detector Support) shares deliverables

with FGT, but nominally replicates the current mechanical interface of the current cone system to the STAR TPC. This will be described in more detail below. Installation of this structure is nominally identical to the insertion/removal of the current support cone so will follow existing procedures and use current tooling

HFT also requires a new beam pipe for STAR. The Pixel Detector has a smaller aperture than the current beam pipe therefore a necked beam pipe is required on the same timeframe as first insertion of HFT Pixels. The HFT Pixel Detector is intended to be easily installed/removed even/especially during operations, so Pixel installation is explicitly not included here, rather in the Pixel Mechanics section of this document.

The various support structures for SSD, FGT, IST, Pixels, and the Beam Pipe also support all internal service routing, and must be compatible with IFC (Inner Field Cage) E-Field requirements. The services for the SSD will impact the design of the FGT as they will share space with FGT Services. Adequate routing space and strain relief for services is a requirement across all integrated detectors and here we will include requirements placed on the FGT project (to allow space).

The integration of the HFT Project is probably best described in terms of the Assembly Break Down Structure. An ABS rather than a WBS is better at capturing discrete interfaces which must be controlled--even within a given WBS task. The sections below will roughly follow an ABS.

Following is an overview of the primary integrating structures, their interfaces to each other and the detectors which they support. This will be presented in an ABS format, and followed by a summary of Services both internal and external (inventory and requirements). A brief description of the New Beam Pipe for STAR will also be provided.

4.5.1. Mechanical Supports and Structures

The HFT and FGT Projects will replace what STAR calls the 'Cones' within the IFC of the TPC. The 'Cones' currently support the Beam Pipe, and formerly the SVT and SSD detectors. The current Cone Structure is incompatible with the FGT. The FGT requires a 'cylindrical' replacement of the West Support Cone, to accommodate the cylindrical shape of the GEM Disks and their positions for required pseudo-rapidity coverage.

The current, soon former, cone structure is monolithic--it is bonded together; two identical cones, attached to each other via two elliptical beams. These are bonded together via large aluminum inserts at the ends of each beam and the small ends of the cones. The SSD and Beam Pipe are currently supported via these large inserts (**REF Fig below**).

--> Insert figure of current cone structure <--

The IDS, will replicate the support interface of the current cone structures to the TPC Wheels. Several options have been investigated for this replacement; choice between the various options was optimized via cost and schedule to arrive at the current baseline. The options are not presented in this document.

The baseline plan for support of the HFT Detectors and the New STAR Beam Pipe involves a new support structure: The IDS. The SSD (and FGT) will be directly supported on this structure and the Pixels and IST will be integrated on a separate structure the MSC (Middle Support Cylinder) which will be inserted into the IDS from the East end. The MSC will also provide the inner supports for the new Beam Pipe.

The goal of the structural layout is to enable as much as possible the parallel integration of sub detectors prior to a STAR opening. For the first iteration, the Pixel Engineering Run for run 12 (summer 2011), the mechanics will be a direct replacement of the entire cone/beam pipe system. Later installation of the IST and SSD in Run 14 (Summer 2013) will require recovery of at least the beam pipe from the installed system. Some duplicate structures (production versus prototype) will allow pre-assembly of the IST and SSD before the opening of STAR in Summer 2013, removing these activities from the critical path of the shutdown. A description of the structures, followed by assembly sequences required for Runs 12 and 14 follows. Note that most figures shown will be indicative of the configuration for run 14 as all structures must be compatible with this configuration.

Inner Detector Support

The Inner Detector Support is composed of 3 main structures, the East and West Support Cylinders (ESC/WSC), and the Outer Support Cylinder (OSC) which spans the gap between the ESC And WSC. The OSC also will eventually support the SSD in Run 14. The three cylinders, ESC, OSC, and WSC are the primary supporting structure for both HFT and FGT and these structures together are the IDS. The ESC and WSC are nominally copies of each other using common fabrication and assembly tooling. The SSD will eventually be supported on an OSC, but is not intended for Run 12. The MSC which will support Pixels, and the Beam Pipe for run 12 is supported at both ends of the ESC, and potentially by the west end of the OSC (TBD).

Mechanical Requirements

The Structural performance and interface requirements of the IDS is driven by both HFT and FGT requirements. As it is impossible to have separate supports within the Inner Field cage for these detectors, some shared design responsibility is inevitable. The HFT requires global stability on the order of the pointing resolution of the TPC, Order ~1mm, however the FGT uses the beam constraint for tracking so requires stability on the order of the beam diameter, Order ~100µ, so drives the global stability of the IDS. The stability performance of the current design of the IDS is presented in the Appendices (REFERENCE APPENDIX)

The mechanical interfaces, e.g. envelopes and supports are also driven by both FGT and HFT. The length and diameter of the OSC is set by mechanical interface of the SSD Layout and its services. The Length and diameter of the WSC (thus ESC), is set by the FGT acceptance. The Structural elements (material) of the IDS which traverses these envelopes is driven by the structural performance requirement. Additionally, support elements for the SSD, FGT and MSC (Middle Support Cylinder) must be included in the interfaces of the IDS. Routing space for services of the SSD and FGT also impact the IDS.

-->IDEALLY should include reference to 2D Layout of complete Inner Tracking System in Appendices when it becomes available.

Electrical Requirements

The IDS is inserted into the Inner Field Cage of the STAR TPC, thus it must be compatible with the bias voltages applied within this environment. The ESC and WSC (large diameters) will protrude into the IFC to lengths at which the bias voltage is ~6kV. A large radius shroud will be provided (See figure below) to ameliorate the potential for surface breakdown or coronas at the abrupt changes in radii of the structures. The shroud will also support an EMI foil over the SSD. Subject to further field analyses, this shroud, and perhaps a portion of the outer skins of the ESC/WSC may need to be biased. Standoff, both surface and thru-thickness of any applied bias voltage (some few kV) of the base material of the ESC/WSC structures is required, detail design remains.

West and East Support Cylinders

The intention is to share tooling and thus geometry between these two structures. They are each composed of 3 main elements, each with some sub-structure appropriate to their side (e.g. FGT support on the WSC). These elements are the primary shell (with a flat to avoid the Inner Field Cage Resistor Chain), a Transition Cone which spans the radial gap between the shell and the OSC, and a Termination Ring which is the primary interface to the TPC—essentially replicating the current mechanical support (with brief modifications to improve upon the old adjustment interface).

These structures are the dominant part of the 'simply supported beam' which is the IDS. Each component plays its part in transferring the static loads between TPC supports; these are the primary moment loads from the eccentrically applied detector/service masses, and the reactive point loads from the supports. The transition cones dominate the moment load transfer, and the Termination Rings will hold the roundness of the shells, both contribute to the overall stability of the IDS.

The electrical Shrouds are not considered part of this deliverable, but are obviously required to meet electrical performance of the IDS system—they will be discussed later.

Structural Shell Assembly

The main component of the Structural Shell is a thin carbon fiber laminate, potentially with an integral outer layer applied during manufacture to allow for bias voltage to be applied. The inner diameter will be common to both WSC and ESC as it will be set by common tooling. Lamina may differ between the two structures based on differing structural requirements to support the FGT.

The large sectional inertia of the shell implies that the global performance of the IDS is not dominated by the laminate properties as born out in (APPENDICES REFERENCE). It was shown that thickening this laminate simply increased the mass, increasing the deformation implying that this is not an avenue for decreased deflection.

The geometry of these shells is driven primarily by the FGT acceptance. The laminates may need to include provision for bias, thus include some length of conductive surface and sufficient insulated surface to stand off surface creep, and thru-thickness resistance.

Mechanical Flanges at the 'middle' (low |Z|) ends are required for mechanical (bolted) interface to the Transition Cones. A bolted interface is desired to reduce overall risk. The shell is a large part with potentially high fabrication cost; secondary bonding of orthogonal features rather than integrating them into the tooling reduces likelihood of engaging contingency at the expense of an additional assembly step. This is amortized over the risk involved in fabricating the Cone Structure. Should the Transition Cone prove inadequate after prototyping, it will allow easier replacement with another iteration of the transition cone.

Transition Cone

The Transition Cone transfers the primary moment load of the simply supported IDS from the Structural Shell to the OSC. It was initially envisioned as a flat 'plate' perhaps a honeycomb panel, but studies showed that a conical laminate was more efficient in terms of material. (APPENDIX Reference). Maximizing the cone depth (frustum), maximizes performance of the entire IDS. The frustum is limited by the length of the SSD and the position of the first disk of the FGT. Currently this is limited to 7cm. With the depth of the cone limited to what is acceptable from active detector layout, the overall stability performance of the IDS is most sensitive to the thickness of the Transition cone. The Transition cone is currently 4mm thick, with 5mm flanges at both inner and outer diameters to allow bolted interface to the Structural Shells and the OSC. Note that the flange thicknesses are 10mm overall, 5mm for each side of the flange.

Transfer of stresses into the cone via the flanges has yet to be investigated—they are currently idealized in the analyses, i.e. perfectly coupled. The flanges are currently envisioned to be CFRP with either Aluminum or Titanium fasteners. Fastener stresses will dictate whether these are Al or Ti fasteners, and contact stress may dictate that these flanges may need to be metallic. Albemet (Aluminum Beryllium alloy) is an option which would maintain the same X0 as CFRP. Cost versus X0 needs to be studied.

Termination Ring

The Termination Ring is intended to replicate the mechanical interfaces of the current cone system, i.e. the mounts to the TPC and to the existing installation rails used to insert the cone system. It is most likely a machined aluminum ring that will be bonded to the structural shell.

As does the Transition Cone, the Termination ring also contributes to holding the ESC/WSC round. As its radial extent is limited to be the same as that of the current cone's termination rings, an auxiliary radial stiffening plate will be required at each end to help resolve the point loads into the shells of the ESC/WSC. The interface to this stiffening plate is intended to be compatible with all service exits and independent removal of the stiffening plate for various service scenarios, in the case of the FGT, also removal/installation of FGT Disks. Due to a desire for shared interfaces, this will be true

for both sides. The implication is that the interface must 'force' the Transition Ring to be round via tapered pins or some absolute reference/interface to maintain the global shape/deflection of the IDS should one of the stiffening plates need to be removed and re-installed.

Support of the IDS to the STAR TPC is a functional part of the Termination Ring. As mentioned above, this will be modified to allow for more independent adjustment of the IDS position. Currently, all motions are coupled, i.e. are not independently orthogonal, and the current cone is over constrained in more than 1 DOF. The new support will be '4-2-1' i.e. 4 vertical, 2 horizontal and 1 "Z" constraint, so only over-constrained in the 'vertical' dimension.

E-Field Shroud

Initial field calculations indicate that a 4cm or greater radius is required at the |Z| extent of the ESC/WSC to meet field requirements if the surface is at ground potential. The goal of the shroud design will be to exceed this radius and project down to just outside the SSD radius to support an EMI/Field cover for the SSD. The intention of the current design is to not require bias of any structure, however this will be the result of further field calculation

The structure of the shroud will be fiberglass with a high dielectric matrix (Cyanate Ester) which is also common to all of the other structures (it also has high radiation tolerance). The outer conductive layer is undetermined, but proposed to be metalized fiber rather than conductive paint to reduce chance of contaminating debris within the IFC. The need for bias will likely require some development of this laminate in addition to its interface to the Structural Shells of the ESC/WSC.

OSC (Outer Support Cylinder)

The OSC replaces the elliptical beams of the current cone structure. It spans the gap between the ESC and WSC and carries the moment load between them. It is designed to have the same amount of material as the current beams, but spread over a cylindrical region of volume. Its stiffness will match the current beams for vertical deflection, with the added benefit of also providing the same stiffness horizontally.

The OSC will (eventually) include the supports for the SSD, as well as any strain reliefs for its services. A benefit of the OSC being a cylinder as opposed to the previous elliptical beams is it allows the SSD ladders to be directly mounted to the outer surface of the OSC. This presents several benefits for the SSD, and generally the STAR Inner Tracking performance. The relatively massive aluminum support rings for the SSD can be eliminated, saving mass in front of the FGT, and near the edges of the TPC. The SSD ladders can now be independently mounted/removed increasing serviceability. The SSD coverage can be optimized to maximize hermiticity over the previous layout which had sizeable and non-phi-symmetric holes in coverage.

Additionally, the OSC separates the gas volume of the HFT detectors from the IFC, so if the IST and/or Pixels must operate at other than ambient temperatures, the SSD and IFC will be isolated from their environments.

As the OSC carries the primary moment load of the IDS, the global stability of the IDS is sensitive to its 'thickness' dimension. The present analyses (SEE APPENDIX) treat all lamina as isotropic materials, roughly equivalent to Titanium, with the density of Carbon Fiber. The only way to change the stiffness of the OSC was to change its thickness. With composite materials, another dimension is available, i.e. fiber orientation. The overall thickness of the OSC is currently '1mm Titanium Equivalent'. It is likely that a moderately thinner, oriented CFRP laminate will provide the same or greater stiffness.

MSC (Middle Support Cylinder)

The MSC is a stepped cylinder in form and is the primary integrating structure for the Pixel and IST detectors. It is supported by the IDS via its east end (west end under consideration). It is composed of two cylinders and a transition plate. The transition plate is the primary interface to the IDS.

The smaller cylinder supports the IST, Pixel Detector and New Beam Pipe. The IST is supported on its outer surface via individual stave mounts. The Pixel Detector is supported by 'Kinematic Mounts' integrated into the MSC small cylinder. The Beam Pipe is supported on both ends of the MSC small cylinder, on the West end by a flange and the East end by a longitudinal plate, integrated with the transition plate, that allows for longitudinal expansion during bake-out.

The smaller cylinder is cantilevered off of the ESC via the transition plate which is attached to the larger cylinder of the MSC. The larger cylinder supports the IST services on its outer surface and the Pixel insertion rails on the inside. The length of the larger cylinder will be optimized to facilitate Pixel Insertion. It is planned for the larger cylinder to share diameters with the OSC, minimizing tooling for shells and flanges.

-->**Insert Figure**<--

The MSC also performs as an environmental enclosure for the Pixel system, forming the return ducting for the Pixel air cooling system. The IST will be on the outside and in a separate gas environment. The support of the beam pipe on the far end of the Pixel detector (west) will also serve as the gas return/seal for the Pixel environmental gas.

The FGT requires an enclosed volume for its cooling air, which is currently a separate structure. This may be integrated into the IDS thus providing a support point for the west end of the MSC.

4.5.2. Assembly Sequence

There are two configurations of the IDS required for HFT. The first allows for the Pixel Engineering run with FGT in Run 12, the second is the complete HFT (Pixel, IST, SSD) configuration slated for run 14. All of the structures described above, IDS, E-Field Shrouds, and an MSC are required for both run configurations, however mounts and services for SSD and IST are not required on any of the structures for run 12, implying that pre-production MSC and OSC structures could be used for run 12. The following Assembly Sequences will illustrate why pre-production versions should be used for Run 12 and later production versions of the MSC and OSC should be used for Run 14.

There will be two opening events planned for STAR, first to install the HFT Pixel Engineering system and FGT for Run 12, and later to install the complete HFT system (SSD and IST) along with Pixels for run 14. All subsystems (IST, Pixel, SSD, and FGT) desire some extended commissioning prior to installation in STAR, implying availability of integration structures several months prior to installation. Installation of either configuration of the IDS in STAR is tied to a STAR Opening, so are necessarily on the critical path for RHIC shutdown. The primary integration structures for SSD and IST, OSC and MSC respectively, are required for Run 12, meaning that they are installed in STAR. Preparing these detectors for Run 14 also requires an OSC and MSC allowing both SSD and IST to commission externally to STAR several months prior to STAR opening.

For Schedule purposes, it is highly desirable to produce two versions/copies of the MSC and OSC to allow assembly and commissioning of the IST and SSD in parallel to Run 13 so that they are immediately available for integration into the IDS as soon as it is removed from STAR after opening, reducing time on the critical path of the RHIC Shut down.

The aim of producing copies of the structures is to minimize the number of components that need to be recovered from the configuration installed for Run 12 prior to onset of integration for Run 14. All components installed in Run 12, required for Run 14, places the effort for their recovery (disassembly) and later integration/assembly/test on the critical path of the preparation for Run 14.

One thing common to all assembly scenarios is that the beam pipe must be supported adequately along its length with tooling that allows various transitions of loads to let the various cylinders pass over it. Lengths of these cylinders (MSC/OSC/ESC/WSC) may require either cantilever or 'reach-thru' tooling to guarantee safety of the beam pipe, and leak-tightness of subsequently inaccessible vacuum flanges. Tooling is not yet designed, but it is likely that all operations involving the beam pipe, from initial integration of MSC thru integration of the IDS will be on a common tool of approximately beam pipe length.

The Beam Pipe is a BNL deliverable with many auxiliary processes. The Beam Pipe, its delivery to STAR, and auxiliary requirements, will be described later, however it is important to know that the New Beam Pipe is envisioned to be 3 parts, a middle section of small diameter with a Be middle, then two end pieces with conical transition to larger diameter.

Initial IDS Assembly (Run 12)

It is assumed that the FGT will be pre-integrated into the WSC; for further purpose of this discussion, WSC and FGT are synonymous. Neither the SSD nor the IST are available for Run 12. The FGT will have been previously integrated into the WSC and the main goal of this assembly procedure for HFT is to incorporate the beam pipe with the MSC, and insert that structure into the ESC, mount the OSC and attach these to the WSC. The Pixel insertion happens after the assembled IDS is inserted into STAR. Pixel Insertion is currently described in the Pixel Mechanics section of the CDR (REFERENCE?)

Following is a presentation of the order of assembly. Some activities may happen in parallel, but this represents the basic order of assembly—note that this is aimed at the assembly required for Run 12; sequence for Run 14 will follow.

New Beam Pipe is integrated with MSC.

This can likely be completed prior to STAR being opened, but depending on beam pipe delivery, may need to occur in parallel with assembly of the IDS. Ideally, this would have been dry fit at LBNL prior to arrival at BNL.

As mentioned above, the integration of anything with the beam pipe involves a tool which fully supports the beam pipe. The base procedure is that after the Beam Pipe is supported in the tool, the cylinders are passed over it transitioning supports. First the small cylinder of the MSC is passed thru to the middle, where the beam pipe is attached to supports at both ends of the cylinder--the cylinder then takes the load of the beam pipe, and has its load transferred to the tooling

The Beam Pipe Flange that transitions to the larger diameter section will be in the middle of the larger MSC cylinder which comes next in the assembly of the MSC. The beam pipe section of larger diameter with the conical transition is of longer length than the MSC Large diameter cylinder. The beam pipe extension will be introduced simultaneously with the Large MSC Cylinder so that it can be supported on both ends for mating to the Be section of the Beam Pipe. After mating, but before joining the MSC together, the beam pipe flange must be leak checked, perhaps allowing for 2+ days to pump down and check. Space must be allowed for pure gas purge and full access to the flanges setting some limits on the interplay between lengths of MSC large cylinder and Beam Pipe extension.

The larger cylinder of the MSC is then bolted to the transition flange to the MSC small cylinder. An auxiliary support from MSC to Beam Pipe is installed. The Beam Pipe is now only supported by the MSC internally and the Tooling Externally.

This procedure yields the Beam Pipe supported by the MSC, and ready to insert into the ESC (and perhaps test insert pixels on the same bench (longer length required).

MSC into ESC

The ESC will have been prepared in parallel to the previous integration and mounting the MSC/Beam Pipe Assembly into the ESC can proceed immediately. Similar to the MSC integration, the Beam Pipe and thus the MSC must be fully supported. As the MSC supports the Beam Pipe, some tooling that reaches thru the ESC as it passes over the MSC may be required. Alternately a study of how to cantilever the MSC (likely possible) will be conducted to minimize tooling cost. The primary driver for 'inserting' the MSC into the ESC is support of all elements during assembly.

OSC Over Extended MSC

Once the MSC is joined with the ESC, the OSC can be installed over the small cylinder of the MSC. It is shorter than the ESC so can either share the same tooling or benefit

from the increased stiffness/cantilever possibility of the ongoing assembly. The tooling should be designed to allow for an SSD in this configuration, but as this will be two years hence, the tooling can be simplified somewhat, perhaps even done by hand considering the absence of any sensitive silicon.

WSC attached to OSC

Introducing the WSC to the combined structures of ESC/MSC/OSC is similar to the assembly of the MSC with the beam pipe. There is a flange in the beam pipe which will be covered by the WSC. The WSC is similar in length to the large diameter cylinder of the MSC so the procedure will be similar, though necessitates tooling on the West side; either as an extension of the tooling or included previously in the overall tooling length.

As soon as the Beam Pipe has been leak checked, the WSC can be bolted to the OSC. Once WSC is bolted to the OSC west end, the IDS is complete and nearly ready for insertion into the IFC

Shroud Installation

The East end of the shroud could be installed as soon as the ESC is installed over the MSC, but likely both sides will be installed simultaneously. The Shrouds are necessarily half shells, so they can be installed around the pre-assembled IDS. They will be attached to the ESC/WSC via some form of film backed PSA (tape), conductive or not, and their halves joined similarly. If a bias voltage is required, appropriate terminations and various and sundry resistance testing will be conducted. It is unclear if a further cylindrical cover, normally meant to cover the SSD, now not present, is required. This will likely depend on whether and how the shrouds are biased.

Once Shrouds are fully installed and properly tested, the IDS is fully ready for installation

Installation into STAR IFC

Intention is that IDS identically replicates all current 'cone' interfaces for installation up to how it mounts to (is supported by) the TPC. All steps used to insert/remove the current cone structure should remain valid; only transfer of the load of the IDS to the TPC wheels should differ. The transfer protocol is currently TBD.

Pixel Detector

Pixel Insertion into the MSC is covered in the Pixel Mechanics section of this document. In the interest of covering requirements related to Integration, the HFT Pixel detector is included here.

The Engineering Run for the Pixel detector will need to be commissioned simultaneously with the FGT, likely requiring space in the clean room and access to DAQ, Power crates and some method of cooling (ducted air system). This capability, and space requirement, needs to be maintained throughout the duration of the HFT project to support the later commissioning of the final Pixel System.

Obviously, some time to terminate the Pixel Services will be required after full STAR closure. It is currently unclear where external Pixel Services run, i.e. inside or outside of the Magnet Return Iron, thus uncertain where in the schedule this activity occurs.

Final HFT Assembly (Run 14)

Run 14 will include all HFT deliverable detectors, Pixel, IST and SSD. The Pixel system will provide the next generation of their detector in entirety with mechanics to allow for insertion after end of Run 13. The Pixel System also requires something similar in form/footprint or identical to an MSC to properly cool during system testing. The IST and SSD will be integrated (assembled), surveyed and commissioned prior to the end of run 13 in preparation for installation for Run 14. All of these activities will require space in the clean room for any operations involving exposed Silicon. The clean room is also a primary resource for access to STAR DAQ and similar infrastructural requirements during the commissioning of these detectors. The commissioning of these detectors is foreseen to start during Run 13 and continue thru final integration into the IDS in preparation for Run 14.

To integrate the full HFT into the IDS several structures involved in Runs 12 and 13 will need to be recovered from the IDS after conclusion of Run 13 and before onset of Run 14. This operation—recovery of, and integration with, structures that will comprise the IDS for Run 14 are on the critical path of the onset of run 14. Presently, these recovered structures include the ESC and Beam Pipe. Additionally, the FGT desires to run without the integrated SSD services in the WSC for Runs 12 and 13. The implication is the required removal of the FGT from the WSC to then install the SSD Services followed by re-installation of the FGT. This activity is included in the STAR opening between Runs 13 and 14. It is likely that the FGT would desire maintenance/upgrade during this opening so this is likely off of critical path, but installation of SSD services needs to be included in the HFT Project at this point in the schedule. An auxiliary point is that at this time, the Clean Room is mostly occupied by IST, Pixels and SSD. FGT may require an auxiliary clean room or force HFT into requiring the same.

A detailed schedule for the activities required during Summer '13 (prior to Run 14) does not exist. The designs and activities proposed are aimed at minimizing the activities and thus duration required. This factors into the need for auxiliary/replicate structures for the MSC and OSC to allow commissioning/survey of Pixels, IST and SSD prior to opening STAR after Run 13. Co-habitation with FGT or other ancillary STAR activities is not addressed.

The following description of HFT assembly will start first with activities which precede the STAR opening at end of Run 13, and follow with actions required to recuperate required structures, and re-assemble the detector in preparation for Run 14.

Pixel Integration

The Pixel System is designed to be entirely independent from the global HFT structural assembly—it is meant to be inserted or removed during STAR Run configuration. The primary impact of the Pixel System on this phase of the assembly is occupancy of the

Clean Room. As mentioned above, it will require facilities similar in size to the MSC. Preferably an auxiliary MSC for test insertion and cooling, in addition to similarly sized space upon removal.

IST Integration

The IST Staves are individually attached mechanically onto the outer surface of the smaller MSC cylinder. At this point it can be surveyed, given survey capability at BNL. It is assumed that Staves are previously tested individually, but 'commissioning' as an assembled array will not occur until they are assembled onto the MSC, preferably with its final internal service plant.

The IST Services are supported by/attached to the MSC large cylinder. As mentioned above, the Beam Pipe must be assembled into the small cylinder prior to attaching the large cylinder. It is possible to commission the IST with its 'permanent' service chain, but to install the recovered beam pipe, complete disconnection of this tested and commissioned service chain is required to allow installation of the beam pipe recovered from Run 13. Re-connection and sufficient testing of these connections would be required on the CP of the opening between Runs 13/14.

It is pre-supposed that an additional MSC structure is available well in advance of the end of Run 13 to allow dressing and commissioning of services for the IST.

SSD Integration

The SSD is assembled onto the OSC. 'An' OSC is required for Runs 12/13 to bridge the gap between the East and West Support Cylinders. The SSD needs to be assembled and surveyed as a unit on an OSC, and ideally commissioned in this configuration. It is unreasonable to assume that this could occur after recovering the OSC used for runs 12/13 and before onset of Run 14, thus it is desirable to fabricate an additional OSC with SSD mounts in preparation for Run 14.

The SSD ladders will be assembled onto an OSC and surveyed, either at LBNL or BNL, perhaps both to allay shipping concerns. The SSD Permanent External Services are not available for commissioning as they are integral with the ESC and WSC—these will have to be installed during the opening between runs 13 and 14.

MSC Integration

This is very similar to the initial integration, but needs to wait for the recovery of the central Be section of the Beam Pipe after the IDS is removed from STAR (requires basically complete disassembly of installed IDS). In parallel, the IST services can be disconnected, and MSC large and Small cylinders separated. After recovery of the central Beam Pipe, the assembly process follows identically that above.

Tooling may need to be modified to account for the presence of Silicon and Services. After Termination of Beam Pipe and Small to Large MSC Cylinders, some time to re-test/commission the IST is required. This should not require disassembly of the structure,

but may require replacement of some IST Services and re-testing before moving onto the next step.

MSC into ESC (ESC over MSC)

As the IDS must have been completely disassembled to even begin the MSC integration, the ESC is obviously available by when this occurs, however, some time must be allotted to allow for integration of the SSD Services into the inner surface of the ESC. It is possible that this can occur in parallel to the aforementioned activity (MSC Integration), but additionally available manpower will be required.

The procedure is identical to the one for initial installation, however should occur in a 'clean(ish) room'. It is not likely that this cam occur in 'the clean room' in the STAR Assembly Hall, but should occur in a moderately protected environment as the IST represents exposed silicon and wire bonds.

There is sufficient space in the clean room to accommodate this action, but unclear if previous tooling used to assemble IDS with Beam Pipe will fit into clean room. The previous (initial) assembly of the IDS was not done in the clean room due to Pixel/FGT occupancy and no exposed silicon. It is likely that an external 'clean' or at least 'protected' environment will be required for this assembly procedure.

OSC onto ESC

The OSC and SSD at this point are mechanically integrated. The goal of this operation is to structurally attach the OSC to the ESC, followed shortly by the attachment of the WSC. Unlike the IST, the SSD will not present exposed silicon or wire bonds. This operation can largely be in the open on the assembly hall floor. It is desirable to protect/cover the area to prevent entrainment of contaminants from ceilings, cranes, and various wildlife from imposing on the exposed detector surfaces.

WSC attached to OSC

This basic mechanical procedure is identical to the procedure described for the initial installation. The WSC and Beam Pipe will have been recovered from Run 13, and the FGT will have been refurbished, hopefully all in the time it took to get to this juncture in the schedule. As with the ESC, the WSC will require installation of the SSD Services. The WSC can lag on this the proximal time it takes to integrate OSC to ESC, but again points toward additional manpower to minimize schedule impact.

SSD Service Termination

The ESC and WSC both carry either side of the SSD Services. All cooling connections are available on the ESC and could start as soon as the OSC is attached to the ESC, however the SSD requires services from both sides to be fully operational due to the design of its service chain. Full testing of the SSD cannot occur until the WSC and the related SSD services are available.

SSD will require a nominal time to verify that all services are properly connected before onset of covering it's connections with the E-Field Shroud, after which all service connections will be inaccessible

E-Field Shroud Termination

These structures will have been the first recovered from the Run 13 opening. Additional structures will be provided in case of damage during removal—these will be very low mass, thus fragile objects. Mounting, or re-mounting the shrouds will entail some clean-up of the surfaces (previously taped) to assure proper electrical contact and no aberrant asperities.

Attaching of the shrouds can only follow sign off of acceptable SSD connection. Following that, appropriate electrical conductivity (or bias stand-off) tests must be conducted.

Insertion of the Cone Into STAR

This is fundamentally equivalent to the current procedure, so should both follow the existing procedure and use current tooling.

Additional operations to terminate the IST, SSD, and FGT to service chains which move with star will be completed after STAR is installed on the Beam Line.

Pixel Insertion

The Pixel installation procedure is designed to occur while STAR is in position on the beam line after beam pipe termination and bake out. There is no reason to believe that the Pixel detector would ever install with STAR removed from the experimental hall.

Every effort will be made to assure that the Pixel detector can be installed within an 8hr period, including modification of detector supports of the BBC for quick removal/reinstallation to gain access to the Pixel installation volumes.

Functionally, the Pixel detector is introduced from beneath the beam pipe on an external platform replicating the installation rails internal to the MSC. This platform is aligned to the internal rails, and the Pixel system pushed in, perhaps with additional articulation around external interferences. After insertion, the MSC is sealed to the Pixel Package, and its services terminated to the external service plant.

Assembly area requirements

As mentioned above, several of the operations may require extended length, and perhaps a clean/semi-clean environment. Clearly, installation of the ISC with or without the IST will require the most length. If possible, it would be desirable to move the removed cone to a location where it can stay for all operations, including initial assembly and any FGT related actions.

The final version of the Pixel system (Ultimate, rather than Engineering) will likely compete with the IST/SSD for clean space. The IST will require a clean space to

assemble, and test its staves on the MSC. The Pixel System will require a similarly clean space to test the new electronics for installation after the engineering run.

4.5.3. Beam Pipe

HFT requires a new beam pipe. The Pixel System's innermost radius is smaller than the currently installed beam pipe. The new radius required is identical to that proposed for PHENIX, and thus agreed to by the RHIC Machine interface. The proposed beam pipe has the same length and flanges as the current beam pipe so represents a direct replacement. The primary change is a necked down region surrounding IP. The small diameter region will be thin Beryllium (0.8mm wall) to a length which is beyond any acceptance of currently installed STAR detectors. The remainder of the beam pipe, will be Aluminum.

Mechanical

STAR/HFT will be responsible for the mechanical design and layout of the new STAR Beam Pipe, in consultation with Brush-Wellman, the most likely vendor, and with sign-off from the machine (accelerator) from CAD of BNL.

The layout, primarily Beryllium length, has been optimized to suit STAR's current physics programs. Transitions to larger diameter are limited on one side by the articulation of the Pixel insertion. The other side will transition to larger radius after the Be section, perhaps with some Aluminum transition TBD after consultation with Brush Wellman.

-->**Insert Figure**<--

The Be section is detailed in the above figure

Bake Out Considerations

The beam pipe will have a NEG coating which must be activated after the beam pipe is terminated and evacuated. The required bake out temperature is up to 250C. The Pixel Detector is not compatible with this temperature so must be removed during bake out.

It is intended to have insertable bake-out jackets for at least the pixel section (small diameter) of the beam pipe. It is possible that these insertable jackets might also use the same insertion mechanism as the Pixel detector, but this mechanism only exists on the east side.

It is proposed that all large diameters of the beam pipe have integrated bake out jackets, similar to those installed on the Be beam pipe of ATLAS. These are heaters laminated directly to the beam pipe, and insulated to keep heat egress to a minimum.

Support

The beam pipe will be relatively fragile, so must be adequately supported during all assembly operations and adjustment within the detector volume. It is assumed that the

beam pipe will move with the Support Cone Structure. Any beam pipe adjustment will occur solely by adjusting the position of the support cones within the IFC. As such, the beam pipe will be rigidly supported ultimately to the Support Cone Structure.

Assembly

As mentioned above in the section on assembly, the Beam Pipe must be supported adequately during all phases of assembly. This will require a tool mimicking the final support condition, but with auxiliary attachments to allow transfer of loads. Design of this tooling will need to consider safe load limits during all modes of load transfer

Final Support

The Beam Pipe will have 4 primary support points. Two near IP and two at the extremities of the TPC, all will move with the Support Cone Structure during any STAR movements, and transfer to the external (current) STAR supports after STAR is on beam axis

Two permanent supports will be incorporated into the MSC. The two inner most supports will be directly to the MSC Small Cylinder to either side of the Pixel detector as installed. One of these, the one around which the Pixel system must be installed, will need to be only vertically oriented. Because the Beam Pipe requires stability in all directions, this support must also provide some bending stiffness, thus have some thickness. The other support on the small cylinder (west), opposite the insertion side of Pixels needs to also seal the gas volume of the ISC, so can be disk like. Adaption to flanges incorporated into the Beam Pipe is foreseen.

The Temporary East Support, will be to the large cylinder of the MSC which in turn is supported by the ESC. After STAR is on Axis this can be transferred to the current external support

The Far West support will be terminated after the Beam Pipe is inserted thru the WSC. This will be directly to the WSC and can similarly transferred to the current external support after STAR is on Beam Axis.

-->**Insert Figure**<--

4.5.4. Services

Summary of Air, Water and Power

Space requirements on Magnet and Platform

4.5.5. Controls

4.5.6. Data Acquisition

4.5.7. SSD

4.6. Software

This section contains the description of the software elements required for the successful processing and analysis of the acquired raw HFT data. Since the HFT is an upgrade detector of the STAR experiment, its software needs modules to be incorporated into the existing software and computing environment of the experiment. After a brief discussion of STAR's software environment, we list and describe the online, offline and simulation modules and tools that are required to be developed for the HFT. We will finish with a discussion of resources and institutional software responsibilities and commitments.

4.6.1. STAR's Software Environment

The STAR software environment comprises of a set of tools (development, simulation, production and analysis environment), mainly in the form of plug-in software modules in a ROOT – based backbone interface. At the same time it provides the data model and the coding standards and the data model for new module development and integration in the top-level shell scripts. Each detector sub-system is responsible for the development of all modules necessary for its successful operation. New, major pieces of code need to be reviewed and approved before insertion in the main repository. This work is coordinated with the rest of the experiment through a designated software representative from the group. At the same time there is a software infrastructure group based at Brookhaven National Lab (aka BNL-core), that maintains and manages critical pieces of code (tracking, calibrations, databases) and also provides help with the integration of new software in the system.

Online Environment

The online software primarily ensures the data integrity during data acquisition via appropriate detector monitoring and sample event reconstruction. Beyond these basic but

important tasks, and as computer processing capabilities improve dramatically, more and more formerly offline tasks move to the online environment. One such task is the hit finding in the STAR TPC. Discussion has started on the possibility for online (pre-) tracking in the TPC. This is of particular interest to this group since we plan for on chip Pixel clustering and hit finding for the Pixel detector.

Offline Environment

The offline environment consists of the event reconstruction software packages. This starts with the raw data as input and through proper calibrations it proceeds with detector cluster/hit finding, integrated tracking, event vertex finding and event information writing on DSTs.

4.6.2. Online Software

The online software serves as a tool to monitor detector performance. It is also used to perform online calibrations where possible. Online software is detector specific and is described in Section 4.2 for the Pixel, in Section 4.3 for the IST, and in Section 4.4 for the SSD.

4.6.3. Offline Software

Hit Reconstruction

The Cluster/Hit finder is the first piece of code applied to the pedestal subtracted raw information from the IST and PIXEL detectors.

In the IST detector this will be a standard search for all fired strip-lets, i.e. all strips with a pedestal subtracted ADC value above a cut/threshold value (typically a value two to three times the strip noise-RMS level. Groups of adjacent strips that are fired will be clustered and further analyzed by a peak finding program for one or more possible hits. Every such 'hit' is then first going to be assigned a set of local/wafer coordinates based on the strip's position on the wafer. This will be followed by a local-to-global transformation to STAR global coordinate system (detector hit information needs to be saved in global coordinates), which is usually done via a series of partial transformations (wafer to ladder, ladder to shell, shell to detector, detector to STAR). This is common practice in silicon strip detectors and the MIT group, which will build the detector, has extensive experience in this area.

 In the PIXEL detector the first steps (Cluster/Hit finding) are incorporated on the chip's logic, i.e. done online during data acquisition, as discussed in Section 4.2. The local to global transformation process is identical to the IST even though the partial transformations will be different in order to incorporate the specific geometry and the specific hardware-implemented alignment features of the PIXEL detector (see discussion on Alignment below and in Section 4.2).

Tracking

The current STAR reconstruction environment provides a Kalman-filter based integrated tracker. This tool is in principle ready to accommodate and integrate the IST and PIXEL hits, with their proper error/weights, in its environment. In reality work and close collaboration with the BNL-core group will be required to tune the tracker's parameters and optimize its performance. For example it has to properly handle the high precision information coming from the PIXEL layers. Also, there is a need to develop methods to deal with the path ambiguities in the SSD and IST (effective strip 'hits' with relatively large errors in the long strip direction), as well as dealing with the ghosting in the PIXEL detector due to out of time events in a high luminosity environment. Dealing with the latter two problems of tracking/ghosting will require studies that use a several-passes tracking approach and/or knowledge of the triggered event vertex obtained from a first-pass (or quick) vertex finder. This is a critical item which will finally determine the physics performance of the system and therefore needs special attention and effort.

Event Vertex Reconstruction

Currently STAR deploys two different event vertex finders during event reconstruction, one for heavy ion and one for proton-proton collisions. Each of them is specifically tuned to perform best in these completely different environments (high multiplicity w/out pile up in heavy ions and low multiplicity with high pile-up in p-p). In a typical heavy ion collision the TPC has to cope with events of relatively large multiplicity and virtually pile-up free whereas in p-p one needs to extract the primary vertex from a few primary tracks surrounded by a thousand of out of time (pile-up) tracks. As a direct consequence of this fact STAR uses a Minuit-based event vertex fitter (with a seed finder) in heavy ion collisions. For p-p the vertex fitting procedure is based on a chi-square minimization method but, most importantly, the information from fast detectors is used to select (tag) the tracks that belong to the triggered event. Only these tagged tracks participate in the event vertex-fitting step.

In the RHIC-II era's increased luminosity there is going to be pile-up in the TPC but most importantly in the two PIXEL layers of HFT due to the relatively large integration time of the detector (see Section 4.2 and also *Pileup* discussion below). This will be the case in both p-p and heavy ion collisions. The SSD and IST are assumed to be pile-up free even for the highest rate p-p collisions. The presence of these two (as well as the other) fast detectors will require a new, revised version of the vertex finder that will combine the best features of both current finders. At this point we do not anticipate the need for any new functionality, just the need for tuning and QA-ing the new/combined finder.

We should note here that the mid-term plans of the reconstruction/infrastructure group include the deployment of a Kalman filter-type vertex finder, which at the same time will do the primary track fitting. In high multiplicity events (>30 tracks or so) one can perform without loss the vertex finding/fitting and primary track fitting (i.e. fitting global tracks with the vertex as an extra point on track for tracks with DCA within a cut value, e.g. currently 3cm, from the vertex. This will be revised in the HFT era due to much higher precision in pointing.) in two separate steps. In low multiplicities it is generally better if one performs a simultaneous fit of primary tracks and event vertex. This is worth

exploring. Let us remember that the larger fraction of the secondary/decay vertices we are trying to resolve are in the range of 10-100 microns and any improvement in determining the event vertex (the most important single reference point in the event) is indispensable.

Secondary/Decay Vertex Reconstruction

The reconstruction of short-lived particles in a collider environment is an extremely challenging task. The key measurements of HFT involve the reconstruction of D- and B-mesons with typical $c\tau$ in the range of $120 - 500$ microns, and Λ_C with a $c\tau$ of 60 microns. The lack of a Lorentz boost typically results in mean decay distances of about half the $c\tau$, for decays at midrapidity of a properly p_T weighted sample. For example, the anticipated mean p_T for D_0 mesons in Au+Au collisions at RHIC is about 1 GeV/c. This is a conservative estimate taking into account expected high p_T suppression effects. The $\beta\gamma$ factor for a midrapidity D_0 is 0.54 and thus its mean decay distance ($c\tau$ of 120 microns) is about 65 microns. For a 1 GeV/c Λ_C baryon this will be about 30 microns. This environment demands the highest level of sophistication in the methods used to reconstruct the decay/secondary vertices.

Up to now, the STAR secondary vertex reconstruction code had to deal with decay vertices of strange particles, typically in the few centimeters range. For those distances, simple geometrical reconstruction models coupled to crude, fixed value cuts were sufficient. Only a recent effort to reconstruct D-mesons with the SVT, the first generation silicon vertex detector in STAR, started deploying decay vertex fitting techniques using the full error information of a track, on a track-by-track and vertex-by-vertex basis (sometimes also called μ-Vertexing). Cuts like the decay length are not fixed values but rather a number of standard deviations of the fitted value. This way the cuts are less biased especially the one, like DCA, which have strong momentum dependencies. This work, currently still under development, will be the basis of the modules deployed on the HFT data. These important software modules are to be developed, as they are a key piece of the new software.

Databases – Calibration and Alignment

The accurate monitoring and recording of the state and the position of the detector inside the STAR apparatus is of outmost importance as it directly impacts its performance. Calibration is the online and offline task of monitoring the state of the detector. The online part (often referred to a slow controls) gathers information of the detector in-situ, usually during running periods. Such information might be temperature or position of elements, pedestal files etc. This information is stored in a Database with a timestamp. The slow controls for the SSD, IST and PIXEL detectors are discussed in Sections 4.4, 4.3 and 4.2 respectively. The offline part of the calibration includes also software methods used to check e.g. the position of the detector elements using tracking information. The results of these procedures are stored as updated values in specific bank in the Database and are used in the massive offline physics production reconstruction passes.

The task of Alignment is a very demanding one especially for the PIXEL detector where one would like to perform/know the positioning of the detector elements with offsets and tolerances to within a few microns.

The alignment of the SSD and IST is not a challenging task provided good survey data has been collected of the detector's elements beforehand. The in-situ alignment will be done with software techniques (global and/or local alignment) and there is previous experience on this in the collaboration. All it is required is to bring the SSD (IST) hits within the TPC (TPC+SSD) track projection errors to the detector layer, typically around 100 microns or so. Global alignment techniques usually yield results accurate to about 10 microns using a set of only a few hundred thousand tracks. Rotations are also typically kept to a fraction of milli-radian.

In the PIXEL detector this task is more difficult and the designers of the detector decided early on to incorporate 'hardware' techniques in order to minimize element displacement in-situ. The pixels are designed with a 20 microns 'envelope' error, i.e. maximum allowed displacement in-situ. To achieve this various sophisticated methods have been developed, e.g. interlocking, easily replaceable pre-surveyed shells with extreme precision on-bench survey data. Details on the method and the specific hardware implementation can be found in Section 4.2.

Despite this excellent 'hardware pre-alignment', software methods will have to be deployed in order to both check and fine-tune the in-situ information of the detector elements. There are two categories of software alignment techniques, the so-called Global and Local alignment.

The *Global* alignment uses TPC (+SSD+IST) track information on a statistical basis in order to obtain systematic silicon detector rotations and shifts. Typically a 'rigid body' model is applied (i.e. ignoring possible ladder twists, sagging effects and wafer non-planarity) and a misalignment model is introduced. Then a Taylor expansion with respect to misalignment parameters (3-D shifts and 3-D rotations) is performed looking for deviations of measured hit position from predicted primary track position on a measurement (wafer) plane. The track prediction comes from the detector(s) used as reference, e.g.\ initially the TPC alone, and later the combined TPC+SSD (+IST) tracking. In the next step, from the hit deviations distribution, a misalignment parameter has been calculated as a slope with a straight line fit. A global least-squares fit is also simultaneously performed on all available information. The method is applied iteratively until the fitted parameters reach stability. This global method was first applied to TPC+SSD+SVT data in STAR and it is well developed and understood. It will serve us in the IST alignment but it will need modifications for the PIXEL detector. This is because the Pixel elements (wafers) on a ladder will have deviations from the 'flat plane' hypothesis.

In a *Local* or *Self*-alignment method one aims at the most precise *relative* placement of the detector elements. In this procedure only high precision hit information is used coming exclusively from the detector under local alignment. A successful method using the event vertex constraint was developed and tested on simulations by the BNL-core group and this should be further developed into a working module with data for the HFT complex.

4.6.4. Simulation Framework

The current simulation framework in STAR is based on GEANT-3.0 with custom script extensions to facilitate detector geometry implementation and event generation. It also includes event generators like HIJING, PYTHIA, Phase-space etc. that are interfaced to GEANT. This framework is soon to be abandoned and will be replaced by a ROOT-based geometry and tracking package (VMC, Virtual Monte Carlo). Nevertheless, we are still using it and we will continue to do so in the immediate future. The tasks, and therefore software modules one needs to develop here are: a) the **detector geometry** definition, b) the **detector response** packages (fast and slow simulators), c) track **embedding** in real/raw events, d) a hit **pileup** handler, e) the Association Maker and structures for **evaluation** purposes, and f) Physics **analysis** code (performance, physics etc) capable of handling and evaluating the resulting information. Our group will have to contribute modules and effort in all these categories. It is worth mentioning here that besides this full and detailed simulation chain the group has developed very useful tools for quick estimates of various detector configurations, resolutions, layouts etc. These tools, sometimes referred to as 'hand calculations' or 'fast Monte Carlo' will keep playing an important role when either a quick turn around is needed or for cross checking purposes.

Detector Geometry Definition

This task is to include in the GEANT-simulated apparatus of the experiment the latest and most accurate/realistic geometry of HFT (IST and PIXEL), since this is the only way to ensure reliability of the resulting efficiency numbers. This task also includes the definition of the active areas of the detector, the hit information and the global positioning matrices of the detector. It has been recently realized that for certain studies (e.g. layer optimization studies, overall tracking efficiencies, 'quick' feasibility studies etc), a simplified version of the geometry could be very useful, a version where average material thickness is included but without detailed outline of the discreet components (cables, ICs, ladder support etc).

Detector Response Simulators

The detector response simulation packages in STAR reside outside the Geant framework. They are actually invoked at the event reconstruction step. Typically there are two or three categories of response simulators: a) *Fast simulators*, which smear the hit position coordinates and assign hit uncertainties based on parameterized analytical functions. The fast simulators run extremely fast and are good for quick studies that do not need detailed implementation of the detector. They are also relatively easy to imlement; we already have an HFT fast simulator in place for all syb-systems, b) *Slow simulators,* which simulates hits at the ADC level (usually obtained from sampling parameterized response functions. A slow simulator is a must when accurate acceptance and efficiency numbers are requested in physics analysis. A slow simulator is also used in embedding as discussed below, and c) *Very Slow simulators*, which track individual electrons through the detector body; from their generation to the readout. This is usually very time

consuming and one utilizes this method only in small-scale productions in order to determine or verify the functions used in the first two methods.

A Slow Simulator for the IST detector

The technology similarities between the SSD and IST (both silicon strip detectors with similar Si wafer thicknesses but with SSD being a double-side, crossed strip detector and IST single-side, shorter strip detector) could be beneficial in developing a slow simulator for the IST. The currently under development SSD code could be modified and adapted for the IST needs.

A Slow Simulator for the PIXEL detector

The detailed simulation for STAR Heavy Flavor Track PIXEL silicon detector consists of 4 steps. First, use the information of a charged particle passing through the PIXEL as inputs. The information contains the particle momentum, incident direction, path length in the PIXEL, and the sum of electron-hole pairs it generates. The total number of electrons generated from charged track passing through the silicon sensor is calculated using Bichsel distribution[34]. Second, build the geometry of the detector: one chip of 640 x 640 PIXEL array. One PIXEL is 30um x 50um x 30um, consist of four different layers from top to bottom: Readout electronics layer, diode layer, epitaxial layer and substrate layer. Third, simulate the transportation of electrons generated in the PIXEL[35]: diffusion, recombination and reflection at interfaces between different layers. A Gaussian equation is used to describe the diffusion as a random walk process. The electron recombination rate is dependent on the different doping density of different layers. Finally, calculate the distribution of electrons collected in the PIXEL array as output signal. The left panel of Figure 65 presents the simulated pixel cluster shape from 1GeV charged pion incident at 45-degree angle. The right panel of the figure shows the comparison of the deposited number of electron profile from data [35] and simulation. The two results agree with each other very well. The major problem for this slow simulator is the speed. It takes about 20 minutes to simulate a single charged track and it comes mainly from simulating the electron diffusion process. This is too slow to be used in future large-scale simulation studies.
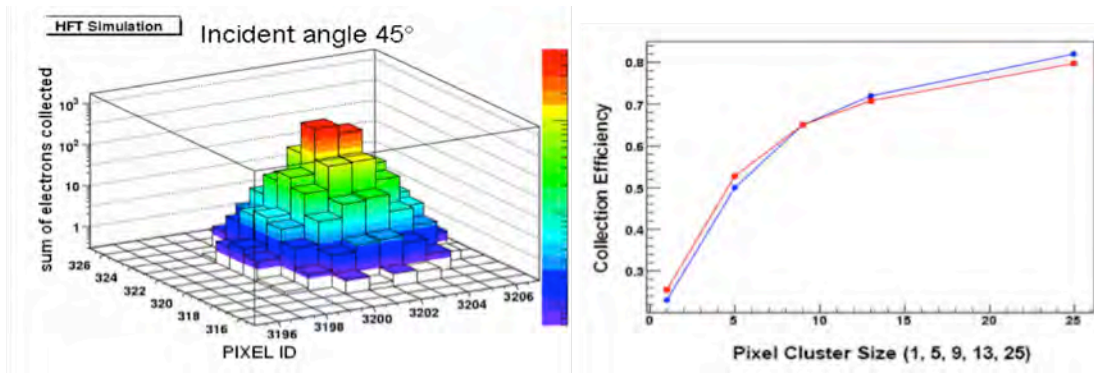
Figure 65: (Left) distribution of number of deposited electrons on pixels from a single charged pion with 45 degree incident angle from the slow simulator; (right) profile of the fraction of deposited number of electrons from simulation (blue) and data [35] (red).

To significantly improve the speed while keeping good accuracy, we developed a simplified method. Instead of simulating diffusion process step by step for each single electron, we calculate the probability distribution function for each electron in a specific space location to be collected by different pixels. Since any electron generated in the PIXEL is independent from each other, by randomly sampling this probability distribution function, we can decide which pixel collected this electron or if the electron recombined before being collected. Following above steps, we collect the pixel IDs that absorb all electrons along a charged track and add them up to obtain the number of electrons deposited in each pixel. To implement this method, we built a fine 3-D grid in a single pixel and calculated the probability distribution function for electron produced from all grid points using the slow simulator. For any one electron from incident charged track, we directly use the probability distribution function for the grid point that is closest to its production point to determine the pixel ID that collected this electron. Since all PIXELs are identical, we only need to make coordinate transformation if any electron is produced outside the pixel where the grid is built and repeat the same operation to finish the whole simulation for a charged track. The speed of the simplified simulator is a few seconds per charged track. The accuracy depends on the granularity of the grid and can be very good with high granularity. However this speed is still too slow to be used in simulation a central Au+Au collision which generates a few thousands of charged tracks. We are developing the third version of the simulator aiming to increase the speed by two orders of magnitude while keeping good accuracy.

Embedding and Pile-Up

The embedding of simulated tracks into the raw data stream (which provides the best 'background environment' for track/particle reconstruction and therefore the best way to estimate accurate efficiency numbers for physics analysis) has been around the heavy ion community for about fifteen years. It is the merging, at the raw ADC level, of a pedestal-subtracted event, for a given detector, with a few, slow-simulated hits. The resulting output is then passed through the reconstruction chain and the output is compared to MC input (this step is performed by the so-called Association Maker in STAR experiment).

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During the merging of real data with simulated hits and tracks one read the appropriate calibration tables so the dead areas of the detectors are properly excluded.

IST Embedding

As we mentioned above the IST could benefit from existing or under development SSD embedding code and adapt it with minor modifications

PIXEL Embedding and Pile-up simulation

The embedding task in the PIXEL layers is more complex since cluster and hit finding is done online. Also, in simulations, one has to properly account for out-of-time events, Pile-up hits. To simulate the PIXEL pile-up hits, we produced one standalone ROOT file containing only the required PIXEL hits multiplicity in both inner and outer layers. The hits are produced from GEANT using the same setups as in the production for CD0 simulation. The hits in this file are then merged with the PIXEL hits in every central collision that is pushed through STAR reconstruction software.

According to the CD0 proposal, the pileup hits density for 1x RHIC-II luminosity is $43/cm^2$ on the inner PIXEL layer and $6/cm^2$ on outer PIXEL layer. The pile-up hits densities under different assumption on the RHIC-II luminosity are listed in the following table. For each of the assumed luminosity, we produced one pile-up hits file.

luminosity	Inner later pile-up hits density	Inner later number of pile-up hits	outer later pile-up hits density	outer later number of pile-up hits
0.5xRHIC-II	21/cm2	6600	3/cm2	2638
1xRHIC-II	43/cm2	13514	6/cm2	5276
2xRHIC-II	86/cm2	27000	12/cm2	10550
3xRHIC-II	129/cm2	40500	18cm2	15826

This method neglects the fluctuation of pile-up hits density in different location of PIXEL detector since for every event, only one set of pile-up hits is applied. In the future, we plan to directly apply white noise on the PIXEL detector before reconstruction happens. This will include the local density variation and is an improvement to the old method.

Association Makers

The step of association comes directly after the embedding. Its basic functionality, which already exists in the STAR framework, is to correlate the MC input with the reconstructed output so one can calculate hit, track, decay-vertex etc finding efficiency. This is done either through the use of an embedded key (idtrue) in the hit structure or by 'proximity association' of reconstructed and MC clusters. The later one is less accurate and not suitable for our purposes. Currently the Association software generates a structure that contains enough correlated (matching) information to allow hit/track and partial decay-vertex evaluation. The current output is usable but not optimized for our

purposes; one has to go through several steps in order to be able to perform a detailed evaluation. The current scheme will need to be modified or augmented to include vital information that will facilitate our work.

Analysis of Simulated Data

There are software modules needed exclusively during the evaluation of simulations, either full-event simulations or embedding. These are in general smaller, utility-type pieces of code. Most of these modules already exist in some form and it is a minor effort to adapt them to HFT.

4.6.5. Physics Analysis Framework

The physics analysis software is the most critical part in signal extraction. When it comes to physics analysis people use a diverse set of tools and methods to extract the physics signals, most of them developed by themselves. Most of the tools and infrastructure needed is either already in place or under development in current charm analyses. Here we will only indentify the broad areas of physics interests for the HFT mainly for the purposes of recording the institutional interests, responsibilities and commitments. These areas are: a) Charm-meson, b) Charm-baryon, c) B-meson reconstruction and d) possible spin-related signals. These are the areas discussed in the next Section.

4.6.6. Institutional Responsibilities

Institutional commitments

The following discussion reflects and summarizes the software interests of the participating institutions at the time of writing of this CDR. Even though it is possible that institutional interests might get modified and shifted with time, it is expected that institutions with responsibility in key software areas (as discussed above) will provide the manpower needed to deliver their modules.

Resources required

From a review of the required tasks one can categorize the required resources into two broad categories: a) effort contributed by the participating institutes and b) effort expected from collaboration resources. A first estimate is that HFT institutions should contribute at least the equivalent constant effort of three FTEs for the lifetime of the project (about a decade), and the collaboration the equivalent constant effort of about one FTE, mainly in infrastructure areas (simulations, tracking, databases etc). The collaboration areas of contribution appear under the BNL institution label in Table below.

Institutional Responsibilities and Commitments

After consultation with the institutional representatives the following Table summarizes their current interests and commitments to software tasks as outlined and discussed above. At this point only a broad categorization and grouping is attempted and not a detailed outline of commitments within a more general task. Details of implementation will be discussed and defined in the group's weekly meetings.

Software task		BNL	UCLA	KSU	NPI	MIT	LBL	Purdue	
Online									
	IST					X			?
	Pixel						X	X	?
Offline									
Hit Reconstr.	IST					X			
	Pixel						X	X	?
Tracking		X							?
Event Vertex		X		X	X				
Decay Vertex		X		X	X				
Calibration Db	IST					X			?
	Pixel						X	X	
Alignment	IST	X		X		X			
	Pixel	X		X			X	X	
Simulation									
Geometry	IST	X				X			
	Pixel	X					X		
Fast/Slow Sim.	IST			X		X			
	Pixel						X	X	
Embed./Pileup	IST			X		X			
	Pixel						X	X	
Assoc/Analysis		X		X	X				
Physics Analysis									
Charm			X	X	X		X	X	
Bottom			X				X	X	
Λ_C				X	X		X		?
Spin							X		

Other collaboration contributed resources

4.7. Cost and Schedule

5.   Resources

6.   Appendix 1

6.1.   Description of the Pixel RDO System

This document is an extension of the Pixel RDO addendum to the HFT proposal. It is intended to give detailed parameters of the function of the Pixel readout system that will allow for the understanding of the logic and memory and requirements and the functionality of the readout system. We will present the designs of the Phase-1 and Ultimate readout systems under periodic triggering conditions. The simulation of the system response to random triggering of the type expected to be seen at the STAR experiment is ongoing and will be available upon completion. The readout design is highly parallel and one of the ten parallel readout systems is analyzed for each system.

6.1.1.   Phase-1 Readout Chain

The Phase-1 detector will consist of two carrier assemblies, each containing four ladders with ten sensors per ladder. The readout is via parallel identical chains of readout electronics. The relevant parameters from the RDO addendum are reproduced in Table 17.

Item	Number
Bits/address	20
Integration time	640 μs
Hits / frame on Inner sensors (r=2.5 cm)	295
Hits / frame on Outer sensors (r=8.0 cm)	29
Phase-1 sensors (Inner ladders)	100
Phase-1 sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5

Table 17: Parameters for the Phase-1 based detector system used in the example calculations shown below.

The functional schematic of the system under discussion is presented in Figure 66.
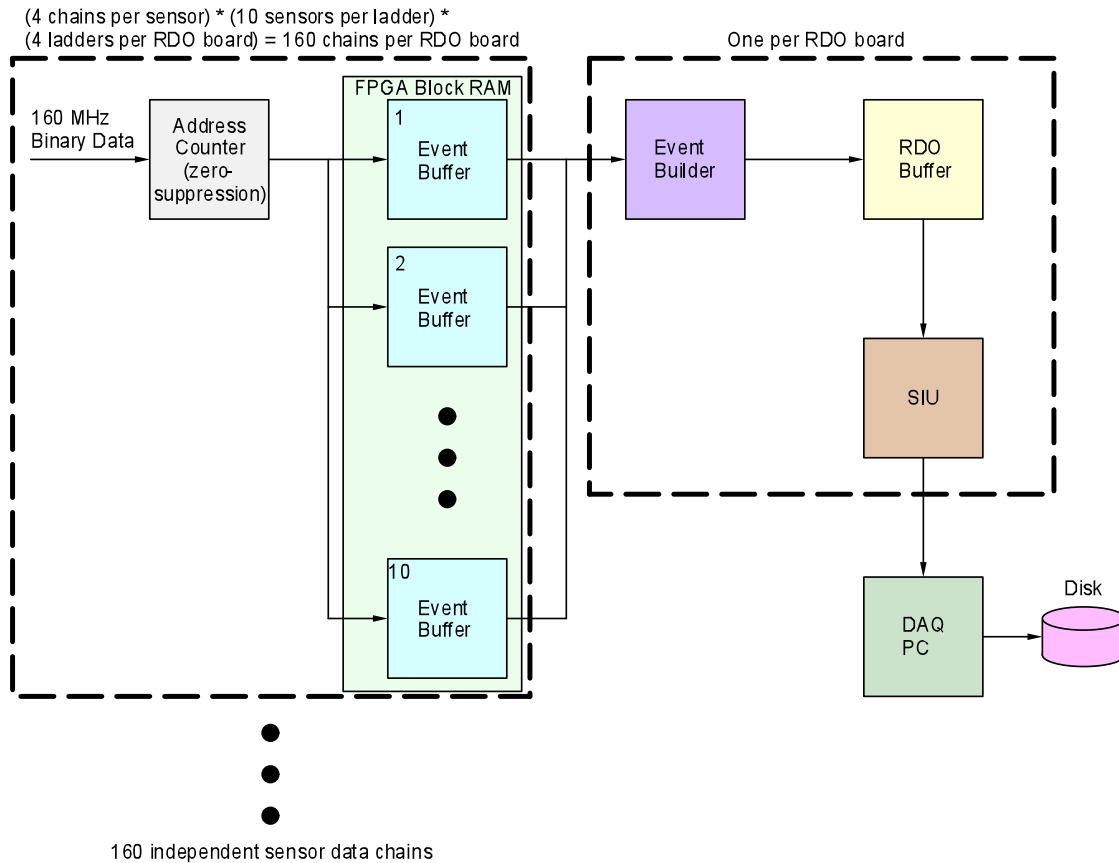
Figure 66: Functional schematic diagram for one Phase-1 sensor based RDO board. Each RDO board services one inner ladder and 3 outer ladders. Each ladder contains 10 sensors.

We will show the system function for two cases. The first is for a periodic trigger rate of 1 kHz. The second is for a periodic trigger rate of 2 kHz. These cases make the scaling clear. In both cases we will use the average (pile-up included) event size. We are currently simulating the dynamic response of the system to the triggering and event size fluctuations seen at STAR and will make this information available after the simulations are completed. It is important to note that the system is FPGA based and can be easily reconfigured to maximize the performance by the adjustment of buffer sizes, memory allocations, and most other parameters. The relevant parameters of the system pictured above are described below;

Data transfer into event buffers – The binary hit data is presented to the address counter at 160 MHz. The corresponding hit address data from the adders counter is read synchronously into the event buffers for one full frame of a 640 × 640 sensor at 160 MHz. This corresponds to an event buffer enable time of 640 μs.

Event Buffers – Each sensor output is connected to a block of memory in the FPGA which serves as the storage for the event buffers. Each block of memory is configured as dual ported RAM and. The overall FPGA block RAM used per sensor output is sized to allow for storage of up to ten average events with event size fluctuation. This leads to a total buffer size that is 20 × the size required for the average sized event (different for inner and outer sensors). The FPGA block RAM will be configured with pointer based

memory management to allow for efficient utilization of the RAM resources. The average inner sensor has 295 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (295 hits) × (20 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 7,375 bits. Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each inner sensor output is 73,750 bits or 3,688 20-bit addresses**.

For outer sensors, the event buffer size is calculated similarly. The average outer sensor has 29 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (29 hits) × (20 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 725 bits. Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each outer sensor output is 7250 bits or 363 20-bit addresses**.

Data transfer into the RDO buffer via the event builder – This process is internal to the FPGA, does not require computational resources, and can run at high speed. In the interests of simplicity, we will assume a 160 MHz clock to move data in 20-bit wide address words. The event builder first adds a 128 Byte header that contains the trigger ID and other identifying information into the RDO buffer, and then moves the address data from the event buffers into the RDO buffer in 20-bit words. The average carrier event size is [(29 hits / sensor (outer)) × (10 sensors) × (3 ladders) + (295 hits / sensor (inner)) × (10 sensors) × (1 ladders)] × (2.5 hits / cluster) = **9550 address words (20-bit)**. The RDO buffer is 5 × the size required for an average event and is thus **955 kb** in size. The full time required to transfer the address data into the RDO buffer (in 20-bit per clock transfers) is then **59.7 μs**.

Data transfer from the RDO buffer over the DDL link – The RDO buffer is dual-ported and thus readout from the SIU to the RORC can proceed as soon as the RDO buffer begins filling. The data transfer rates for the SIU – RORC combination as a function of fragment size are shown in Figure 67.
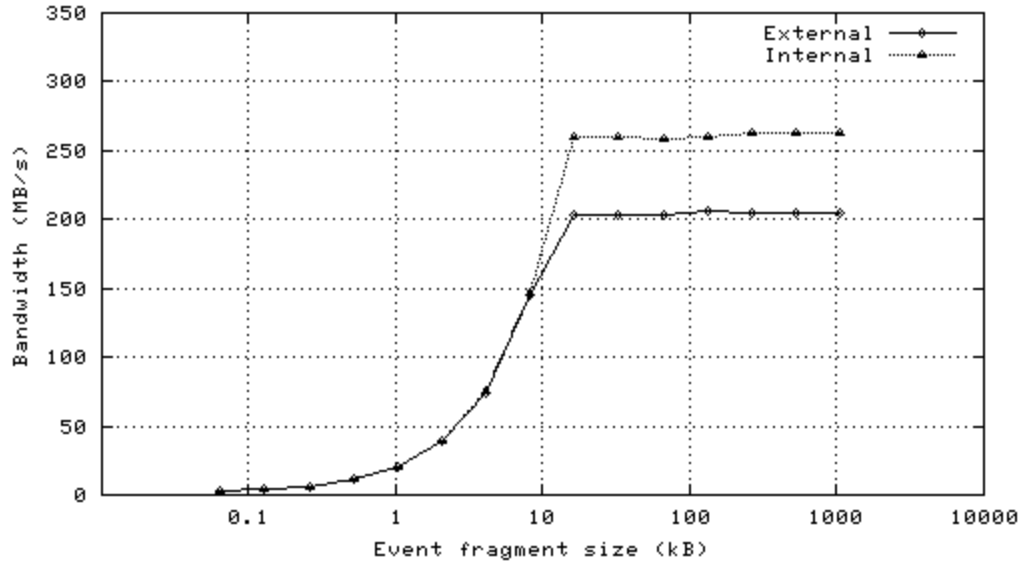
Figure 67: Bandwidth of a single channel of the SIU - RORC fiber optic link as a function of event fragment size with an internal and external (DDL) data source using two D-RORC channels. From the LECC 2004 Workshop in Boston.

In this case, we will assume that we are padding the 20-bit address data to 32-bit word lengths for DDL transfer. The event size is then (32 bits) $\times$ (9550 address words) **= 305.6 kb or 38.2 kB.** In this example, our transfer rate is ~ 200 MB / s. This transfer then takes **191 μs.**

Data transfer to the STAR DAQ for event building – The event data is buffered in the DAQ PC RAM (>4GB) until only accepted events are written to disk and then transferred via Ethernet to an event building node of the DAQ system. Level 2 trigger accepts are delivered to the RDO system and transferred via the SIU – RORC to the DAQ receiver PCs. Only the events that have been accepted by level 2 are then built into an event. In this way, the buffer provided by the DAQ PC RAM provides for the elasticity needed for an average event acceptance of 1 kHz

The results of these calculations and discussion are presented below in the chronograms in Figure 68 and Figure 69.
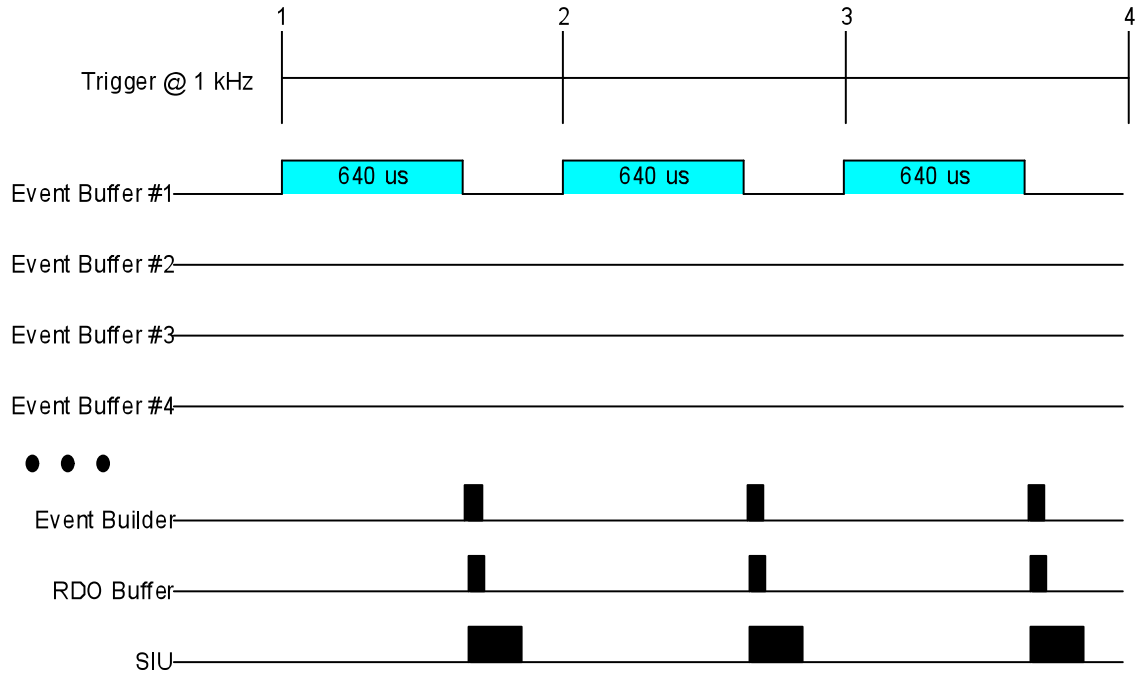
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Figure 68: Chronogram of the Phase-1 based readout system functions for a 1 kHz periodic trigger.
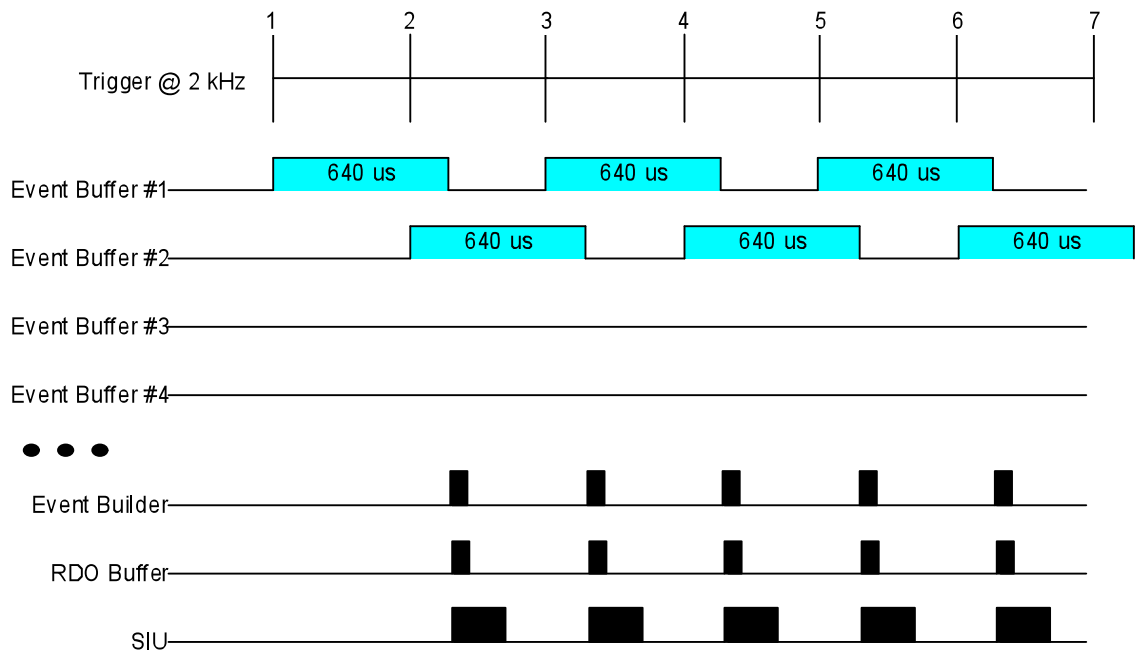

Figure 69: Chronogram of the Phase-1 based readout system functions for a 2 kHz periodic trigger.

The memory resources required in the FPGA / motherboard combination for this readout design are (120 outer sensor readout buffers) × (7.25 kb per event buffer) + (262.5 kb for the RDO buffer) + (40 inner sensor readout buffers) × (73.75 kb per event buffer) + (955 kb for the RDO buffer)= **4775 kb**. The Xilinx Virtex-5 FPGA used in our design

contains 4.6 – 10.4 Mb of block RAM so the entire design should fit easily into the FPGA.

Ultimate Sensor Detector Readout Chain

Again, the Ultimate sensor readout system consists of ten parallel readout chains. The main difference between the Phase-1 sensors and the Ultimate sensors is the inclusion of zero suppression circuitry in the Ultimate sensor, thus only addresses are read out into the RDO boards. In addition, the integration time of the Ultimate sensor is 200 μs and there are two data outputs per sensor. These differences lead to the functional schematic of the readout system shown in Figure 70.
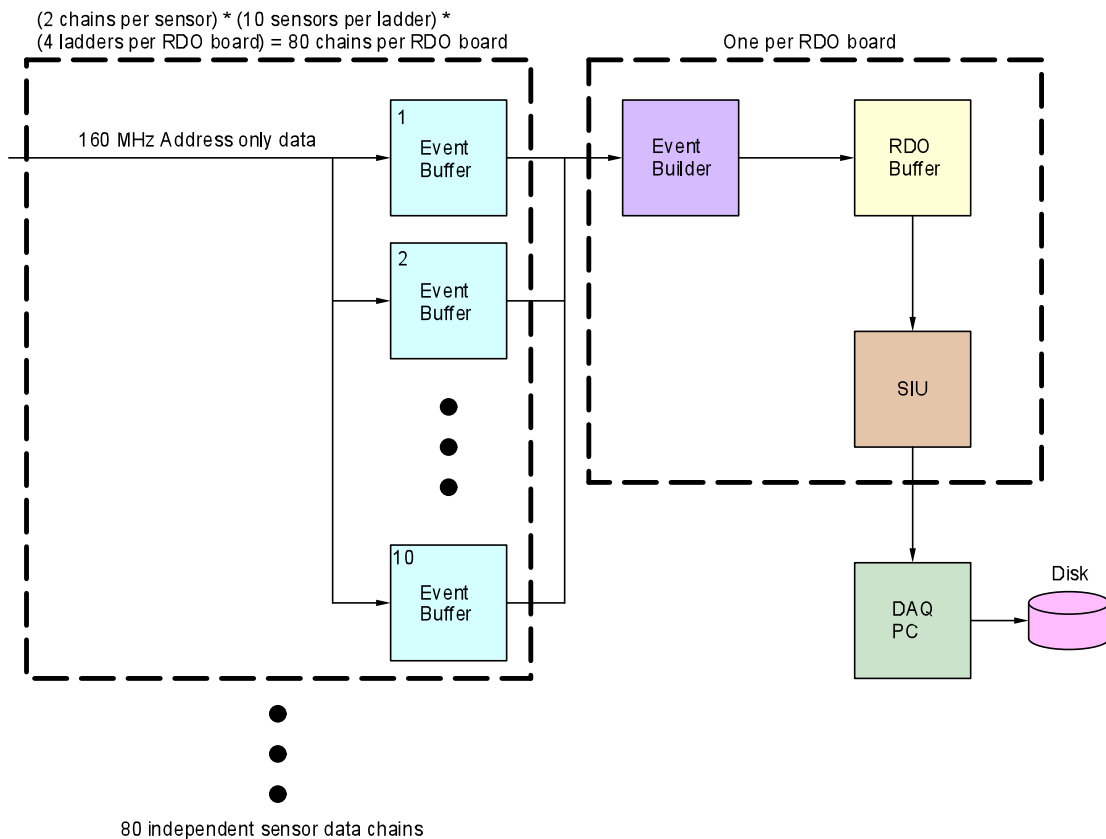

Figure 70: Functional schematic diagram for one Ultimate sensor based RDO board. Each RDO board services one inner ladder and 3 outer ladders. Each ladder contains 10 sensors.

We will show the system function for the same two cases as shown for the Phase-1 readout system. The first is for a periodic trigger rate of 1 kHz. The second is for a periodic data rate of 2 kHz. Again, in both cases we will use the average (pile-up included) event size. The relevant parameters of the Ultimate sensor based system pictured above are described in Table 18.

Item	Number
Bits/address	20
Integration time	200 μs
Hits / frame on Inner sensors (r=2.5 cm)	246
Hits / frame on Outer sensors (r=8.0 cm)	24
Ultimate sensors (Inner ladders)	100
Ultimate sensors (Outer ladders)	300
Event format overhead	TBD
Average Pixels / Cluster	2.5
Average Trigger rate	1 kHz

Table 18: Parameters for the Ultimate sensor based detector system used in the example calculations shown below.

Data transfer into event buffers – The 21-bitaddress data is presented to the event buffer 160 MHz. The integration time is now 200 μs giving an event buffer enable time of 200 μs.

Event Buffers – Again, we will calculate the amount of FPGA block RAM required for the event buffering. The average inner sensor has 246 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (246 hits) × (21 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 6150 bits. Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each inner sensor output is 64,580 bits or 3,075 21-bit addresses**.

For outer sensors, the event buffer size is calculated similarly. The average outer sensor has 24 hits / event. There are 4 outputs per sensor so the average inner sensor event address length is (0.25 sensor area) × (24 hits) × (21 bits) × (2 factor for event size fluctuations) × (2.5 hits per cluster) = 630 bits. Multiplying this event buffer size by 10 gives the size of the RAM required for the full set of event buffers required. **The event buffer block RAM size for each outer sensor output is 6300 bits or 300 20-bit addresses**.

Data transfer into the RDO buffer via the event builder –We will again assume a 160 MHz clock to move data in 20-bit wide address words. The event builder first adds a 128 Byte header that contains the trigger ID and other identifying information into the RDO buffer, and then moves the address data from the event buffers into the RDO buffer in 20-bit words. The average carrier event size is [(24 hits / sensor (outer)) × (10 sensors) × (3 ladders) + (246 hits / sensor (inner)) × (10 sensors) × (1 ladders)] × (2.5 hits / cluster) = **7950 address words (21-bit)**. The RDO buffer is 5 × the size required for an average event and is thus **835 kb** in size. The full time required to transfer the address data into the RDO buffer (in 21-bit per clock transfers) is then **49.7 μs**.

Data transfer from the RDO buffer over the DDL link – The RDO buffer is dual-ported and thus readout from the SIU to the RORC can proceed as soon as the RDO buffer begins filling. Again, we will assume that we are padding the 20-bit address data to 32-bit word lengths for DDL transfer. The event size is then (32 bits) × (7950 address words) **= 254.4 kb or 31.8 kB.** In this example, our transfer rate is ~ 200 MB / s. This transfer then takes **159 μs.**

Data transfer to the STAR DAQ for event building – Again, only the events that have been accepted by level 2 are then built into an event. In this way, the buffer provided by the DAQ PC RAM provides for the elasticity needed for an average event acceptance of 1 kHz

The results of these calculations and discussion are presented below in the chronograms in Figure 71 and Figure 72.
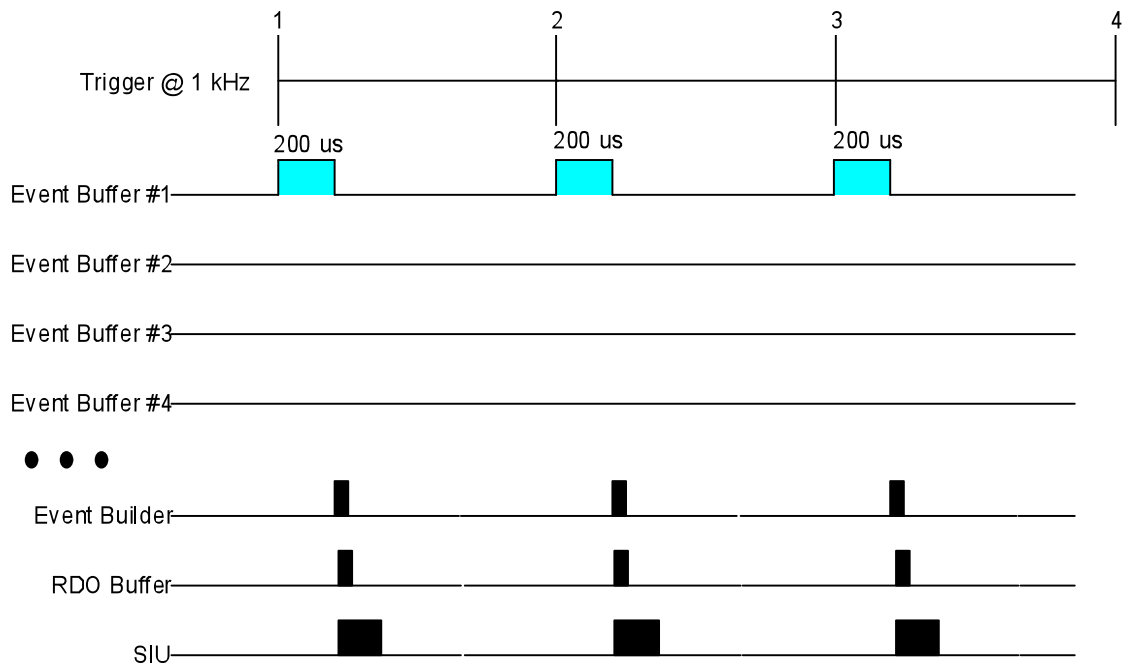

Figure 71: Chronogram of the Ultimate sensor based readout system functions for a 1 kHz periodic trigger.
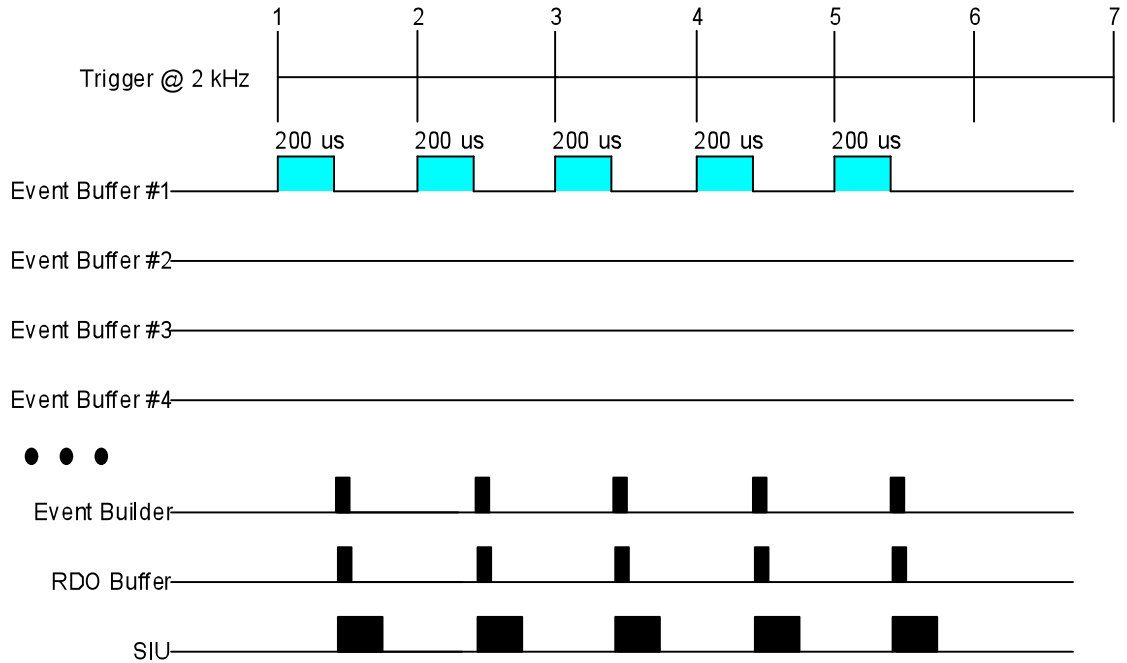
Figure 72: Chronogram of the Ultimate sensor based readout system functions for a 2 kHz periodic trigger.

The system memory resource requirements are somewhat less than those required for the Phase-1 RDO system. This fits easily into the memory resources of the Virtex-5 FPGA.

7.   Appendix 2

7.1.   Mechanical Design Simulation and Analysis

A number of mechanical design studies have been carried out to find designs that can meet requirements of stability and cooling. The work reported here has been carried out by either ARES corporation or us. These analyses are not complete at this time, but they provide a starting point for prototype work which can be expected to achieve the required performance.

7.1.1.   Ladder support Structural analysis

The mechanical design of the pixel support system must meet stringent position stability requirements while also minimizing radiation length. The basic support design analyzed is pictured in Figure 32, but some analysis are also reported for alternative designs that have been considered.

The issues investigated are:

- Ladder backing stiffness required to hold thinned silicon flat against it's tendency to curl

- Support strength to control gravity sag

- Support strength to control deformation from air flow pressures

- Control of thermal expansion induced deformation

- Control of moisture expansion induced deformation

- Support strength to handle insertion loads

Control of Silicon Curl

The pixel chips are mounted on flex cables with a composite backing and these ladders are mounted on a thin large moment carbon composite tubes shown as green in Figure 32. The tubes are the primary source of support and the ladder backers provide support for handling plus these backers must also provide support for the 1 cm overhang of the ladders. In the overhang region the backer provides the only mean for holding the thinned silicon chips flat. Without backing the silicon chips tend to curl as a result of the stresses imposed in the silicon during chip fabrication. A simple analysis shows that a 2 mil thick carbon composite will allow the silicon to curve out of plain by 700 microns. A thicker but less dense backer of perhaps open weave carbon composite that is 10 mils thick will limit the deformation to 30 microns while maintaining a 0.02% X_0 budget for the backer, namely the equivalent of 2 mils carbon composite. This deformation is outside of the 20 microns envelope, but the deformation will be mapped and the stability should satisfy the 20 micron specification.

Control of Gravity Sag

The most critical component for controlling deformation from a variety of sources is the sector tube shown in Figure 32. This structure is in the tracking path and thus requires the most attention to radiation thickness. Analysis of the sector tube control of gravity sag has been carried out by us and by the ARES corporation. The ARES analyses, included details of the composite weave, and showed that a sector tube could be fabricated with a thickness of 120 microns and more than satisfy our 20 micron stability requirement giving a gravitational displacement of less than 6 microns. We have performed a similar analysis, but with an isotropic modulus representation of the composite. This work shows a 5 micron deformation for the detector elements and 35 microns for other parts of the structure, but with the addition of an end lip the analysis gives a gravitational detector displacement limited to 0.6 microns and the maximum displacement of the structure is 4 microns (see Figure 73). These results show that gravity induced distortions are not a problem with this design. As will be shown other contributions to deformation are more significant.

Control of Airflow Induced Deformation

The deformation and vibration induced on the detector support from the cooling air flow requires more study, but preliminary considerations indicate that the current structure could be adequate. The planned cooling air velocity, 8 m/s, has a dynamic pressure that acting on the area of the structure is 1.7 times the gravitational force. From the gravity analysis we conclude that the static deformation will be less than 2 microns. Again, vibration studies with prototype structures and possibly computational fluid dynamics (CDF) simulations will be done.

Control of Thermal Expansion Induced Deformation

One of the greatest potential sources of deformation is differential expansion resulting from changes in temperature between powered on and power off. It is planned to spatially calibrate or map the detector structures in a vision coordinate machine with the power off and the structure should not deviate from the map while powered on during operation by more than 20 microns. This requirement was one of the main reasons for choosing the current design with its large moment of inertia and consequently large stiffness. The ladder and beam structure being examined is illustrated in Figure 31 and Figure 32. It was found that the main issue requiring control is the bimetal thermostat effect from differential expansion. The problem is the result of the very large coefficient of thermal expansion (CTE) of the kapton cable compared to the rest of the structure. An analysis of a short section of the ladder shown in Figure 74 illustrates the problem where in this case the thermally induced displacement is 500 microns at the edge of the silicon.

A thermal expansion analysis of ladders plus support shows that by using a very compliant adhesive (3M 200MP) the kapton cable is largely decoupled from the structure greatly reducing the thermal induced bending. Simulation results shown in Figure 75 give a maximum deformation of 9 microns, well inside of the 20 micron requirement envelope.
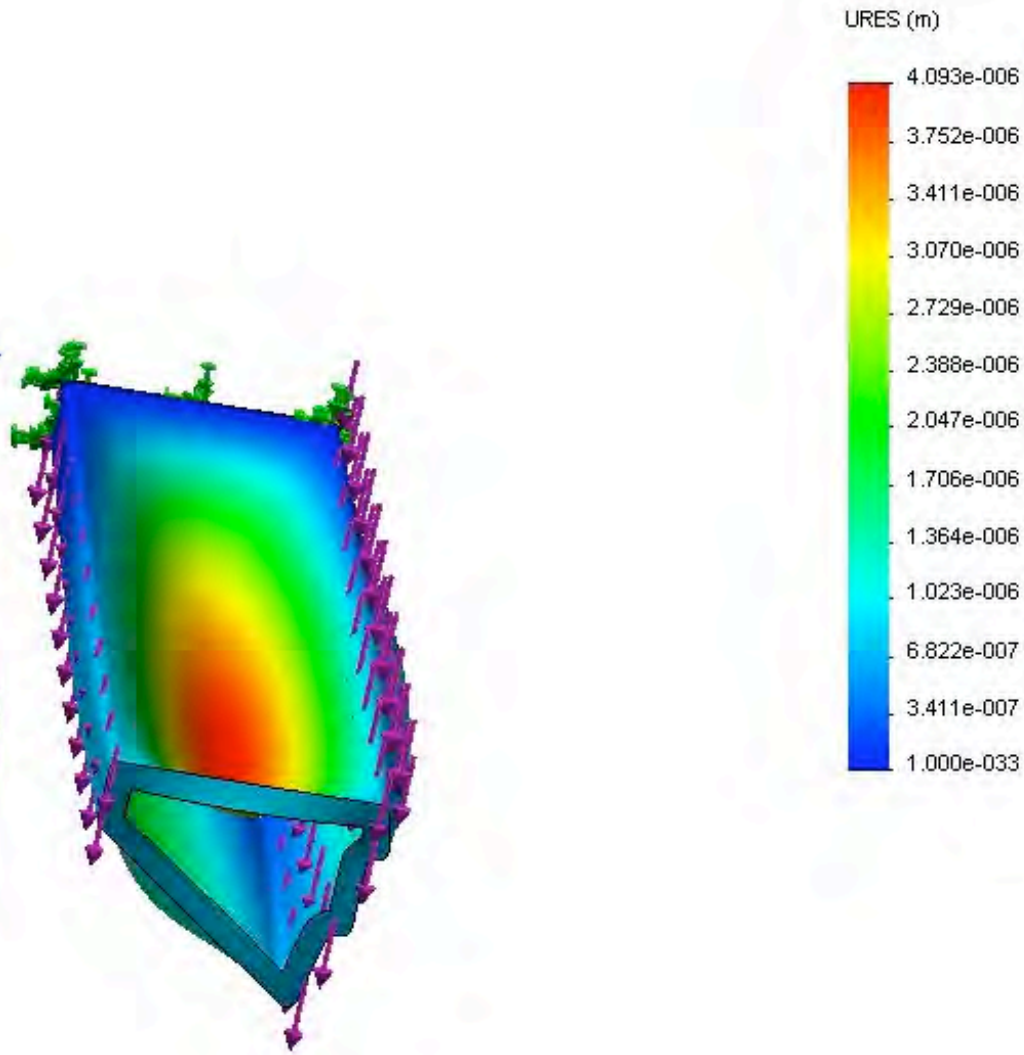
Figure 73: FEA results for gravity deformation of a 120 micron carbon composite support structure carrying 4 detector ladders.
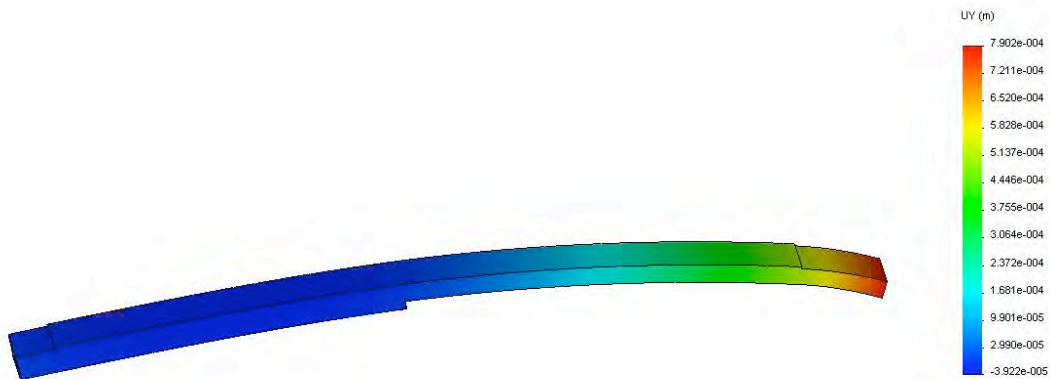

Figure 74: Short section of ladder structure showing problems with excessive thermal bimetal effect bending with using stiff adhesive. The 500 micron displacement resulting from a 20 deg C temperature change is driven by the large CTE of the kapton cable.
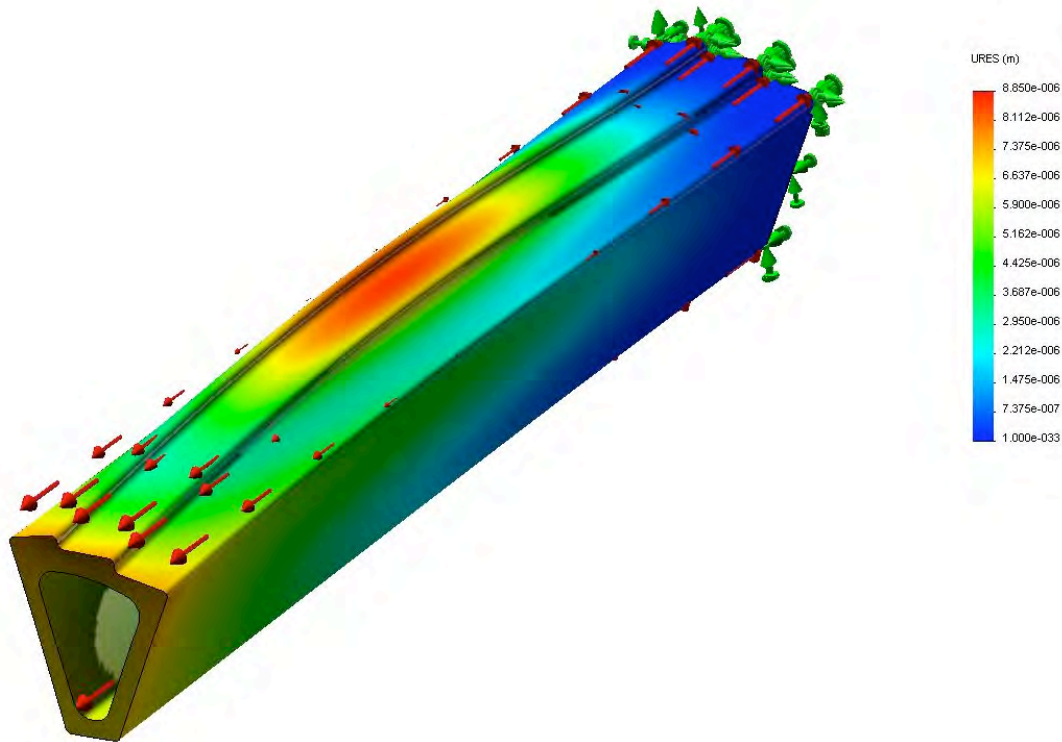
Figure 75: Thermally induced displacement of a sector beam with end reinforcement. The maximum resulting displacement is 9 μm. The beam and end reinforcement is composed of 200 μm carbon composite.

Control of Moisture Expansion Induced Deformation

The carbon composites expand with increased moisture content. There will be a long term reduction in the moisture content from the time of manufacture until completion of operation in the experiment environment which can potentially lead to unacceptable geometry changes. The ARES Corporation has studied this problem for us and has found a composite layup configuration that meets our 20 micron requirement. This work appears on p. 99 and 102 of their summary report. They recommend a laminate: YSH-50/EX-1515 with a layup: [0, +60, -60]. The FEA analysis gives a maximum displacement of 16 microns. Further analysis and prototyping is required to address this issue. The inclusion of a soft decoupling adhesive may help as it appears to help in the thermal case.

Support strength to handle insertion loads

When the detector is inserted into the final docking position in the center of STAR it engages spring loaded over center latches into the kinematic mounts. The insertion supports have much less stringent stability requirements than the detector ladders since the positioning only has to be good enough to lie inside the kinematic mount engagement window which is ~1 mm, but the support must be able to handle the cocking load of the latches which is on the order of 15 lbs. Displacements must also be limited such that the

two half detector cylinders do not collide during the insertion process. A FEA analysis of the supporting hinge structure has been done to check that it is adequate for cocking loads. The results of this analysis, shown in Figure 76, indicate that the design can safely handle the load without undue distortion. The analysis was not done on the latest complete hinge design, but an analysis of one part (see Figure 77) of the latest design shows that it is more than adequate.
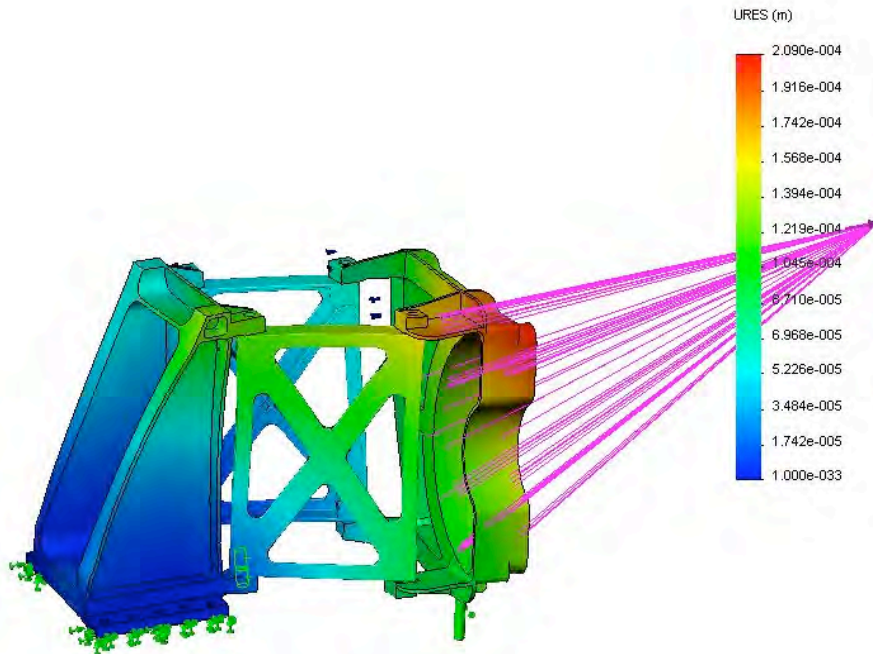

Figure 76:   Displacement of an early insertion hinge design under cocking load of the latching mechanism. The displacement in the image is magnified by 140 and the maximum displacement is 210 microns. The pink lines show the position of the remote load as it is carried through the D tube, not shown.

Model name: hinge back RP
Study name: test 2
Plot type: Static displacement Displacement3
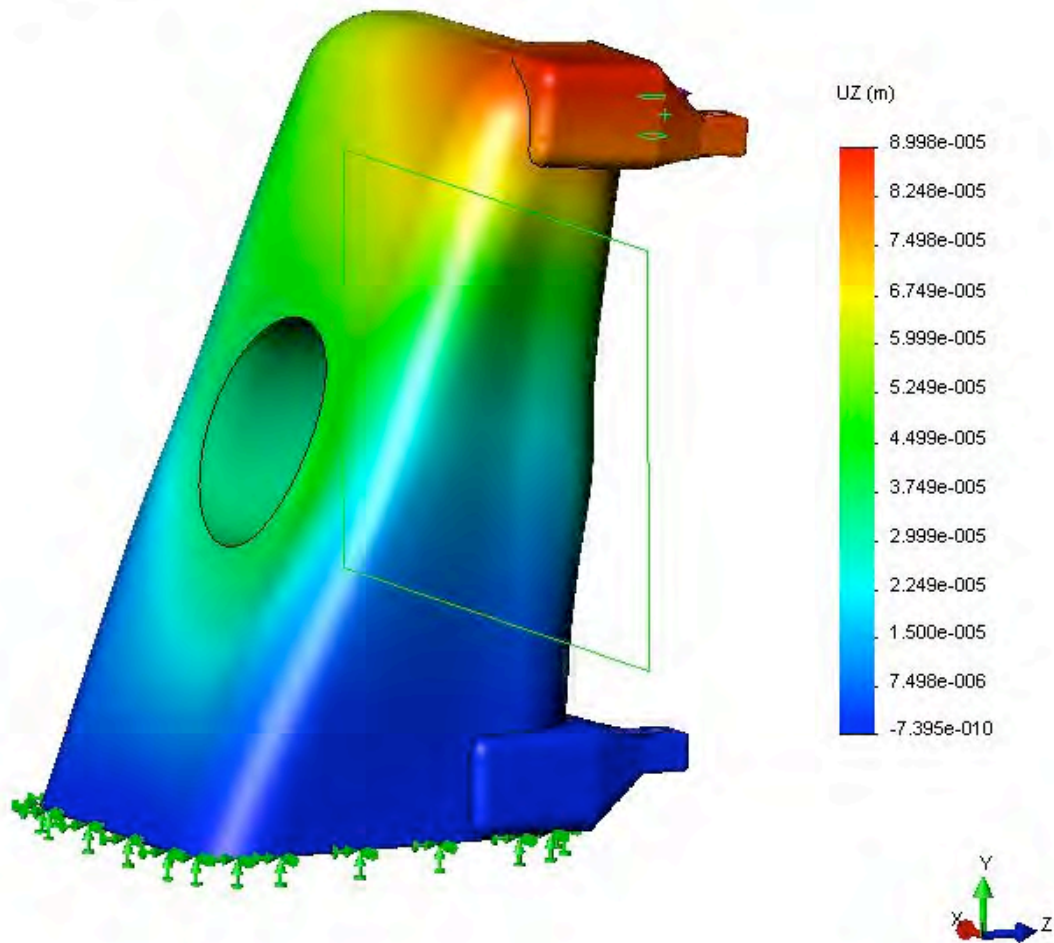Reference geometry: Front
Deformation scale: 206.067

UZ (m)

8.998e-005
8.248e-005
7.498e-005
6.749e-005
5.999e-005
5.249e-005
4.499e-005
3.749e-005
2.999e-005
2.249e-005
1.500e-005
7.498e-006
-7.395e-010

Figure 77: Distortion of support hinge backer under latch cocking load. The flexing in the beam axis direction is 90 microns.

Vibration of STAR central support

In STAR the central inner detectors such as the pixel detector are supported through the OSC and the ISC to TPC end caps. An accelerometer was mounted on the TPC end cap to measure possible vibrations that might couple to the pixel detector and affect position stability. A result from this measurement study (Figure 78) shows the response of a harmonic oscillator as a function of its resonant frequency to vibration if mounted directly on the end cap. This data can be used to set limits on expected vibration of various components and determine whether the performance of the detector is compromised. There are several components of the detector system which each have their own requirements with respect to stability and vibration.

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Consider first the vibration of one pixel sector ladder support with respect to the other. This case affects directly the pointing accuracy of multiple tracks to a vertex and therefore the full resolution is required and the vibration should stay below the 9 micron RMS requirement. The fundamental frequency for the sector can be obtained from FEA analysis which gave a 6 micron movement under gravity load. The fundamental frequency is

$$f = \frac{1}{-} \cdot \sqrt{\frac{g}{\cdot}}$$

or 200 Hz for the 6 micron sag under gravity. From Figure 78 this gives a RMS vibration of .04 microns which is completely negligible compared to our 9 microns requirement. This vibration from this source will actually be significantly less than this because the sector is not directly coupled to the TPC wheel. The less stiff OFC and IFC provide the connection reducing the high frequency coupling.
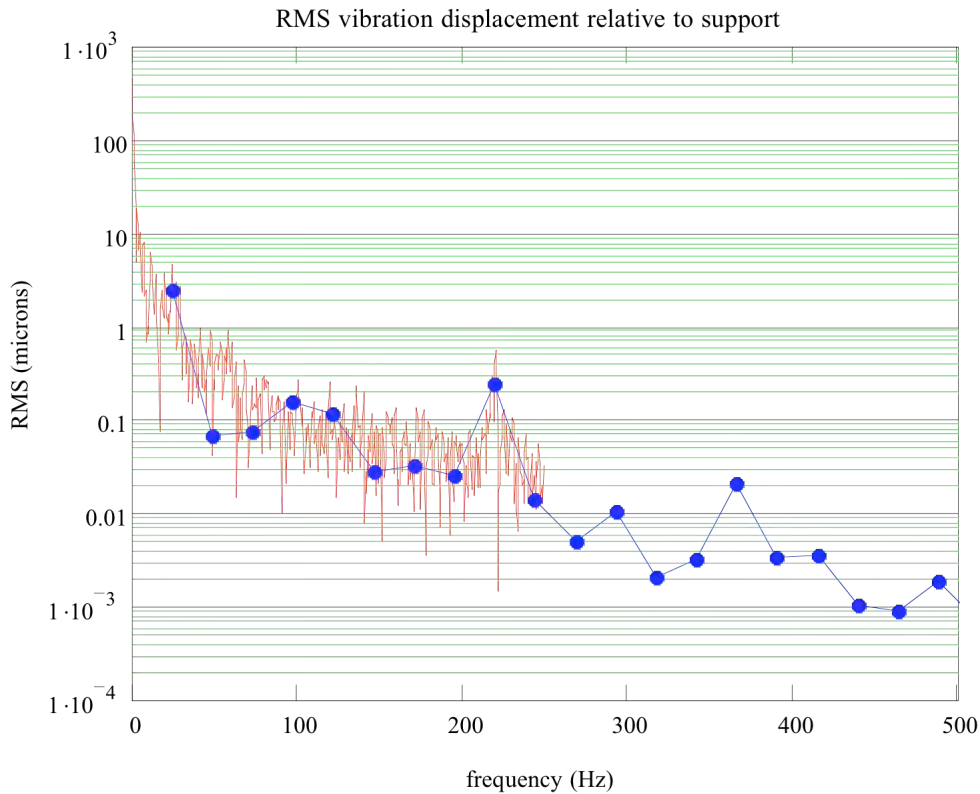

Figure 78: This shows the vibration response of mechanical harmonic oscillator mounted on the TPC end cap as determined with measurements of an accelerometer bolted to the TPC end cap. The two curves represent measurements made using two different methods of recording the data.

The next element to consider is the pixel half cylinder as a whole. The stability of this element is most important for track matching from the IST, so the stability of this element should be good enough that it does not compromise the IST pointing resolution, namely it should be less than 100 microns RMS. It is preferable though to be within the pixel limit

since there are overlapping pixels between the two half cylinders. The ARES analysis p. 144 gives a fundamental frequency of 110 Hz for the pixel half cylinder when supported on the kinematic mounts. This, according to Figure 78, gives a RMS vibration of 0.2 microns which again is insignificant.

Finally the vibration of the OFC can be checked. The stability of this element only has to be good enough to not compromise the TPC tracking precision which is ~ 1 mm. It is expected that the OFC will be built with a gravity sag of 1 mm or better which was the number for the old support cones that are being replaced by the OFC. The fundamental frequency for this displacement is 16 Hz which according to Figure 78 gives ~ 4 microns RMS vibration. Again, this is not an issue compared to the 1 mm requirement.

7.1.2. Ladder Cooling Analysis

Air cooling has been chosen for the pixel detector in order to minimize multiple coulomb scattering and a number of studies have been carried out to optimize the air cooling design. Original tests with a heated ladder in a fan driven air stream indicated that ladders with heat loads of 100 mW/cm^2 could be successfully cooled with a moderate air velocity. A study by ARES Corporation, p. 73 found that an airflow velocity of 8 m/s through the sector beam was sufficient to limit the silicon temperature rise above ambient to 13 deg C. To accomplish this however additional cooling fins required under the outer layer of silicon which adds mass and complicates construction.

Bi directional air flow cooling

Since then more extensive, but still preliminary, CDF modeling has been done with air flow over both the inner and outer surfaces of the sector structure. The cooling simulation was run for one sector out of the 10 sectors in the complete pixel cylinder. The air flow path is shown in Figure 38 and Figure 79.
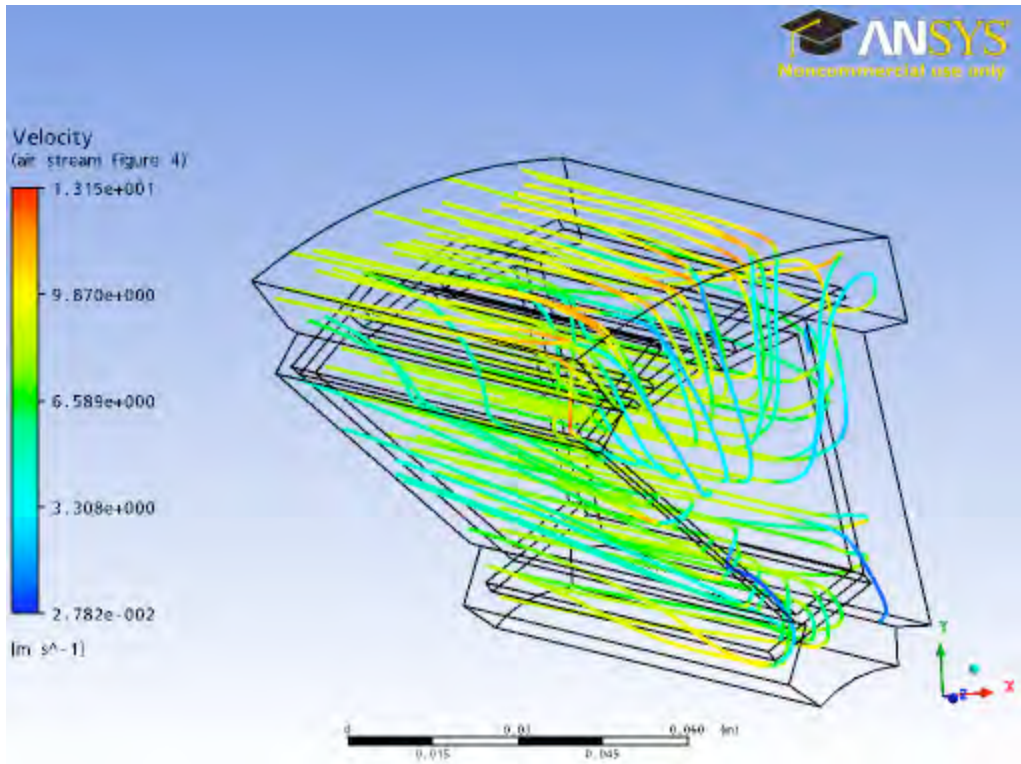
Figure 79: Stream lines showing the cooling air flow. The flow direction is from inside to outside. The color code shows air velocity.

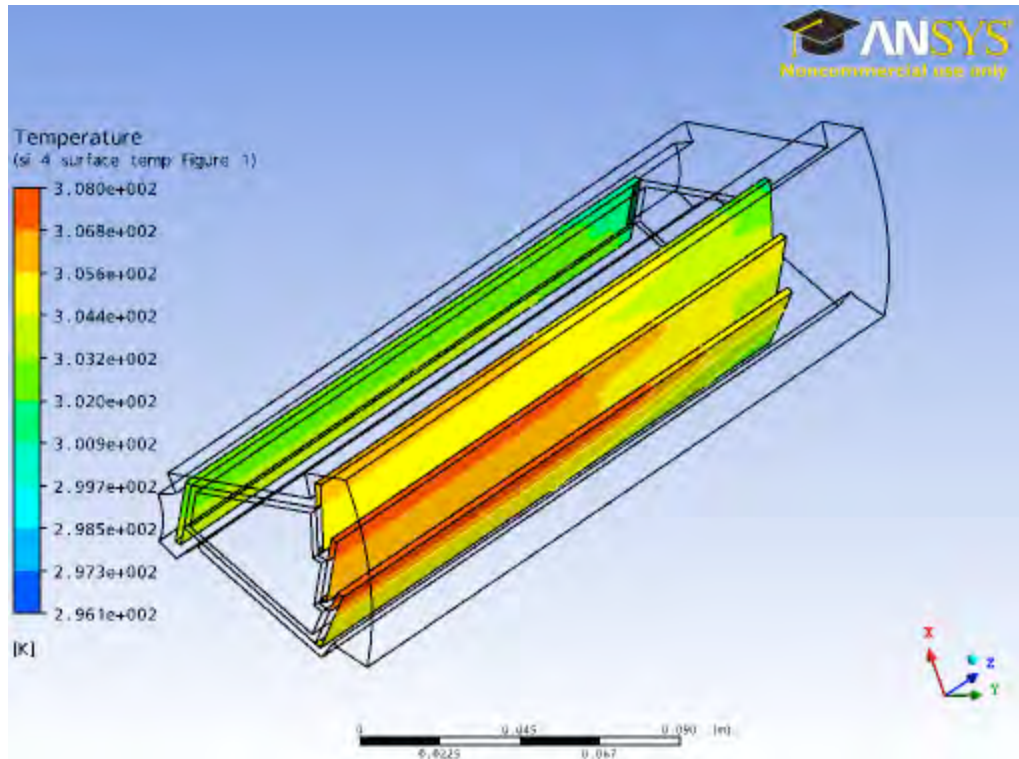The silicon surface temperature profile is shown in Figure 80.

Figure 80; Surface temperature of silicon ladders. The maximum temperature increase above ambient is 12 deg C. The cooling air flows across both the inner and outer surfaces. The air enters from the left on the inside of the support beam, turns around at the right and exits on the left.

In this case an input air velocity of 8 m/s was used. This results in a maximum silicon temperature rise above ambient of 12 deg C which is acceptable. It is interesting to note that the inside ladders next to the beam pipe cool more effectively than the outside ladders. This is because the surface area of the support beam sides provides a significant fraction of the cooling.

The total air flow in this case for the full pixel detector barrel is ~280 CFPM and the temperature rise in the air for the total power of the ladders, 240 W, is 1.5 deg. C. This is a very small rise in the air temperature, so alternatives can be considered with reduced total air flow which would result in a smaller air cooling system.

Alternative air flow design

An alternative design has been investigated with reduced total air flow volume and an increased air velocity at the surface to improve the heat transfer. In this design the high velocity air flow is in the transverse direction local to the ladder surface (see Figure 81). The air flows through narrow slits in the ladder support beam from outside into the sector beam.
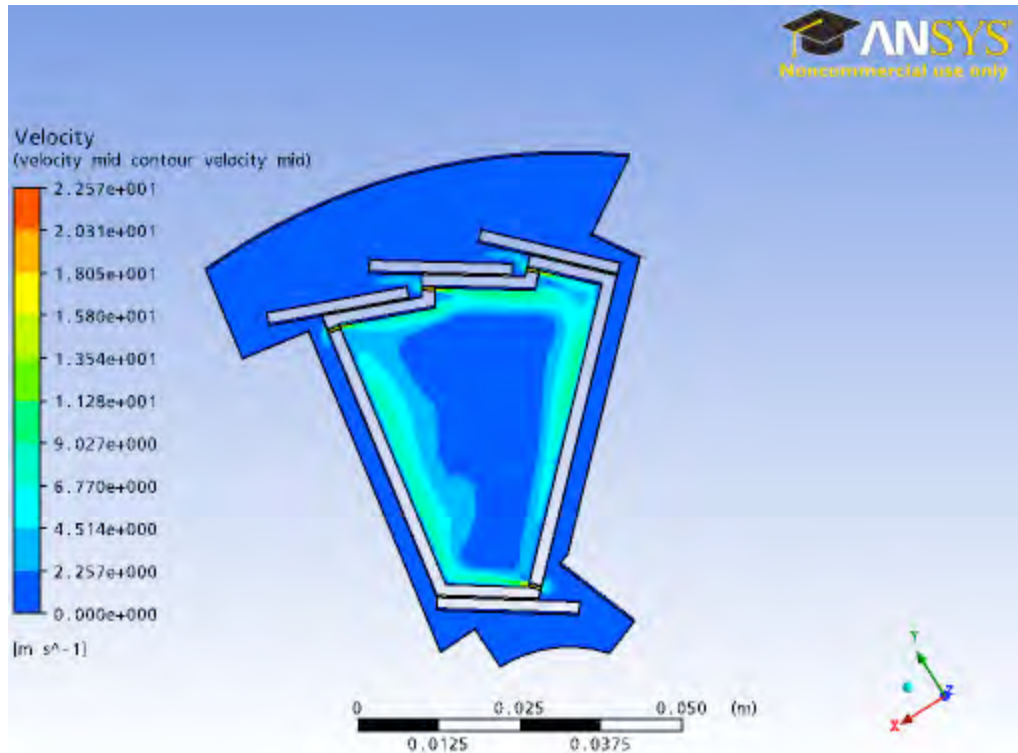
Figure 81: Sector cooling with transverse jets of cooling directed to the inside of the sector beam support structure through thin slots. The air velocity profile is shown in color. The air velocity near the surfaces beneath the ladders is 11 m/s.

The calculated surface temperature as shown in Figure 82 gives a maximum silicon temperature above ambient of 14 deg C. This is not quite as good as the performance with the simpler longitudinal bi directional cooling design with air flow over both inside and outside surface. For this reason future development will focus on the simpler longitudinal flow design.
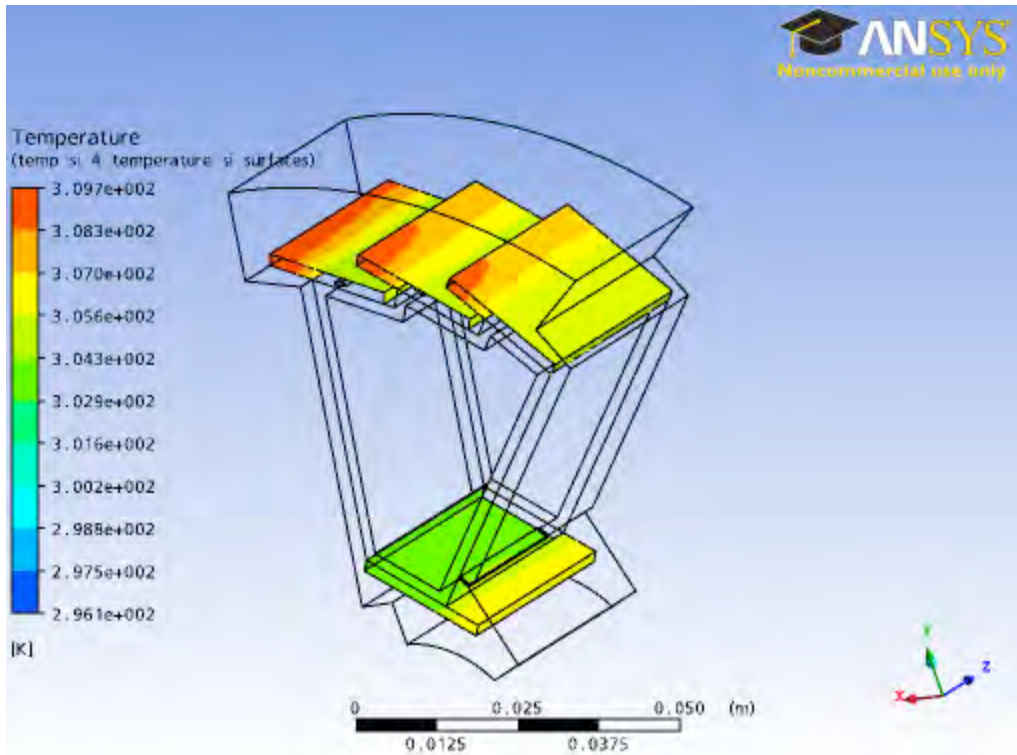
Figure 82: Silicon surface temperature profile for the transverse cooling jet design.

Air flow induced vibration

A mechanical finite analysis of the sector structure shows that there are multiple vibration modes close in frequency that can potentially be excited by the cooling air flow. Two design examples are shown in Figure 83 and Figure 84 in one case with a simple open end and another with a reinforced end. The reinforced end increases the resonant frequency making this the desirable choice.
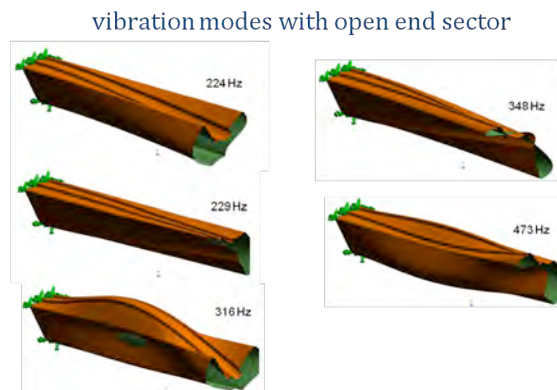

Figure 83 First vibration modes for an open ended sector. Frequencies are relative as composites properties in the FEA are not as built.

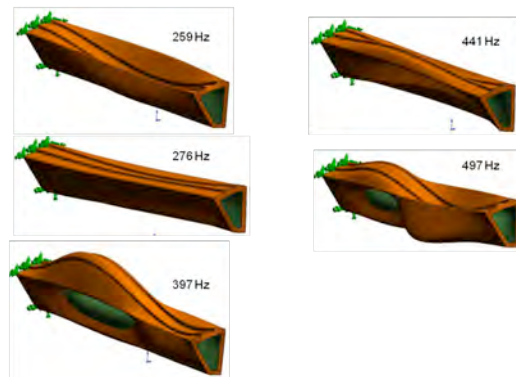vibration modes with reinforced end

Figure 84 First vibration modes for a sector with a reinforced end. Frequencies are relative as composite properties in the FEA are not as built

A single sector sized wind tunnel was built and used to measure the vibration of the sector structure when subjected to cooling air flow. The test structure, shown in Figure 85, is equipped with a sensitive capacitive probe to measure vibration, an air velocity probe and a vacuum cleaner to provide air flow.
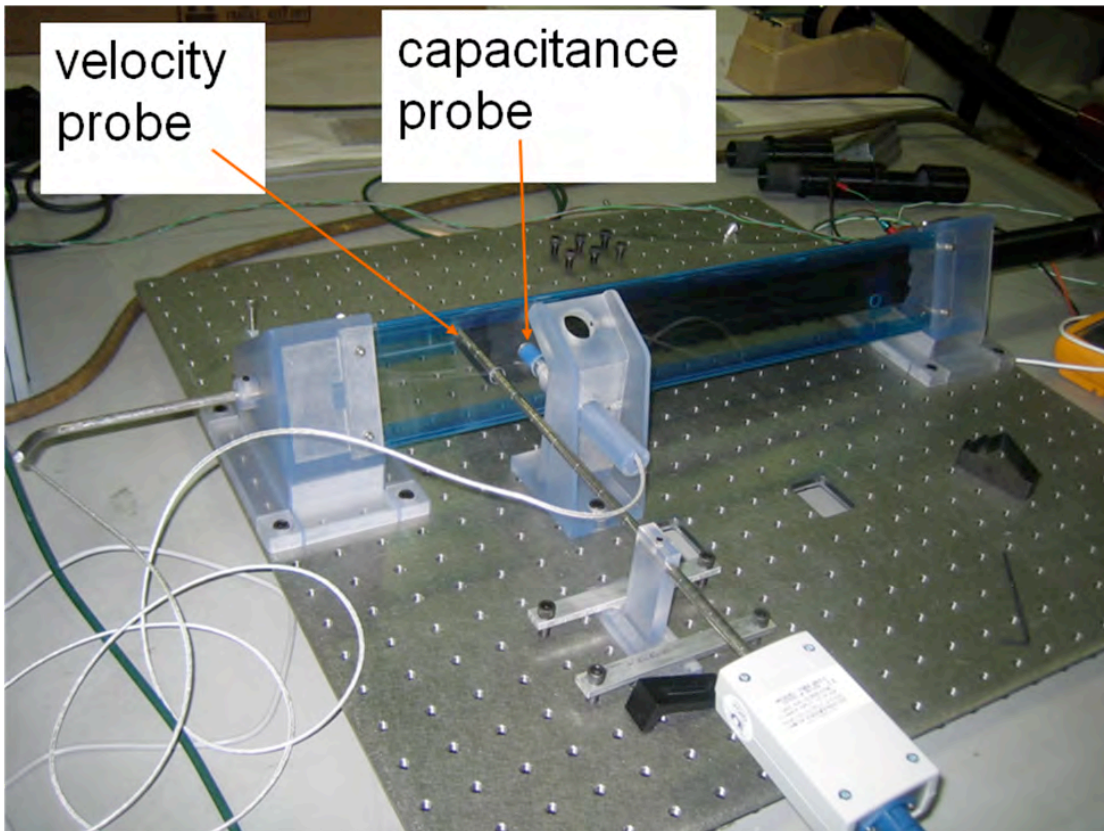

Figure 85 Wind tunnel to measure vibration of the sector structure induced by cooling air flow. The carbon composite sector under test weighs 21 gm. Additional weight was attached to include the effect of installed ladders

Figure 86 shows the measured rms amplitude of vibration of the middle outside ladder at the end of the unreinforced sector as a function of the air velocity. This measurement was made with the probes positioned as shown in Figure 85. The vibration amplitude is at the limit of the acceptable range. Additional measurements on both the open sector and the reinforced sector were made at multiple points as shown in Figure 87 with the desired air velocity required for cooling. For comparison the first FEA vibration mode shapes are shown, but amplitudes are not calculated. The numbers shown in the figure are the measured rms amplitudes which are well within our requirement limits.
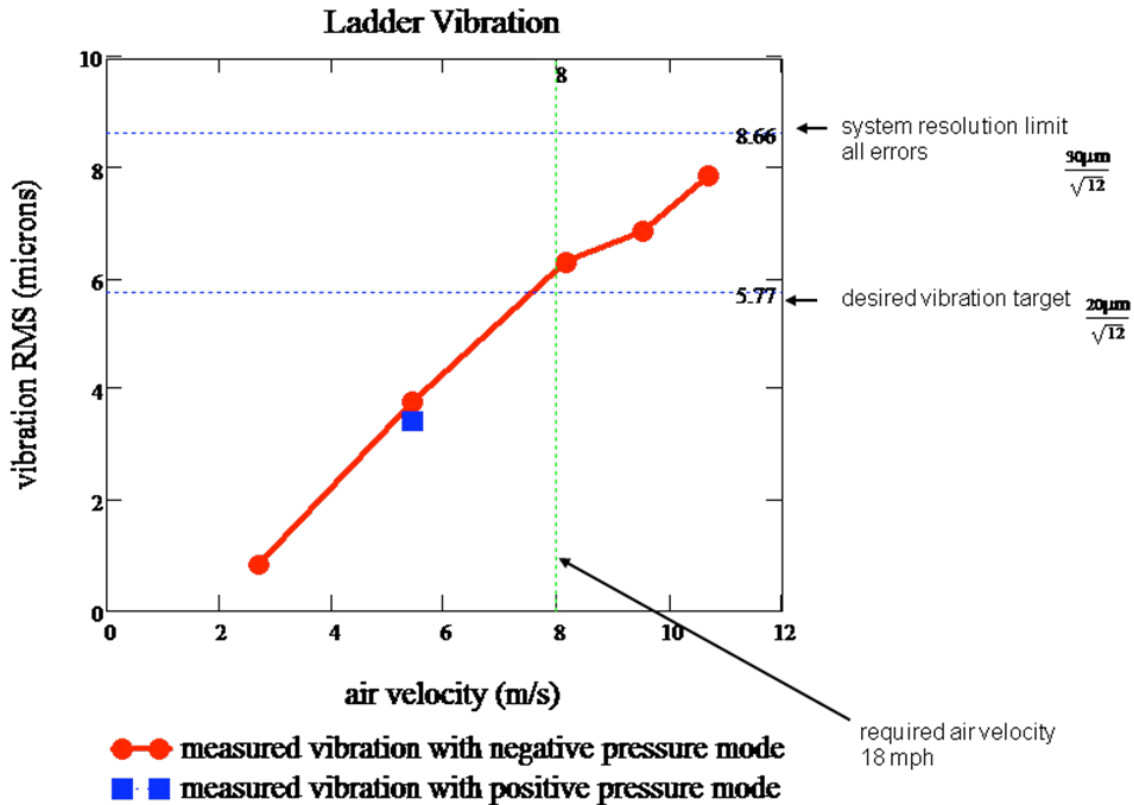

Figure 86 Measured rms vibration of the middle outside ladder position at the point of maximum vibration. The sector in this case was open ended, no reinforcement.
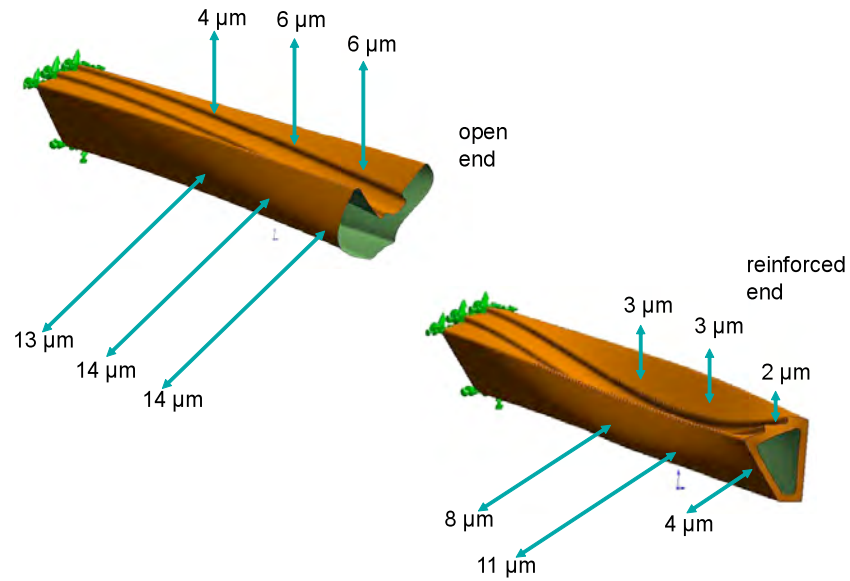
Figure 87 Measured vibration at several points on two sector designs, one with an open end and another with a reinforced end. The first vibration modes from FEA are shown for qualitative comparison. The top position measurements give the ladder vibration which is of interest because this affects the detector performance. The 3 micron value is well within our 20 micron requirement. The side vibration does not affect detector positions.

8.   Appendix 3

8.1.   LVDS Data Path Testing Discussion

The readout system architecture for the Phase-1 and Ultimate sensors to be used in the Pixel detector for the Heavy Flavor Tracker upgrade at STAR contains a high speed digital data path that is required to read out the sensor hits during the sensor integration time. This data path is well described in the addendum to the HFT proposal and can be found at http://rnc.lbl.gov/hft/hardware/docs/Addendum_rdo_2007_12_26.pdf. The RDO sensor data interface path requires that LVDS data move over a total distance of 6 – 8 meters with a speed of 160 MHz for Phase-1 and 125 MHz for Ultimate. 1-2 meters of this distance is over high impedance fine twisted pair wire. Since this design is challenging, though it works on paper, it is prudent to make a prototype set of testing boards and check the performance of our design as a precursor to starting a production design for the final set of readout boards. A diagram of the physical layout of the parts of the Pixel RDO system is shown as Figure 88.
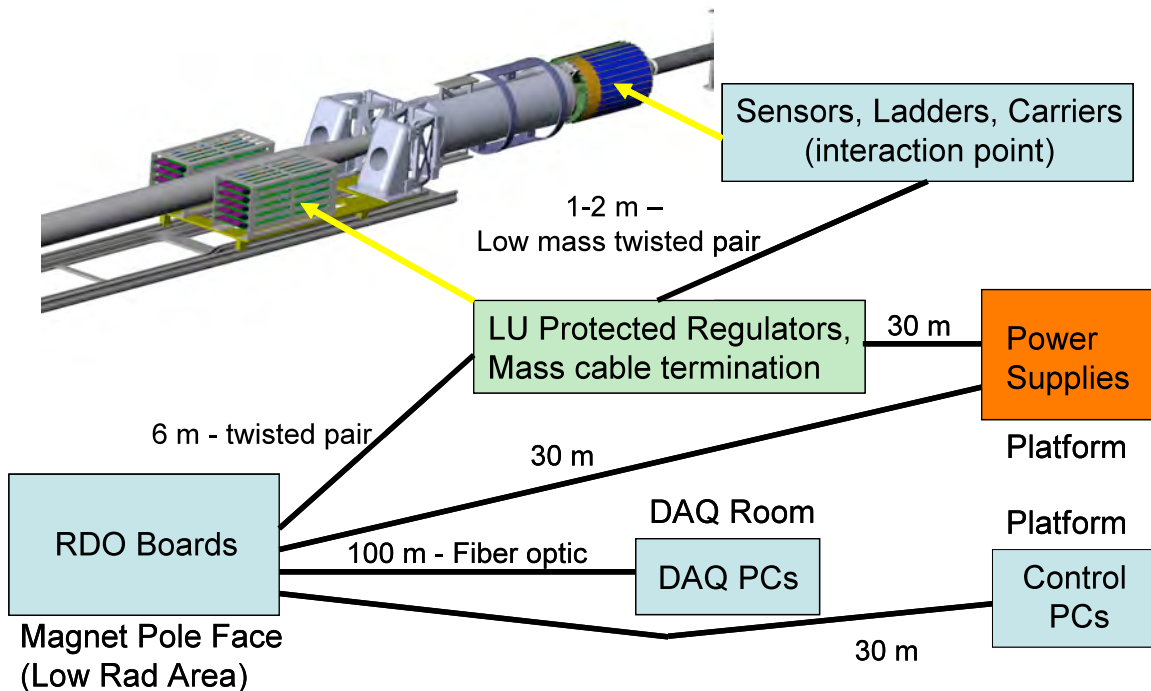

Figure 88: Physical layout of the RDO system.

To accomplish this testing task, we have constructed a set of PCBs that mock the components expected to be used in the final system. A functional system diagram is shown in Figure 89. We intend to produce a system that is a mockup of the complete data path for a single ladder starting and returning from the Virtex-5 development board. The wire used to connect the system boards will also be the same as what we expect to use in

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the final system. The fine twisted pair wire bringing LVDS signals to and from the ladder are 42 AWG Wiretronic part # 2-42QPN-05 in two tested lengths, 1.0 m and 2.3 m. The cables carrying the LVDS signals from the mass termination boards to the Virtex-5 interface readout boards are 3M type 3644 CL2 rated.
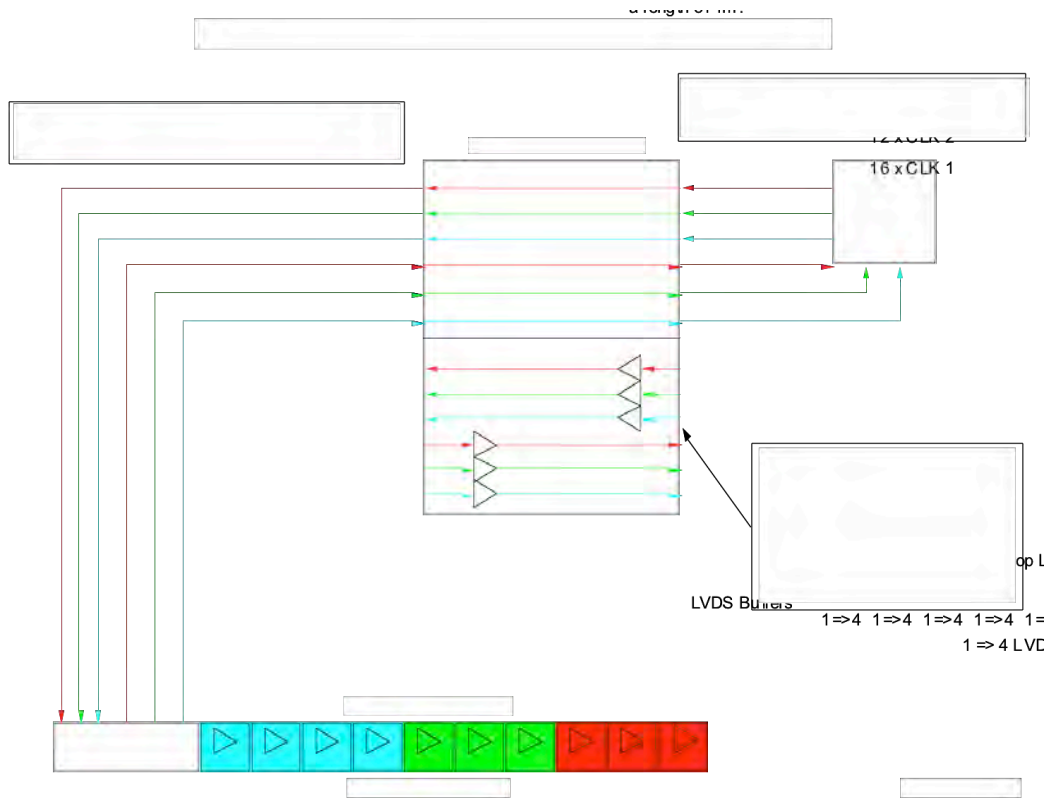

Figure 89: Functional block diagram of the LVDS data path test system.

8.1.1. Hardware

There are four basic components to the test system.

1. Mock Ladder – We have constructed a mock ladder. Since Phase-1 sensors are not available, we have used a LVDS 1:4 fan-out chip SN65LVDS104 to take the place of the Phase-1 sensor. The mock ladder contains ten SN65LVDS104s on 2 cm spacing, and six FIN1108 8-port LVDS repeater chips as buffers at the end of the ladder. The mock ladder receives 3 input LVDS signals that are multi-dropped in groups of 4, 3 and 3. Correspondingly, there are 40 outputs that are buffered at the ends of the mock ladder and carried to the Mass termination board. The mock ladder is constructed of standard FR4 with copper traces and has a finish thickness of 0.032" for 4 layers. We have constructed two mock ladders. They are identical except for the fine twisted pair signal wire lengths of 1.0 and 2.3 meters. A photograph of the mock ladder is shown as Figure 90.
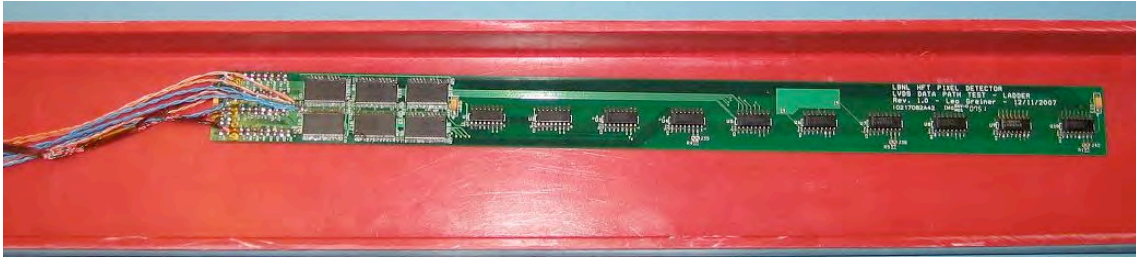
Figure 90: Mock ladder PCB as used in the tests.

2. Mass termination board – The mass termination board (MTB) is a close model of what we expect to have for a single ladder in the final system. Latch-up protected power is generated on the MTB and delivered to the mock ladder via 24 AWG wire. In the interest of testing multiple possible signal paths, the MTB used in these tests has two possible data paths. One is straight through from input to output connectors. The other is buffered with the same FIN1108 parts used on the mock ladder. A photograph of the MTB is shown as Figure 91.
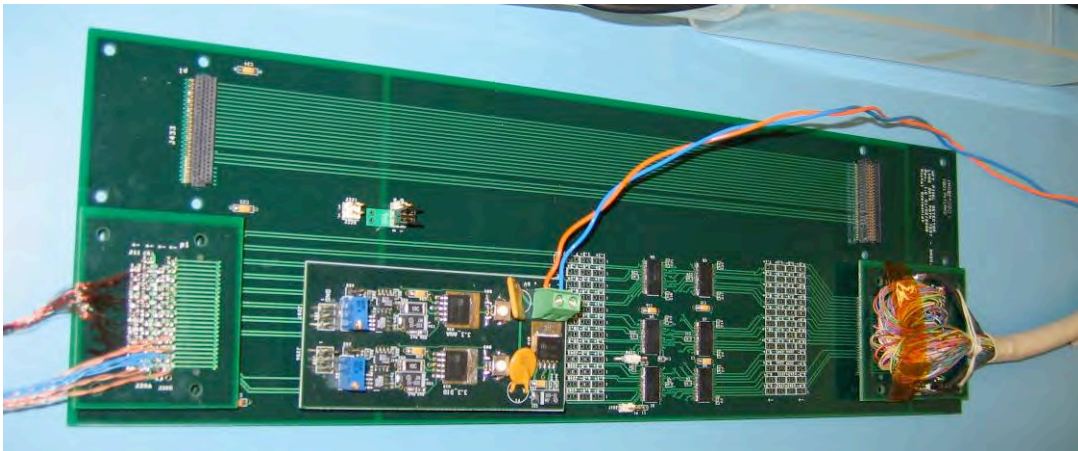

Figure 91: Mass termination board as used in the test. Ladder connection is to the left of the board, 6m cable to Virtex5 interface RDO board is on the right. The daughter card mounted to the middle of the board supplies latch up protected and monitored power. Note that there are two data paths. One is un-buffered and the other is buffered through Fin1108 LVDS buffers.

3. Virtex-5 interface – The Virtex-5 interface board (V5IB) attaches to the Xilinx Virtex-5 development board with a 1200 contact points. The data signals into and out of the Xilinx V-5 are buffered on the V5IB with FIN1108s. There are test points to look at all differential signals.
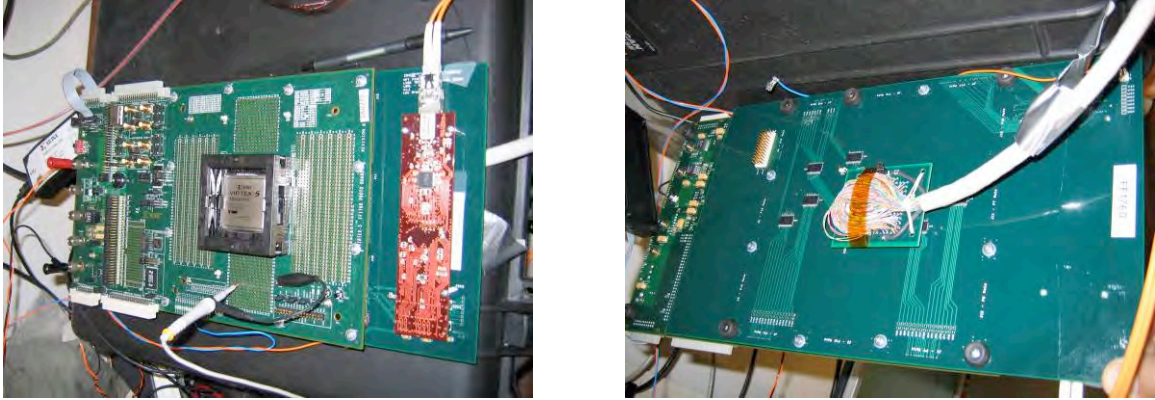
Figure 92: Vertex-5 interface board mounted to the Xilinx Virtex-5 development board. The top view is on the left showing the Xilinx Virtex-5 development board on top with the SIU visible on the V5IB. The photograph on the right shows the cable attachment and test points on the V5IB.

8.1.2. Firmware and Software

The firmware and software developed for the test have the primary task of measuring the time offsets needed to calibrate the IODELAY elements in the Virtex-5 FPGA. The IODELAY element is a function in the Xilinx Virtex-5 family of FPGAs that allows for the adjustment of the latching time on any input pin(s) with a very fine granularity. This is the essential functionality that allows us to do a channel by channel adjustment for each input. This compensates for all fixed time shifts in the system due to cable lengths, buffer propagation times, etc and allows the data transfer to be limited only by the intrinsic system jitter. There are two modes for operation of the firmware. The first mode of operation is a calibration of the system. In this mode, the firmware sends a single pulse through each channel of the system. The transit time through the system is measured for each LVDS channel and that data is sent over the fiber optic communication link (SIU) to the software in the DAQ RDO PC. The firmware then executes a sequence of steps where the timing of the latching of data into each of the FPGA inputs is varied in 75 ps steps via the IODELAY element and the transition of the received pulse from one clock cycle into the next is observed. This procedure is repeated 20 times for each input to map the range of the jitter envelope. The data is transferred via the SIU into the software in the DAQ PC where it is used to calculate the optimum delay setting for each individual input that places the average midpoint of the data pulse at the FPGA latch time. This data is then transferred back into the FPGA to set the optimum delay for each i/o pin and the FPGA is then set to the bit error rate mode. In this mode, pseudo random data is generated and transferred (with different offsets) over the three data outputs. In the firmware, each data path is checked against what was sent and errors are counted.

8.1.3. Operation of the LVDS Test System

The Virtex-5 development board generates 3 streams of pseudo random data that are fed through the data path chain and returned to the V5IB. Each stream of data is compared to what was sent and any errors are counted. The results are then displayed on LEDs on the

V5 development board and can be read out over the SIU interface. In this way we have tested the following;

- 1 full data path for a complete ladder.
- Multi-drop LVDS distribution in groups on 4, 3, 3.
- Cross-talk through the whole system – each muti-drop group carries different random data.
- The signal paths on the PCBs and the cabling are as comparable as possible to the final implementation.
- External SIU communication and software/firmware to set IODELAY for each channel.
- Bit error rate for different read out frequencies, paths, cables, etc.

8.1.4.   Results

The test system was used to evaluate the system response to data transfer frequency, fine twisted pair wire length and buffering in the data path on the MTB. Some representative eye patterns are shown below.

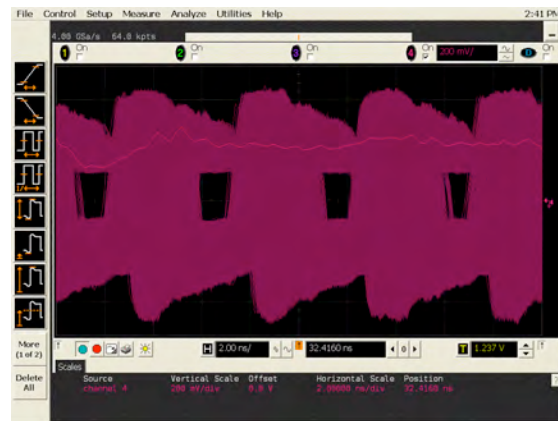**Buffered** path 200 MHz 1.0 m cables   **Un-buffered** path 200 MHz 1.0 m cables

Figure 93: Test results: Oscilloscope pictures with 2ns per division.

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