HFT Pre-CD2 Deliverables

# Evaluation SSD vs $2^{nd}$ IST layer

## Response to issues raised during

## the HFT CD-1 review on Nov. 12, 2009

Dec. 29, 2009

# 1 Introduction

This report evaluates the possibility of completely replacing the Silicon Strip Detector (SSD) with a second layer of the Intermediate Silicon Tracker (IST). We will investigate the optimum placement of such a layer and the consequences for the budget and the schedule. In all cases we will try to keep cost and schedule increase to a minimum by copying as much as possible the structures of the first IST layer which is located at a radius of 14 cm. This means that also the same internal sensor geometry will be used. We have shown in the Heavy Flavor Tracker (HFT) Conceptual Design Report [1] that this geometry works well at 14 cm. Since issues like occupancy and multiple hit ambiguities are even less of a problem at larger radii we will not discuss them any further in this report.

The APV25-S1 readout chip dead time arising from large input signals, is being discussed in a separate report. Although these Highly Ionizing Particle (HIP) events will be present in the IST layer at 14 cm, their effect is well below the 1% level. For a larger radii layer the effect, since it is determined by the particle flux, is expected to fall at least as fast as 1/r.

## 2 Performance second IST layer vs SSD

Figure 1 shows a side- and front cross-sectional view of the Heavy Flavor Tracker (HFT) as presented in the Conceptual Design Report (CDR). We were asked to review the possibility to replace the Silicon Strip Detector (SSD) layer by another Intermediate Silicon Tracker (IST) layer. The second IST layer should be positioned in such a way as not to compromise too much on the performance that is envisioned with a configuration that includes the SSD. However, the system performance will suffer because the spatial resolution of the SSD is significantly better than that of the IST. Because of the effort involved, a radical redesign of the current IST to adapt it more to the SSD specifications is not a realistic possibility. Therefor, we have to study what the performance degradation will be when replacing the SSD with another IST layer.

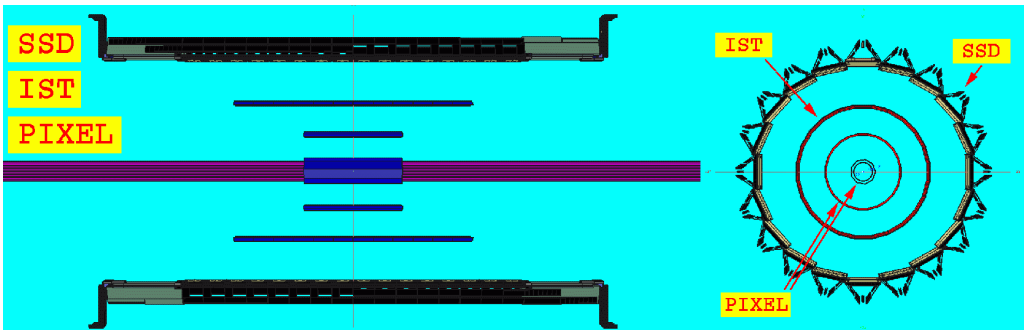



Figure 1: Side view (left picture) and cross-sectional view (right picture) of the Heavy Flavor Tracker configuration.

The figure of merit which played a key design role in the HFT CDR is the single track efficiency. In particular the single track efficiency at 750 MeV/c was used in our studies because these are expected to be the most abundant daughters for $D^0$ decay. Figure 2 shows the relative efficiency of the HFT system as a function of the radius at which a second IST would be placed. This efficiency was normalized to the efficiency of the system including the SSD and shows immediately the effect of the worse resolution of the IST if it would be used as a replacement. A straight replacement of the SSD layer at 23 cm by an IST layer at the same radius would lead to a drop in efficiency of about 6%. Optimizing the radius for the IST internal geometry, i.e. putting the layer at a radius of about 27 cm just doesn't make much sense. The total

surface would need to be covered is about 4 times as much as that of the IST layer at 14 cm. This would make the cost of this new layer comparable to the total project cost of the HFT. Also the resulting long ladders would make it necessary to rethink their mechanical rigidity and supports. The ladders in the IST layer at 14 cm are rigid enough to be only supported at their ends. A similar ladders at 27 cm would be twice as long and would need additional supports in the middle or would need to be made stiffer, leading to a higher material budget.

Moreover, the efficiency doesn't change too much going from a second IST layer located very close to the first IST layer to a second IST layer located as far out as 40 cm. We think that locating this second layer rather close to the first layer offers the most cost effective solution if we want to replace the SSD tracking capabilities by a second IST layer.

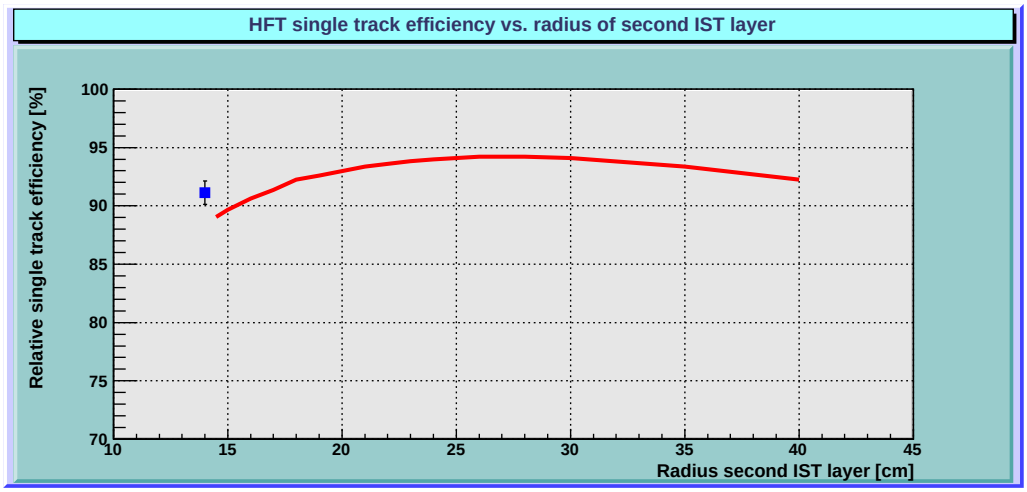



Figure 2: Relative efficiency of the total HFT tracking system as a function of the radius of a second IST layer that would be replacing the SSD. This efficiency is normalized to the efficiency when the SSD is included in the tracking system, i.e. the configuration as proposed in the Conceptual Design Report [1]. The single blue marker at a radius of 14 cm represents the relative efficiency when there is no SSD and just one IST layer at a radius of 14 cm.

# 3 An IST-like replacement for the SSD

As argued in section 2 the most cost effective placement of the second IST layer would be as close as possible to the first IST layer at 14 cm. If we want to keep the second IST layer as similar as possible to the first layer then the mechanical support structures will constrain the location. Figure 3 shows an engineering drawing cross section of the HFT as it described in the CDR. From this drawing we have determined that if we want to make second IST layer a scaled up version of the first layer that this second layer can be located no closer than at a radius of 19 cm.

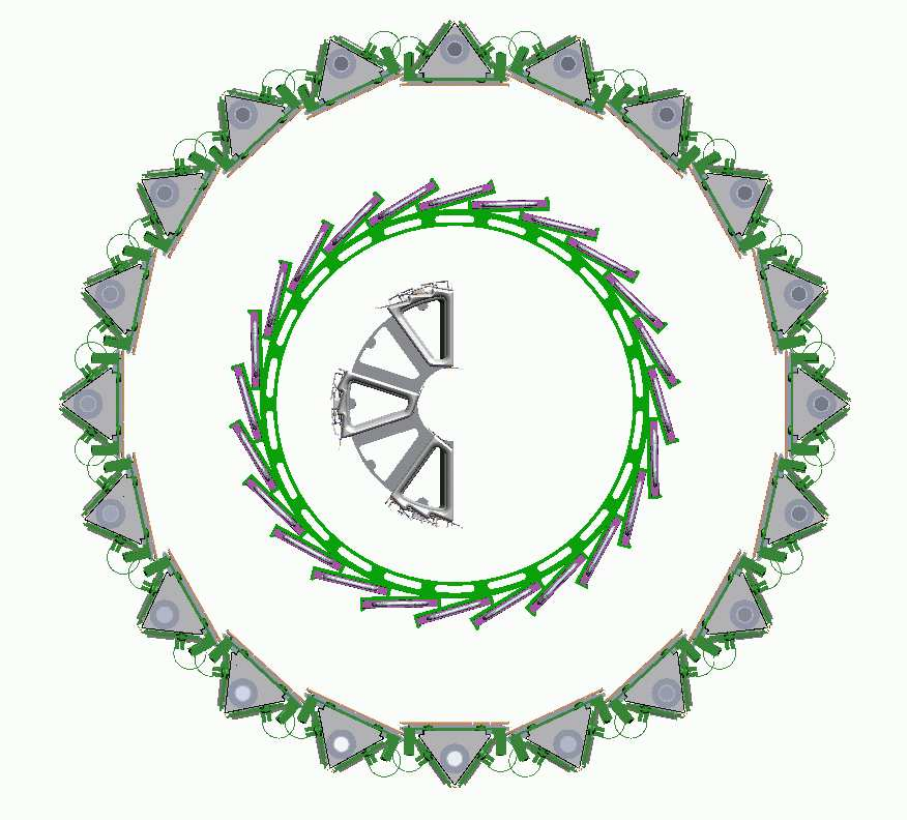


Figure 3: A more detailed (SolidWorks) view of the 3 detector layers of the IST. From inside out; Half of the PIXEL layer, the IST layer at 14 cm and the SSD layer at 23 cm.

This choice leads to ladders with 4 IST modules (i.e. 8 IST sensors) and a

length of about 65 cm. We think this length will pose no problem for rigidity or for mounting with just end supports like is done for the first IST layer. To fill the layer at 19 cm radius 32 of these ladders are needed.

| Item | IST14 Amount | Spares | IST19 Amount | Spares |
|---|---|---|---|---|
| Number of channels | 110592 | | 196608 | |
| Sensors | 144 | 24 | 256 | 40 |
| Hybrids | 72 | 12 | 128 | 40 |
| APV25 chips | 864 | 144 | 1536 | 240 |
| Ladders | 24 | 4 | 32 | 5 |
| Cables | 72 | 12 | 128 | 20 |
| Transition Boxes | 6 | 1 | 8 | 1 |
| Bias supplies | 6 | 2 | 8 | 2 |
| Readout Crates | 2 | 1 | 4 | 1 |
| Data Transmitters | 6 | 2 | 11 | 2 |
| Readout ARM's | 36 | 4 | 64 | 6 |
| Readout ARC's | 6 | 1 | 11 | 2 |
| Data Receivers | 3 | 2 | 6 | 1 |
| DAQ computers | 1 | 1 | 2 | 1 |
| Cooling | 1 | | 1 | |
| Mounting crowns | 4 | 2 | 4 | 2 |
| Support cylinder | 1 | | 1 | |

Table 1: Material needed for an IST layer at a radius of 14cm (IST14) and at a radius of 19cm (IST19)

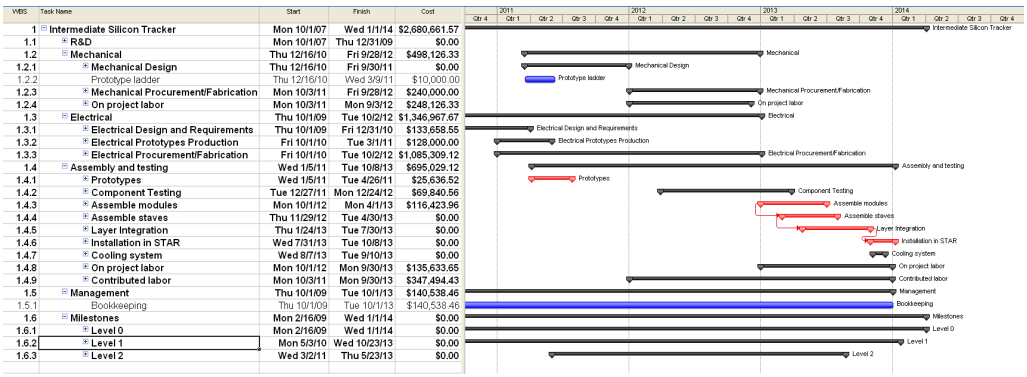
Table 3 gives the number of components needed for the IST layer at a radius of 14cm and for a new layer at 19cm. Most of the numbers scale roughly with a factor of 1.7 between larger and smaller layer.

# 4 Cost and schedule of a second IST layer

In section 3 we have shown there is a rough scaling of 1.7 between the IST layer at 14cm and the larger layer at 19cm. We expect this scaling to not only hold for the material cost but also for labor and schedule.

By modifying the existing Work Breakdown Schedule (WBS) for the IST, see figure 4, we tried to get a reasonable estimate for the extra cost of the larger layer. We added the material needed to build the larger IST layer and added the necessary labor based on the smaller layer and multiplied by a factor of 1.7. Because we are using almost identical building blocks in the small and large layer, most of the R&D costs do not have to be taken into account for the second layer. Figure 5 shows a view of the resulting WBS for the IST with 2 layers. The result of this exercise was that the total cost of the IST went up from \$2.6M to \$6.0M. This means that the additional cost of the larger layer is about \$3.4M.

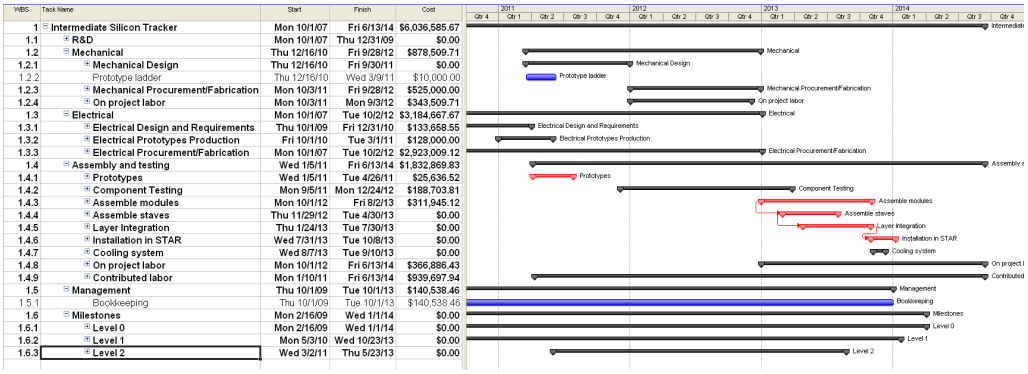
When adapting the original WBS we focused on the financial aspects of the second layer rather than trying to get the time schedule right. For this reason the schedule shown in the time scale of figure 5 is not correct. In reality the time needed to complete the second layer will extend the duration of the project significantly. Assembling and testing the small IST layer will take roughly 2 years. Since a lot will have been learned from building the first layer, a second will probably take a little less time overall. Still, we will have to reckon with about 3 years to put this larger layer together.



| WBS | Task Name | Start | Finish | Cost |
|---|---|---|---|---|
| 1 | Intermediate Silicon Tracker | Mon 10/1/07 | Wed 1/1/14 | $2,680,661.57 |
| 1.1 | R&D | Mon 10/1/07 | Thu 12/31/09 | $0.00 |
| 1.2 | Mechanical | Thu 12/16/10 | Fri 9/28/12 | $498,126.33 |
| 1.2.1 | Mechanical Design | Thu 12/16/10 | Fri 9/30/11 | $0.00 |
| 1.2.2 | Prototype ladder | Thu 12/16/10 | Wed 3/9/11 | $10,000.00 |
| 1.2.3 | Mechanical Procurement/Fabrication | Mon 10/3/11 | Fri 9/28/12 | $240,000.00 |
| 1.2.4 | On project labor | Mon 10/3/11 | Mon 9/3/12 | $248,126.33 |
| 1.3 | Electrical | Thu 10/1/09 | Tue 10/2/12 | $1,346,967.67 |
| 1.3.1 | Electrical Design and Requirements | Thu 10/1/09 | Fri 12/31/10 | $133,658.55 |
| 1.3.2 | Electrical Prototypes Production | Fri 10/1/10 | Tue 3/1/11 | $128,000.00 |
| 1.3.3 | Electrical Procurement/Fabrication | Fri 10/1/10 | Tue 10/2/12 | $1,085,309.12 |
| 1.4 | Assembly and testing | Wed 1/5/11 | Tue 10/8/13 | $695,029.12 |
| 1.4.1 | Prototypes | Wed 1/5/11 | Tue 4/26/11 | $25,636.52 |
| 1.4.2 | Component Testing | Tue 12/27/11 | Mon 12/24/12 | $69,840.56 |
| 1.4.3 | Assemble modules | Mon 10/1/12 | Mon 4/1/13 | $116,423.96 |
| 1.4.4 | Assemble staves | Thu 11/29/12 | Tue 4/30/13 | $0.00 |
| 1.4.5 | Layer Integration | Thu 1/24/13 | Tue 7/30/13 | $0.00 |
| 1.4.6 | Installation in STAR | Wed 7/31/13 | Tue 10/8/13 | $0.00 |
| 1.4.7 | Cooling system | Wed 8/7/13 | Tue 9/10/13 | $0.00 |
| 1.4.8 | On project labor | Mon 10/1/12 | Mon 9/30/13 | $135,633.65 |
| 1.4.9 | Contributed labor | Mon 10/3/11 | Mon 9/30/13 | $347,494.43 |
| 1.5 | Management | Thu 10/1/09 | Tue 10/1/13 | $140,538.46 |
| 1.5.1 | Bookkeeping | Thu 10/1/09 | Tue 10/1/13 | $140,538.46 |
| 1.6 | Milestones | Mon 2/16/09 | Wed 1/1/14 | $0.00 |
| 1.6.1 | Level 0 | Mon 2/16/09 | Wed 1/1/14 | $0.00 |
| 1.6.2 | Level 1 | Mon 5/3/10 | Wed 10/23/13 | $0.00 |
| 1.6.3 | Level 2 | Wed 3/2/11 | Thu 5/23/13 | $0.00 |



Figure 4: View of the Work Breakdown Schedule for the IST layer at 14cm as described in the HFT Conceptual Design Report [1]. The total cost of the IST project adds up to about \$2.68M, before contingency.



| WBS | Task Name | Start | Finish | Cost |
|---|---|---|---|---|
| 1 | Intermediate Silicon Tracker | Mon 10/1/07 | Fri 6/13/14 | $6,036,585.67 |
| 1.1 | R&D | Mon 10/1/07 | Thu 12/31/09 | $0.00 |
| 1.2 | Mechanical | Thu 12/16/10 | Fri 9/28/12 | $878,509.71 |
| 1.2.1 | Mechanical Design | Thu 12/16/10 | Fri 9/30/11 | $0.00 |
| 1.2.2 | Prototype ladder | Thu 12/16/10 | Wed 3/9/11 | $10,000.00 |
| 1.2.3 | Mechanical Procurement/Fabrication | Mon 10/3/11 | Fri 9/28/12 | $525,000.00 |
| 1.2.4 | On project labor | Mon 10/3/11 | Mon 9/3/12 | $343,509.71 |
| 1.3 | Electrical | Mon 10/1/07 | Tue 10/2/12 | $3,184,667.67 |
| 1.3.1 | Electrical Design and Requirements | Thu 10/1/09 | Fri 12/31/10 | $133,658.55 |
| 1.3.2 | Electrical Prototypes Production | Fri 10/1/10 | Tue 3/1/11 | $128,000.00 |
| 1.3.3 | Electrical Procurement/Fabrication | Mon 10/1/07 | Tue 10/2/12 | $2,923,009.12 |
| 1.4 | Assembly and testing | Wed 1/5/11 | Fri 6/13/14 | $1,832,869.83 |
| 1.4.1 | Prototypes | Wed 1/5/11 | Tue 4/26/11 | $25,636.52 |
| 1.4.2 | Component Testing | Mon 9/5/11 | Mon 12/24/12 | $188,703.81 |
| 1.4.3 | Assemble modules | Mon 10/1/12 | Fri 8/2/13 | $311,945.12 |
| 1.4.4 | Assemble staves | Thu 11/29/12 | Tue 4/30/13 | $0.00 |
| 1.4.5 | Layer Integration | Thu 1/24/13 | Tue 7/30/13 | $0.00 |
| 1.4.6 | Installation in STAR | Wed 7/31/13 | Tue 10/8/13 | $0.00 |
| 1.4.7 | Cooling system | Wed 8/7/13 | Tue 9/10/13 | $0.00 |
| 1.4.8 | On project labor | Mon 10/1/12 | Fri 6/13/14 | $366,886.43 |
| 1.4.9 | Contributed labor | Mon 1/10/11 | Fri 6/13/14 | $939,697.94 |
| 1.5 | Management | Thu 10/1/09 | Tue 10/1/13 | $140,538.46 |
| 1.5.1 | Bookkeeping | Thu 10/1/09 | Tue 10/1/13 | $140,538.46 |
| 1.6 | Milestones | Mon 2/16/09 | Wed 1/1/14 | $0.00 |
| 1.6.1 | Level 0 | Mon 2/16/09 | Wed 1/1/14 | $0.00 |
| 1.6.2 | Level 1 | Mon 5/3/10 | Wed 10/23/13 | $0.00 |
| 1.6.3 | Level 2 | Wed 3/2/11 | Thu 5/23/13 | $0.00 |

Figure 5: View of the Work Breakdown Schedule from figure 4, but now with a second IST layer at 19cm factored in. The emphasis was on the increase in material cost and labor, no attempt was made to make the time scheduling realistic. The total cost of the IST project with 2 layers adds up to approximately $6.04M, before contingency.

# 5 Conclusion

In this report we have shown that it is possible to replace the existing Silicon Strip Detector (SSD) at a radius of 23cm with an additional Intermediate Silicon Tracker IST layer at 19cm. To keep the cost and effort down this new layer should be positioned at a radius of 19cm and it should copy as much as possible of the components of the layer at 14cm. Because of the worse position resolution of the IST sensors with respect to the SSD sensors there will be a 7—8% loss in the single track efficiency of the whole Heavy Flavor Tracker (HFT).

We have made a detailed study of the expected cost increase for the whole HFT project when replacing the SSD by a second IST layer. By adding the extra material and labor cost of the second layer to the existing Work Breakdown Schedule of the single layer IST project, we concluded that the second layer leads to a cost increase of $3.4M, before contingency.

With similar human resources as for the first IST layer, we expect that it will take 2 to 3 extra years to produce the second layer. This estimate is based on the observation that the amount of effort roughly scales with the number of channels, also taking into account the already existing experience resulting from production of the first IST layer.

From a cost-benefit point of view building a second IST layer for $3.4M instead of refurbishing the existing SSD for about $0.8M doesn't make much sense. Even if parts of the refurbished SSD would not be functional then the IST layer at 14cm will already ensure that there is not more than 9—10% loss in efficiency in those areas. This has to be compared to the 7—8% overall loss of efficiency when replacing the whole SDD with an IST layer at 19cm.

Furthermore, the additional 2 to 3 years of added IST project time when building the second layer has not been anticipated by the participating institutes. Reassigning physicists and students to building another layer instead of participating in the physics analysis of the already functioning parts of the HFT (PIXEL, IST layer at 14cm and SSD) will be very difficult to defend. The same physicists and students are also expected to commission and operate the HFT system. This is especially important in the first year of operation and we can safely assume that a production of the second layer will only start after the end of the first run in which the HFT participates. From this we expect the second layer to probably be installed 3 years after PIXEL, IST layer at 14cm and possibly SSD are installed. Most likely, a big portion of the HFT physics program will have been completed by then.

Taking cost, effort, schedule and performance into account, we come to the conclusion that replacing the SSD by another IST layer is feasible but not a desirable and most likely also not a viable option.

# References

[1] The Heavy Flavor Tracker Conceptual Design Report, November 11, 2009.